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# NTE74HC374
# Integrated Circuit
# TTL – High Speed CMOS,
# Octal D–Type Flip–Flop with 3–State Outputs
# Common Output Control and Common Clock

**Description:**

The NTE74HC374 is a high speed octal D–type flip–flop with 3–state outputs in a 20–Lead DIP type package with the capability to drive 15 LS–TTL loads. The eight edge–triggered flip–flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ($\overline{OE}$) controls the 3–state outputs and is independent of the register operation. When $\overline{OE}$ is HIGH, the outputs are in the high–impedance state.

**Features:**

- Wide Power Supply Range: 2V to 6V
- High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V
- Buffered Inputs
- Common Three–State Output Enable Control
- Three–State Outputs
- Bus Line Driving Capability
- Typical Propagation Delay (Clock to Q): 15ns at $V_{CC}$ = 5V, $C_L$ = 15pF, $T_A$ = +25°C
- Fanout (Over Temperature Range):
  - Standard Outputs . . . 10 LS–TTL Loads
  - Bus Driver Outputs . . 15 LS–TTL Loads

**Absolute Maximum Ratings:** (Note 1, Note 2)

Supply Voltage, $V_{CC}$ . . . . . –0.5 to +7.0V
Clamp Diode Current, $I_{IK}$, $I_{OK}$ . . . . . ±20mA
DC Drain Current (Per Output), $I_{OUT}$ . . . . . ±35mA
DC Output Source or Sink Current (Per Output), $I_{OUT}$ . . . . . ±25mA
DC $V_{CC}$ or GND Current (Per Pin), $I_{CC}$ . . . . . ±50mA
Maximum Junction, $T_J$ . . . . . +150°C
Storage Temperature Range, $T_{stg}$ . . . . . –65°C to +150°C
Typical Thermal Resistance, Junction–to–Ambient, $R_{thJA}$ . . . . . 69°C/W
Lead Temperature (During Soldering, 10sec), $T_L$ . . . . . +300°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.

## Recommended Operating Conditions:

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 2.0 | – | 6.0 | V |
| DC Input or Output Voltage | $V_{IN}$, $V_{OUT}$ | 0 | – | $V_{CC}$ | V |
| Operating Temperature Range | $T_A$ | –40 | – | +85 | °C |
| Input Rise or Fall Times | $t_r$, $t_f$ | | | | |
| $V_{CC}$ = 2.0V | | – | – | 1000 | ns |
| $V_{CC}$ = 4.5V | | – | – | 500 | ns |
| $V_{CC}$ = 6.0V | | – | – | 400 | ns |

## DC Electrical Characteristics:

| Parameter | Symbol | Test Conditions | | $V_{CC}$ | $T_A$ = +25°C | $T_A$ = –40° to +85°C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Typ | Guaranteed Limits | | |
| Minimum HIGH Level Input Voltage | $V_{IH}$ | | | 2.0 | – | 1.5 | 1.5 | V |
| | | | | 4.5 | – | 3.15 | 3.15 | V |
| | | | | 6.0 | – | 4.2 | 4.2 | V |
| Maximum LOW Level Input Voltage | $V_{IL}$ | | | 2.0 | – | 0.5 | 0.5 | V |
| | | | | 4.5 | – | 1.35 | 1.35 | V |
| | | | | 6.0 | – | 1.8 | 1.8 | V |
| Minimum HIGH Level Output Voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OUT}$ = –20μA | – | $V_{CC}$ | $V_{CC}$ –0.1 | $V_{CC}$ –0.1 | V |
| | | | $I_{OUT}$ = –6mA | 4.5 | – | 3.98 | 3.84 | V |
| | | | $I_{OUT}$ = –7.8mA | 6.0 | – | 5.48 | 5.34 | V |
| Minimum LOW Level Output Voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OUT}$ = 20μA | – | – | 0.1 | 0.1 | V |
| | | | $I_{OUT}$ = 6mA | 4.5 | 0.2 | 0.26 | 0.33 | V |
| | | | $I_{OUT}$ = 7.8mA | 6.0 | 0.2 | 0.26 | 0.33 | V |
| Maximum Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | – | ±0.1 | ±1.0 | μA |
| Maximum Quiescent Supply Current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0μA | | 6.0 | – | 8.0 | 80 | μA |
| Three–State Leakage Current | $I_{OZ}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 6.0 | – | ±0.5 | ±5.0 | μA |

## Prerequisite for Switching Specifications:

| Parameter | Symbol | Test Conditions | $V_{CC}$ | $T_A$ = +25°C | $T_A$ = –40° to +85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| Maximum Clock Frequency | $f_{MAX}$ | | 2.0 | – | 6 | 5 | MHz |
| | | | 4.5 | – | 30 | 25 | MHz |
| | | | 6.0 | – | 35 | 29 | MHz |
| Clock Pulse Width | $t_W$ | | 2.0 | – | 80 | 100 | ns |
| | | | 4.5 | – | 16 | 20 | ns |
| | | | 6.0 | – | 14 | 17 | ns |
| Setup Time (Date to Clock) | $t_{SU}$ | | 2.0 | – | 60 | 75 | ns |
| | | | 4.5 | – | 12 | 15 | ns |
| | | | 6.0 | – | 10 | 13 | ns |
| Hold Time (Date to Clock) | $t_H$ | | 2.0 | – | 5 | 5 | ns |
| | | | 4.5 | – | 5 | 5 | ns |
| | | | 6.0 | – | 5 | 5 | ns |

**Switching Specifications:** ($t_r = t_f$ = 6ns unless otherwise specified)

| Parameter | Symbol | Test Conditions | $V_{CC}$ | $T_A$ = +25°C | $T_A$ = −40° to +85°C | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| Propagation Delay Time (Clock to Output) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2.0 | – | 165 | 205 | ns |
| | | | 4.5 | – | 33 | 41 | ns |
| | | $C_L$ = 15pF | 5.0 | 15 | – | – | ns |
| | | $C_L$ = 50pF | 6.0 | – | 28 | 35 | ns |
| Propagation Delay Time (Disable to Q) | $t_{PLZ}$, $t_{PHZ}$ | $C_L$ = 50pF | 2.0 | – | 135 | 170 | ns |
| | | | 4.5 | – | 27 | 34 | ns |
| | | $C_L$ = 15pF | 5.0 | 11 | – | – | ns |
| | | $C_L$ = 50pF | 6.0 | – | 23 | 29 | ns |
| Propagation Delay Time (Output Enable to Q) | $t_{PZL}$, $t_{PZH}$ | $C_L$ = 50pF | 2.0 | – | 150 | 190 | ns |
| | | | 4.5 | – | 30 | 38 | ns |
| | | $C_L$ = 15pF | 5.0 | 12 | – | – | ns |
| | | $C_L$ = 50pF | 6.0 | – | 26 | 33 | ns |
| Maximum Clock Frequency | $f_{MAX}$ | $C_L$ = 15pF | 5.0 | 60 | – | – | MHz |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2.0 | – | 60 | 75 | ns |
| | | | 4.5 | – | 12 | 15 | ns |
| | | | 6.0 | – | 10 | 13 | ns |
| Maximum Input Capacitance | $C_{IN}$ | | – | – | 10 | 10 | pF |
| Minimum Three−State Output Capacitance | $C_O$ | | – | – | 20 | 20 | pF |
| Power Dissipation Capacitance | $C_{PD}$ | $C_L$ = 15pF, Note 3 | 5.0 | 39 | – | – | pF |

Note 3. $C_{PD}$ is used to determine the dynamic power consumption, per channel.
$P_D = C_{PD} V_{CC}^2 fi + \Sigma V_{CC}^2 f_O C_L$ where $f_i$ = Input Frequency, $f_O$ = Output Frequency,
$C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

**Truth Table:**

| Inputs | | | Output |
|---|---|---|---|
| $\overline{OE}$ | CP | Data $D_n$ | $Q_n$ |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | Q0 |
| H | X | X | Z |

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
↑ = Transition from LOW to HIGH Level
Q0 = The level of Q before the indicated steady state input conditions were established.
Z = High Impedance State

**Pin Connection Diagram**