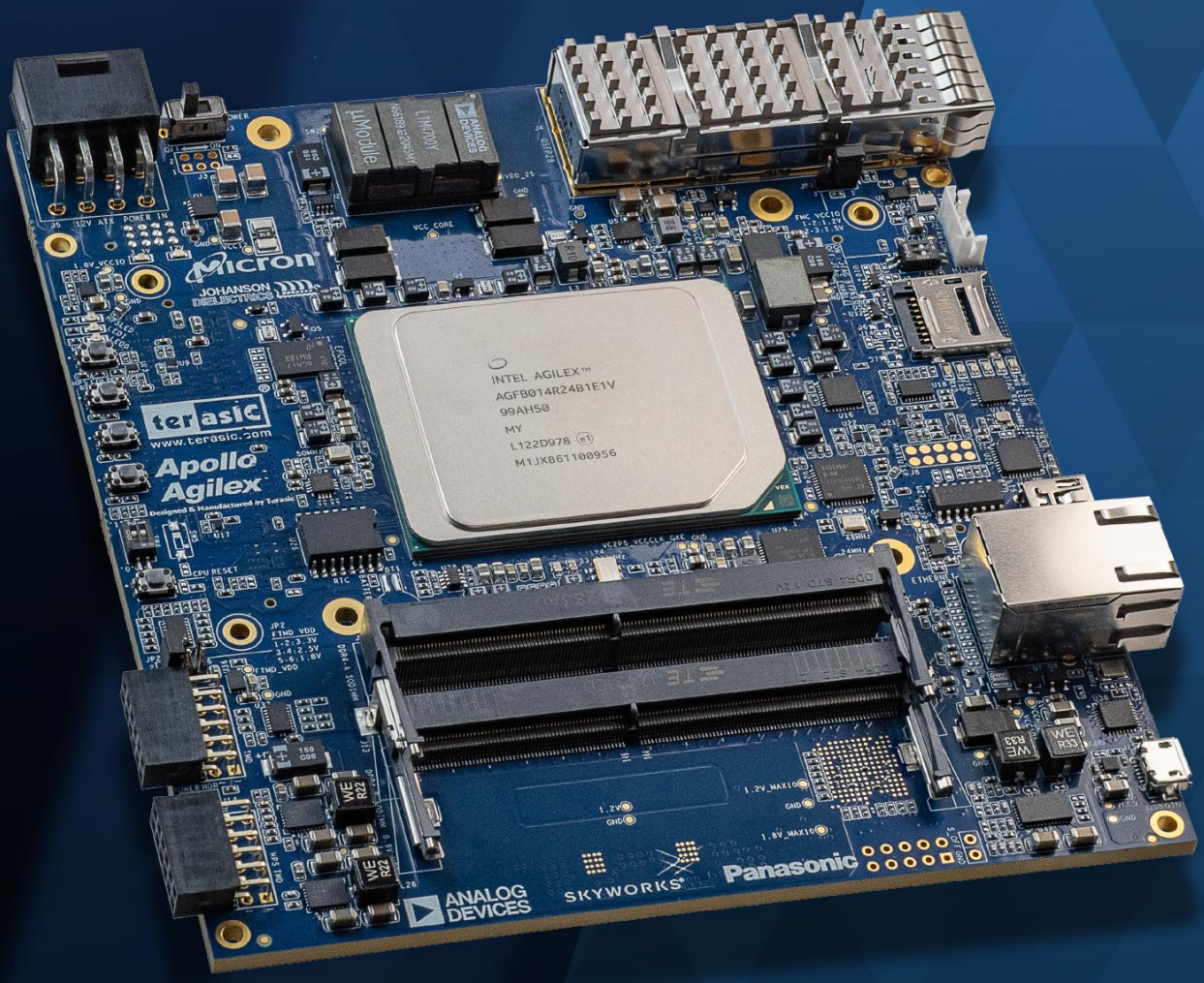
Apollo-Agilex

User Manual



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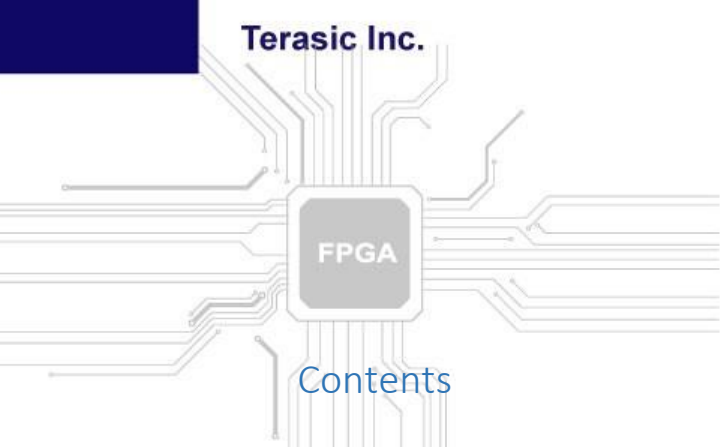

Contents

Chapter 1

Overview

This chapter provides an overview of the Apollo Agilex SoM Board and installation guide.

1.1 General Description

Designed for high-performance AI-enabled edge solutions and HPC solutions, Apollo Agilex SOM packs unbeatable performance optimization and provides highest real-time compute/watts for edge AI applications.

Apollo Agilex SOM takes advantage of the latest Intel® Agilex® SoC with 1400K logic elements to obtain performance and power breakthrough (with up to 40% lower power than Stratix 10 series). Combining high-end hardware interfaces such as two high-capacity and high-bandwidth DDR4 SO-DIMM Sockets, on-board QSFP28 connector, PCIe Gen 4x16 up to 25.8 Gbps/ch with carrier, on-board USB-Blaster II, and FMC/FMC+ connectors for I/O expansion, the board delivers more than 2X the performance of previous generation development kits.

Figure 1-1 Apollo Agilex board with heat sink and fan

1.2 Board Layout

The figures below depict the layout of the board and indicate the location of the connectors and key components.

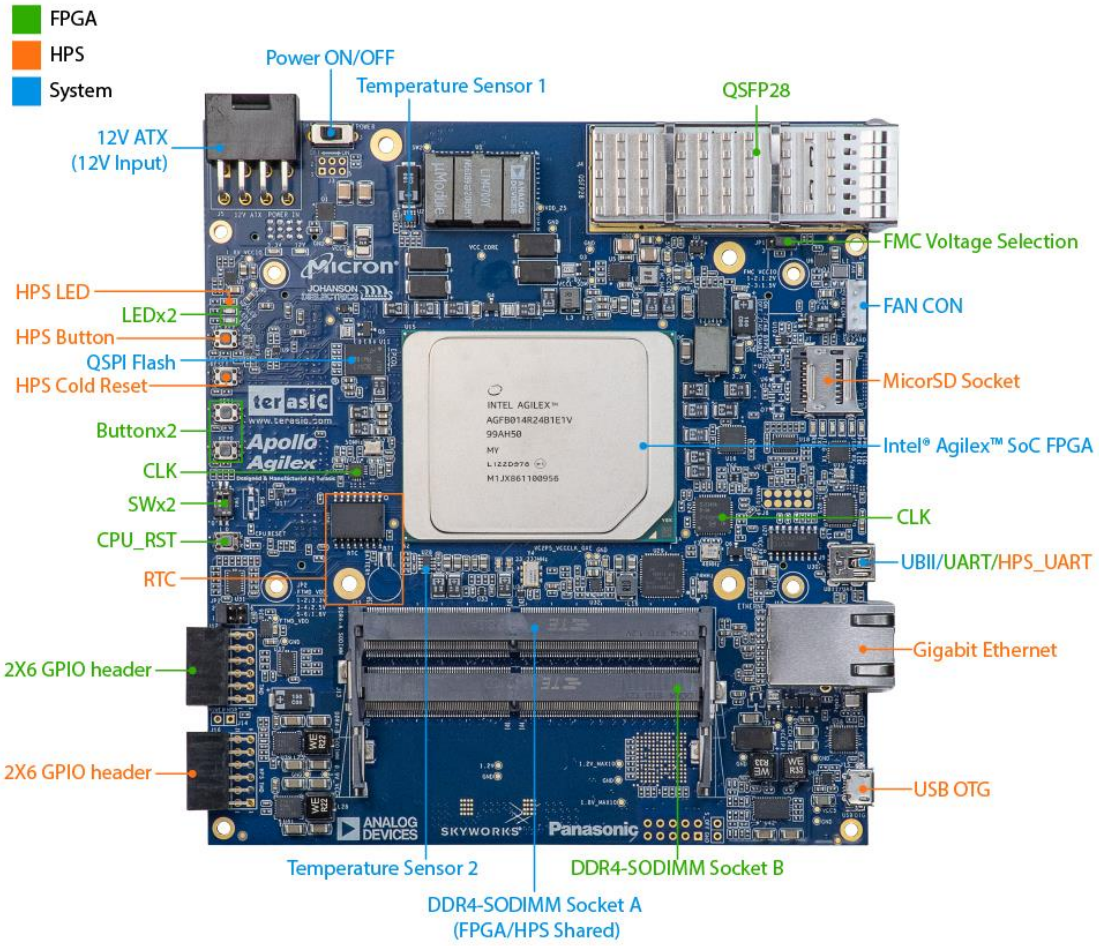

Figure 1-2 Apollo Agilex board top

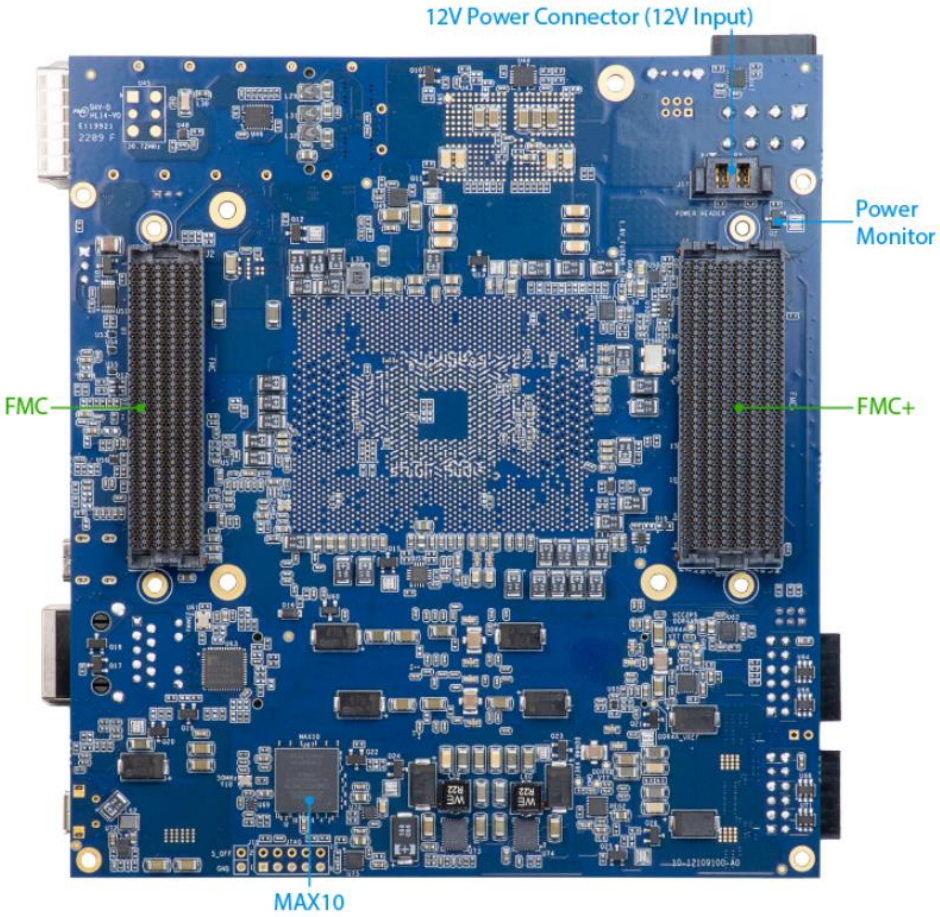

Figure 1-3 Apollo Agilex board bottom

1.3 Key Features

The following hardware is implemented on the Apollo Agilex board:

■ FPGA Device

- Intel® Agilex® SoC FPGA : AGFB014R24B1E1V/AGFB014R24B2E2V
  - 1,400K logic elements (LEs)
  - 229 Mbits embedded memory(M20K)
  - 96 transceivers (up to 28.3Gbps)
  - 11,520 18-bit x 19-bit multipliers
  - 5,760 Variable-precision DSP blocks

■ FPGA Configuration

- On-Board USB Blaster II (UB2) for FPGA programming and Debug
- AS Mode configuration from QSPI Flash

FPGA Fabric

- 1024Mbit QSPI Flash (EPCQL1024 Compliant)
- Two DDR4 SO-DIMM Sockets (each with 72-bit ECC, speed up to 2666MT/s, and size up to 16GB)
- Onboard QSFP28
- One FMC+ Connector
- One FMC Connector
- Two 50Mhz Single-ended
- 1.2V 2x6 GPIO header
- LED x2, Button x2, DIP Switch x2, CPU Reset

HPS(Hard Processor System) Fabric

- Quad-core 64 bit ARM Cortex-A53 MPCore* processor
- MicroSD Socket
- Gigabit Ethernet PHY with RJ45
- USB OTG PHY with Micro USB Connector
- UART to USB with Mini USB Connector
- LED x1, Button x1, Cold Reset Button
- 3.3V 2x6 GPIO Expansion header for GPIO/SPI/I2C/UART
- RTC

Dashboard System

- Input Power Monitor
- FPGA and Board Temperature Monitor
- Fan Control and Monitor
- Auto Fan Speed
- Auto Shutdown

Power Source

- 12V from 2x4 PCIe connector

- 12V from Samtec connector (reserved for carrier board)

1.3. Block Diagram

Figure 1-4 shows the block diagram of the Apollo Agilex board. To provide maximum flexibility for the users, all key components are connected to the Agilex® SoC FPGA device. Thus, users can configure the FPGA to implement any system design.

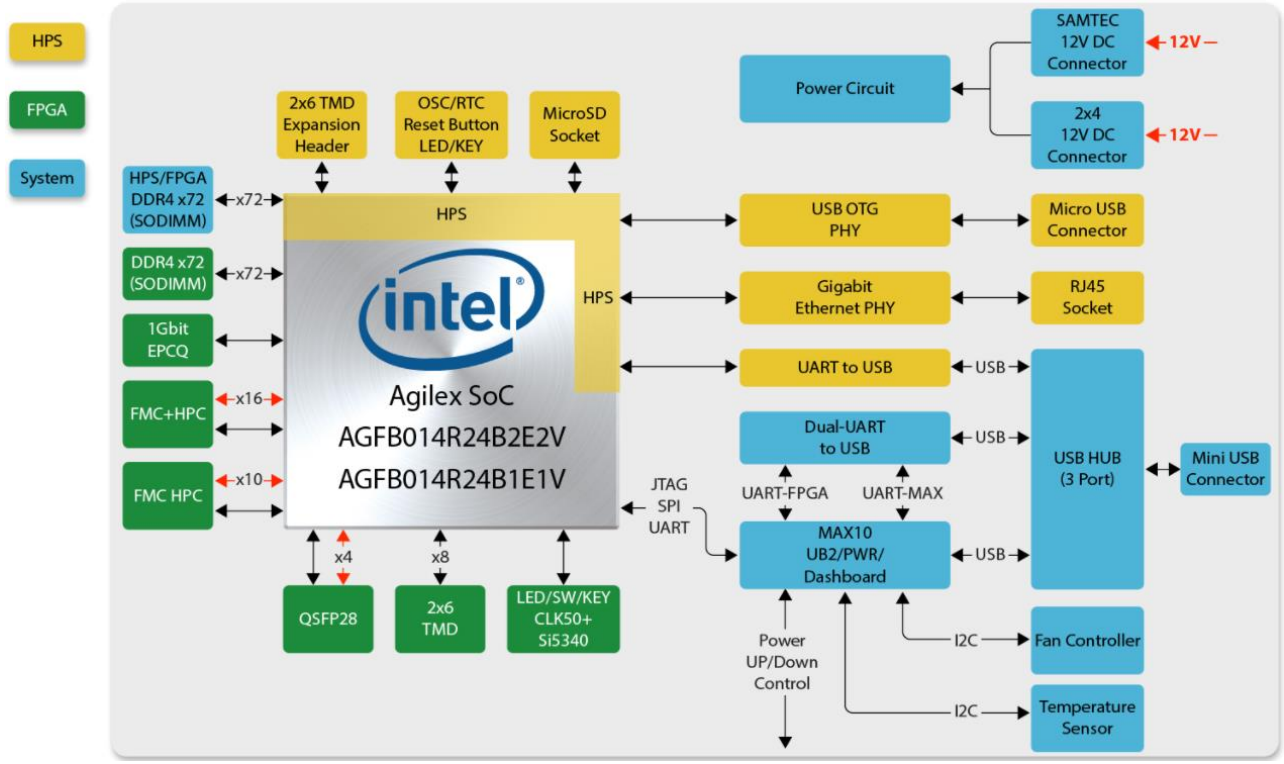

Figure 1-4 Block diagram of the Apollo Agilex board

1.4. Mechanical Specifications

Figure 1-5 shows the Mechanical Layout of Apollo Agilex board. The unit of the Mechanical Layout is millimeter (mm).

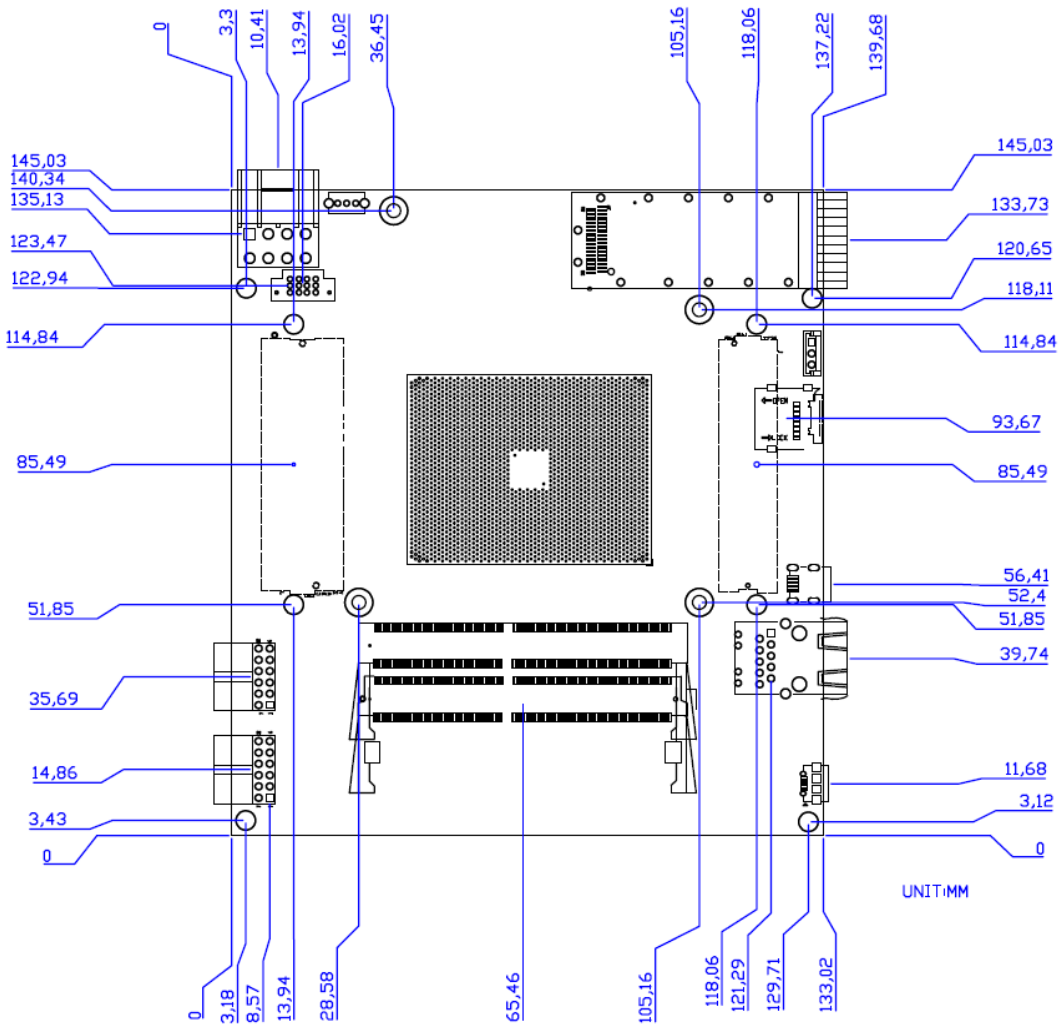

Figure 1-5 Mechanical layout

1.5. Power Requirement

■ Stand-alone mode

When the Apollo Agilex board is used in stand-alone mode, users can use the 12 V ATX power provided in the kit to connect to the 8-pin 12V ATX power connector (See **Figure 1-6**) of the Apollo Agilex.

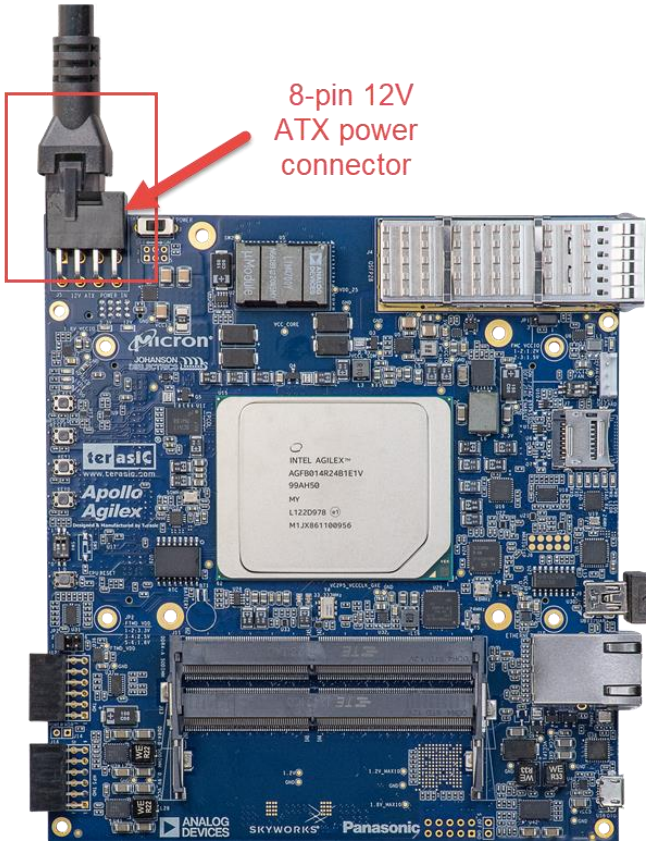

Figure 1-6 8-Pin 12V ATX Power Connector

■ Connect to the based board

If user wants use the Apollo Agilex board as the module board and connect it to the carrier board. The carrier board needs to provide at least **12V 15A** power to the J10 power connector (See **Figure 1-7**) of the Apollo Agilex board. Please note that the 12V and 3.3V of the FMC and FMC + connector are provided by the Apollo Agilex board, the carrier board does not need to provide these powers. For part number of the connector connected to J10, please refer to **Table 1-1** in the section 1.7.

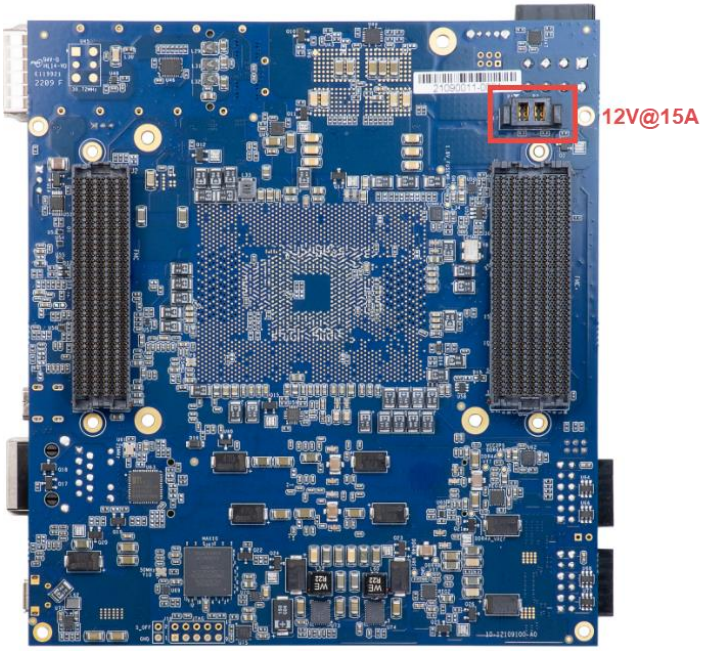

Figure 1-7 Power connector for connecting based board

1.6. Connectivity

Most of the FPGA I/O on the FMC and FMC+ connectors of the Apollo Agilex board are **1.2V standard** (*1). Therefore, if users want to connect FMC/FMC+ daughter cards or other motherboards to the Apollo Agilex board, users need to pay special attention to whether they directly support the 1.2V I/O standard.

If user wants to make their owned carrier board to connect with the Apollo Agilex board, there are three connectors are needed to be used, they are FMC +, FMC and Power connector (See 錯誤! 找不到參照來源。). The following table lists the manufacturer and manufacturer part numbers of the three connectors that can match with the connectors of the Apollo Agilex board.

*1 **:** The HPC part of the FMC+ pins can be set 1.5 or 1.2V I/O standard, please refer to section 2.2 "**FMC_VCCIO Select Header**" part for detailed.

Table 1-1 Part Number of the connector on the Apollo Agilex board

Connector	Apollo Agilex Board's Part Number	Carrier Board's Part Number
FMC	**J2**	Samtec : ASP-134488-01

	Samtec : ASP-134486-01	
FMC+	**J1** Samtec : ASP-184329-01	Samtec : ASP-184330-01
Power Connector	**J17** Samtec : UPS-02-07.0-02-L-V	Samtec : UPT-02-03.0-01-L-V

Chapter 2

Board Component

This chapter introduces all the important components on the Apollo Agilex.

2.1 Configuration Interface

This section describes the configuration mode for Agilex SoC FPGA available on the Apollo Agilex. The peripheral circuits and usage scenarios for each mode will be listed.

As shown in **Figure 2-1**, the mode select pin of the FPGA on the Apollo Agilex board has been set to **Active Serial (AS) mode** using resistors. Thus, the Apollo Agilex board supports the following configuration modes:

- JTAG Mode (Configure the FPGA using the on-board USB Blaster II).
- Active Serial (AS) mode

Users can use these modes to configure the FPGA or HPS (Hardware Process System) fabric in the Agilex SoC FPGA and make the FPGA to run the user's logic or boot the HPS to run the OS.

Below we will introduce more detailed information of AS mode, as well as other configuration information.

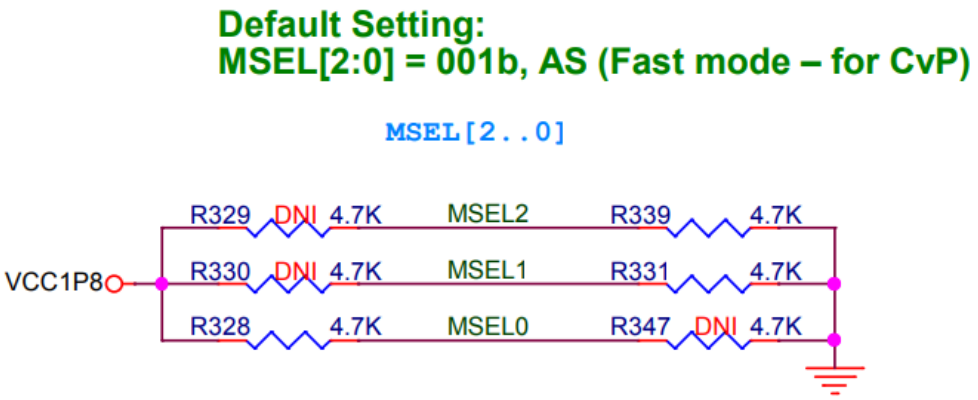

Figure 2-1 The MSEL pin setting

■ Active Serial (Fast) mode

In AS mode, the FPGA's configuration file is stored in the QSPI flash. The Secure Device Manager (SDM) in Agilex SoC FPGA is responsible for the entire AS mode process and interface. The SDM will load the initial configuration firmware from the QSPI flash to configure the FPGA including FPGA I / O and core configuration. HPS part of the boot can also be completed in this mode. **Figure 2-2** shows the architecture of the AS mode of the Apollo Agilex board.

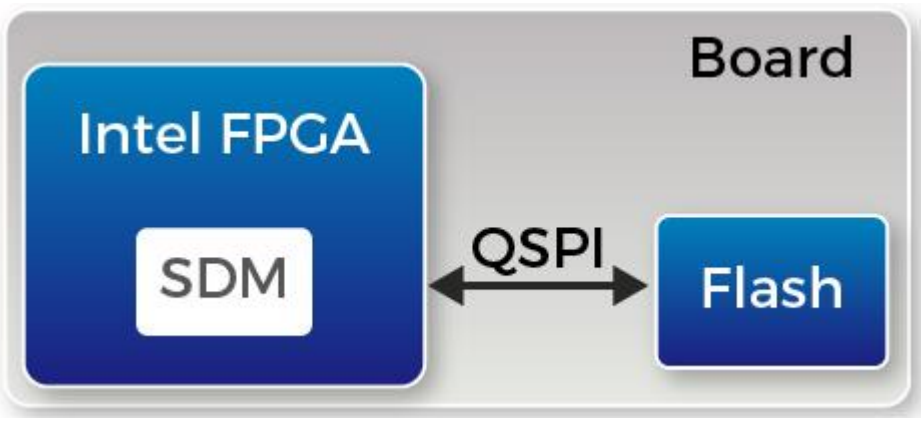

Figure 2-2 AS mode for the Apollo Agilex board

For more information on the configuration of Agilex SoC FPGAs, please refer to the file: Intel Agilex Configuration User Guide

■ SoC FPGA boot

The boot process for Agilex SoC FPGA can be divided into two different methods:

- FPGA Configuration First Mode
- HPS Boot First Mode

The difference between the two methods is the initial difference between HPS and FPGA fabric after powering on. More details can be found in the user documentation: Intel® Agilex™ SoC FPGA Boot User Guide.

The factory setting of the SoC boot of the Apollo Agilex board is the **FPGA Configuration First Mode**. The architecture is shown in the **Figure 2-3**. Two storage mediums are used. The system needs QSPI flash on Apollo Agilex as SDM flash for booting.

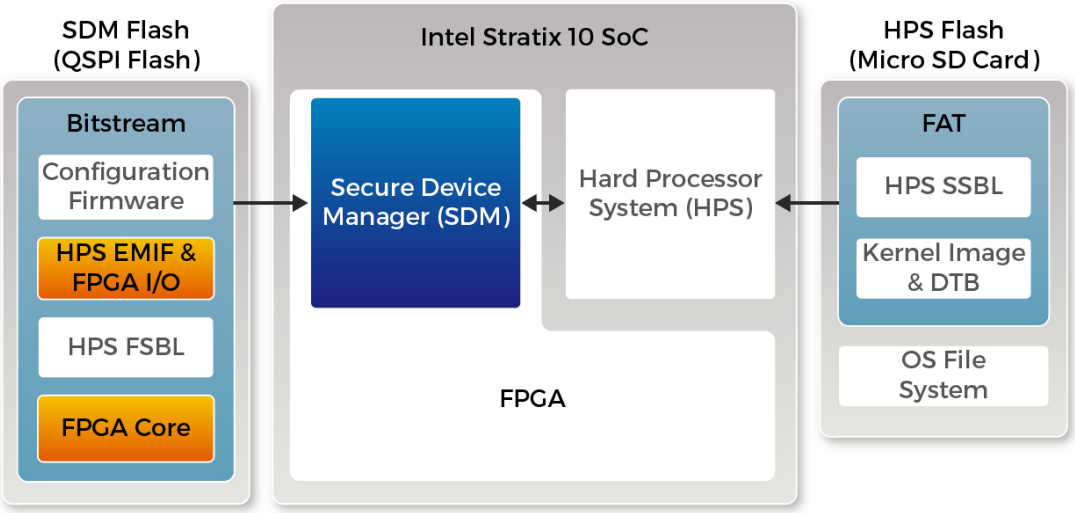

Figure 2-3 FPGA Configuration First Dual SDM and HPS Flash

The QSPI flash memory has the following boot data for the first part of the SoC FPGA configuration:

- Configuration firmware for the SDM
- FPGA I/O and HPS external memory interface (EMIF) I/O configuration data
- FPGA core configuration data
- HPS First-Stage Boot Loader(FSBL) code and FSBL hardware handoff binary data

Meanwhile, Terasic provides the micro SD card with built-in image data as HPS flash, which is used for HPS boot in the later part. The micro SD card stores the following data:

- Second-Stage Boot Loader(SSBL)
- Kernel Image and Device Tree Blob(DTB)
- Operating System

The factory SoC boot process of Apollo Agilex is summarized as follows:

When the Apollo Agilex board is powered on, the SDM will read the configuration firmware and complete SDM initial form the QSPI flash according to the MSEL pin setting. Then, the SDM will configure the FPGA I/O and core (full configuration).

After the FPGA is first configured, SDM continues to load the FSBL(First-Stage Boot Loader) from the QSPI flash and transfer it to the HPS on-chip RAM, and releases the HPS reset to let the HPS start using the FSBL hardware handoff file to setup the clocks, HPS dedicated I/Os, and peripherals.

The FSBL then loads the SSBL(Second-Stage Boot Loader) from the Micro SD Card into HPS SDRAM and passes the control to the SSBL. The SSBL enables more advanced peripherals and loads OS into SDRAM.

Finally, the OS boots and applications are scheduled for runtime launch.

■ JTAG Programming

The JTAG interface of the Apollo Agilex is mainly implemented by the USB Blaster II circuit on the board. For programming by on-board USB Blaster II, the following procedures show how to download a configuration bit stream into the Agilex SoC FPGA:

- Make sure that power is provided to the FPGA board
- Connect your PC to the FPGA board using a micro-USB cable and make sure the USB Blaster II driver is installed on the PC.
- Launch Quartus Prime programmer and make sure the USB Blaster II is detected.
- In Quartus Prime Programmer, add the configuration bit stream file (.sof), check the associated “Program/Configure” item, and click “Start” to start FPGA programming.

2.2 Setup and Status Components

This section will introduce the use of the switch for setup on the Apollo Agilex board, as well as a description of the various status LEDs.

■ Status LED

The FPGA development board includes board-specific status LEDs to indicate board status. Please refer to **Table 2-1** for the description of the LED indicators. **Figure 2-4** shows the location of all these status LED.

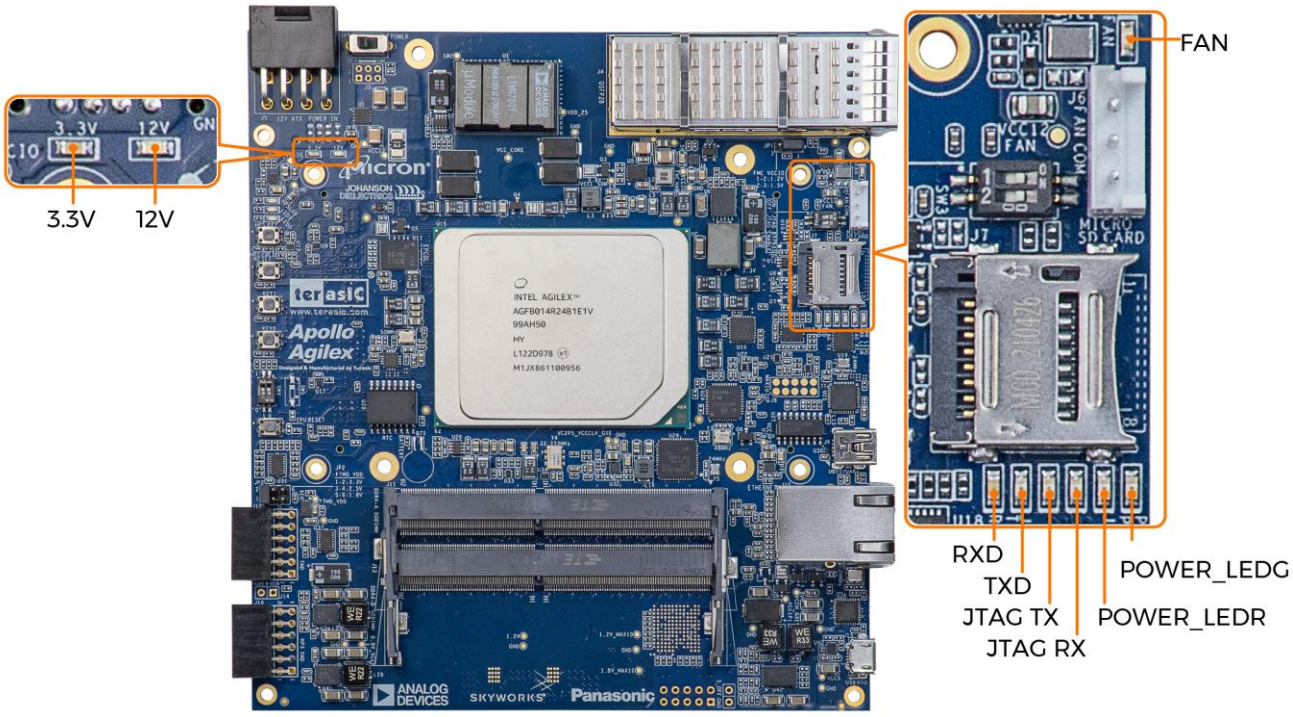

Figure 2-4 Position of the status LED

Table 2-1 Status LED

Board Reference	LED Name	Description
D4	FAN(FAN_ALERT)	Illuminates when the fan is abnormal, such as when the fan speed is different from expected
D2	12V(12-V Power)	Illuminates when 12-V power is active.
D1	3.3V(3.3-V Power)	Illuminates when 3.3-V power is active.

TXD	UART_TXLED	Illuminates when the UART interface is transmitting data
RXD	UART_RXLED	Illuminates when the UART interface is receiving data
D8	JTAG_TX	Illuminates when the USB Blaster II circuit is transmitting data
D9	JTAG_RX	Illuminates when the USB Blaster II circuit is receiving data
D11	POWER_LEDG	Illuminates when the 3.3V power good and power sequence process finished.
D10	POWER_LEDR	1. Illuminates when the 3.3V power abnormal or power sequence process failed. 2. LED will blink when the following situations occur: (i) the FPGA temperature on the board temperature exceeds 95 degrees. (ii) the power consumption exceeds 160W. (iii) when the current of VCC_CORE exceeds 100A. Also, all the power of the FPGA will be cut off when this LED is blinking.

■ JTAG Interface Switch

The JTAG interface switch **SW3** is to set whether the JTAG interface of the FMC and FMC + connector is connected to the JTAG chain in the Apollo Agilex board. Both the FMC+ and FMC connectors will **not** be included in the JTAG chain if the switches are set to **ON** position (See **Figure 2-5**).**Table 2-2** lists the setting of the SW3. Note, if the user turns any of the position on SW3 to the OFF position, but does not connect the JTAG device on the FMC or FMC+ connector. The JTAG chain on the Apollo Agilex board will not be able to form a closed loop and Quartus will not be able to detect the FPGA device.

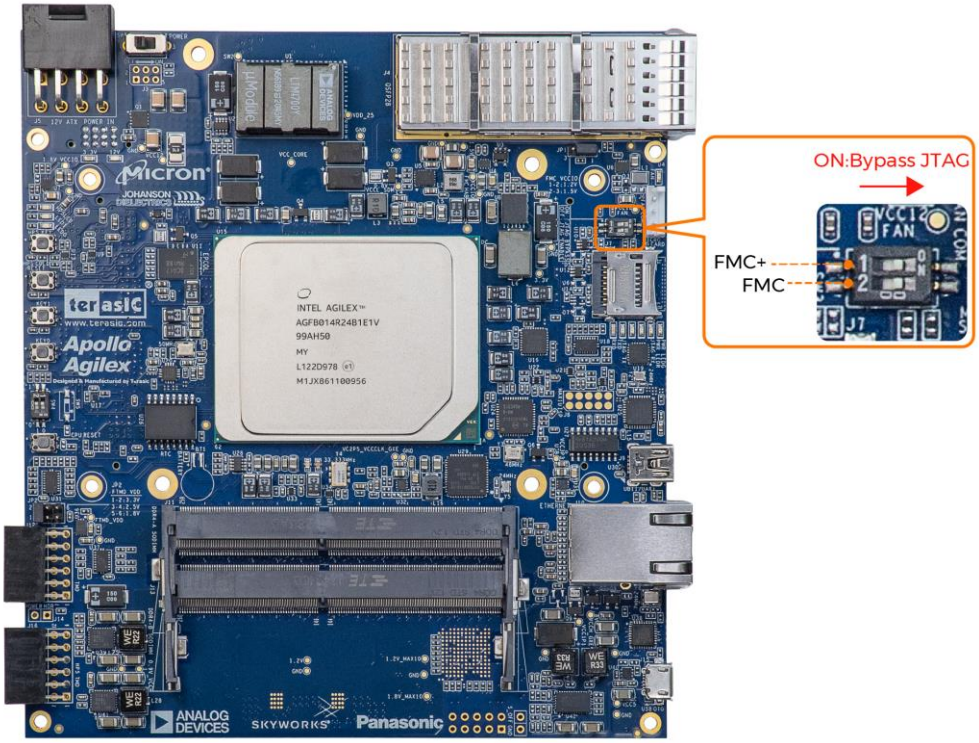

Figure 2-5 Position of slide switches SW3

Table 2-2 SW4 setting

Board Reference	Signal Name	Description	Default
SW3.1	FMCP_JTAG_BYPASS_n	**ON** : **Disable** the JTAG interface of the **FMC+** connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the **FMC+** connector into the JTAG chain	ON
SW3.2	FMC_JTAG_BYPASS_n	**ON** : **Disable** the JTAG interface of the **FMC** connector into the JTAG chain **OFF**: **Enable** the JTAG interface of the **FMC** connector into the JTAG chain	ON

■ FMC_VCCIO Select Header

Some of the FPGA pin's I/O standard connected with the HPC (High Pin Count) part of

the **FMC connector** can be set to voltages: 1.5V and 1.2V (See **Figure 2-6** and **Table 2-3**). This function can be achieved because the VCCIO power pin of the FPGA bank where these FPGA I/Os are located can adjust the input voltage through the 3 pin header (JP1). **Figure 2-7** shows the position of the JP1. **Table 2-4** list the setting for the JP1, user can short 2 pins of the header to modify the voltage level of the FMC_VCCIO_HAB.

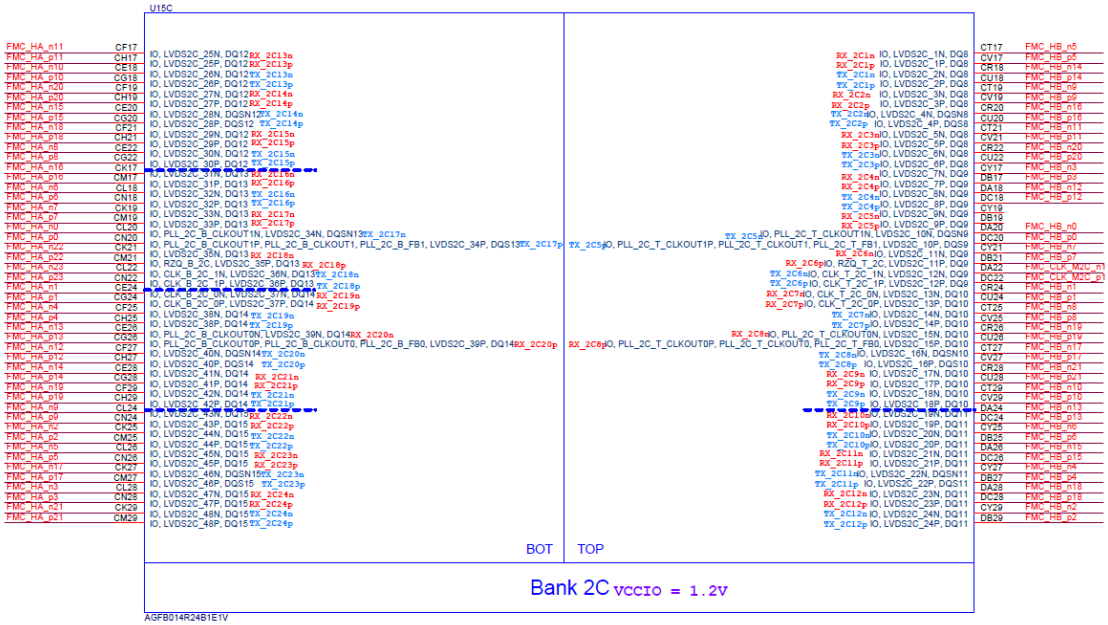

Figure 2-6 HPC FMC pin to the FPGA Bank 2C

Table 2-3 FPGA I/Os on the FMC connector which can be changed I/O standard to 1.2 or 1.5V

FMC Pins which can modify I/O stadnard
FMC_HA_p[23..0]
FMC_HA_n[23..0]
FMC_HB_p[21..0]
FMC_HB_p[21..0]
FMC_HB_n[21..0]
FMC_CLK_M2C_p[1..0]
FMC_CLK_M2C_n[1..0]

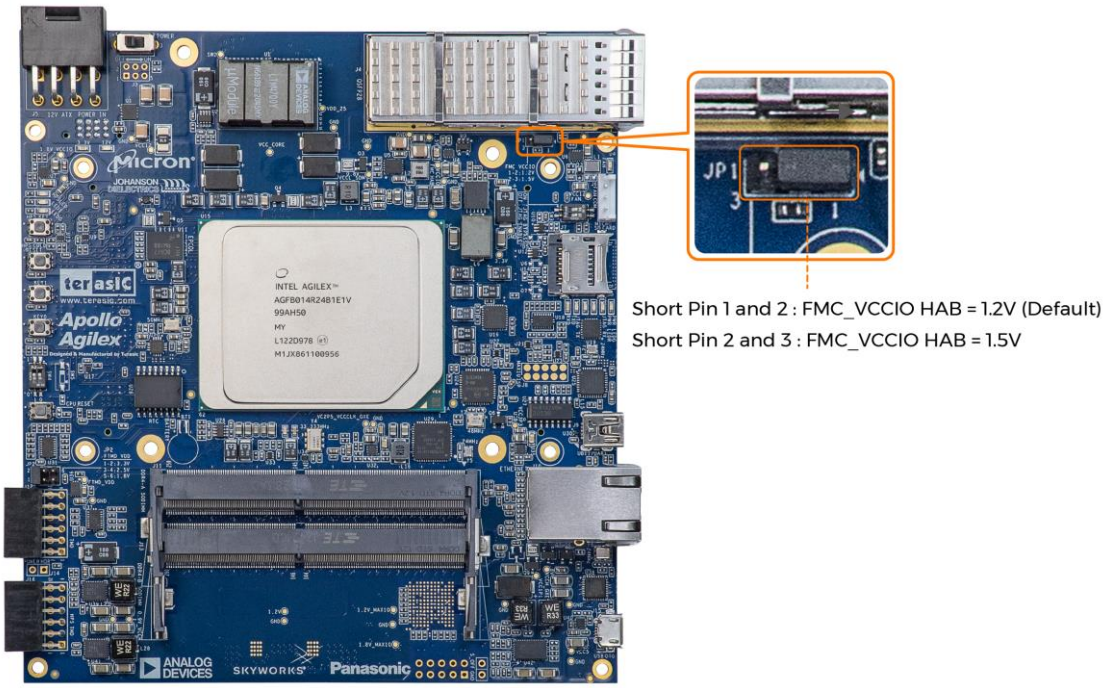

Figure 2-7 FMC and FMC+ I/O standard setting headers

Table 2-4 JP3 Setting for FMC+ I/O standard

JP3 Setting	FMC I/O Standard
	1.2V (Default)
	1.5V

2.3 General User I/O

This section describes the user I/O interface of the FPGA and HPS fabric. Please note that the HPS and FPGA portions of the device each have their own pins. Pins are not freely shared between the HPS and the FPGA fabric.

■ User Defined Push-buttons

The FPGA board includes two FPGA and one HPS fabric user defined push-buttons that allow users to interact with the Agilex SoC device. Each push-button provides a high logic level or a low logic level when it is not pressed or pressed, respectively. **Table 2-5** lists the board references, signal names and their corresponding Agilex SoC device pin numbers for the push-buttons of the FPGA fabric. **Table 2-6** list the information of the push-button for the HPS fabric.

Table 2-5 Push-button (FPGA) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
PB0	BUTTON0	High Logic Level when the button is not pressed	1.2 V	PIN_ W54
PB1	BUTTON1		1.2 V	PIN_ U54
PB4	CPU_RESET_n		1.2 V	PIN_ U56

Table 2-6 Push-button (HPS fabric) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
PB3	HPS_KEY	High Logic Level when the button is not pressed	1.8-V	PIN_H1

■ User-Defined Dip Switch

There are two positions dip switch (**SW4**) on the FPGA fabric to provide additional FPGA input control. When a position of dip switch is in the DOWN position or the UPPER position, it provides a low logic level or a high logic level to the Agilex SoC FPGA, respectively.

Table 2-7 lists the signal names and their corresponding Agilex SoC device pin numbers.

Table 2-7 Dip Switch Pin Assignments, Schematic Signal Names, and Functions

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number

SW0	SW0	High logic level when SW in the UPPER position.	1.2 V	PIN_V51
SW1	SW1		1.2 V	PIN_T51

■ User-Defined LEDs

The FPGA board consists of 2 FPGA fabric and 1 HPS fabric user-controllable LEDs to allow status and debugging signals to be driven to the LEDs from the designs loaded into the Agilex SoC FPGA. Each LED is driven directly by the FPGA. The LED is turned on or off when the associated pins are driven to a low or high logic level, respectively. A list of the pin names on the FPGA that are connected to the LEDs is given in **Table 2-8**. **Table 2-9** list the information of the LED for the HPS fabric.

Table 2-8 User LEDs (FPGA fabric) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
LED0	LED0	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.2 V	PIN_CU52
LED1	LED1		1.2 V	PIN_CR52

Table 2-9 User LEDs (HPS fabric) Pin Assignments, Schematic Signal Names

Board Reference	Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_LED	HPS_LED	Driving a logic 0 on the I/O port turns the LED ON. Driving a logic 1 on the I/O port turns the LED OFF.	1.8-V	PIN_AC6

2.4 Micro SD Card Socket

The board supports Micro SD card interface with x4 data lines. It serves for an external storage for the HPS fabric. Figure 2-8 shows signals connected between the HPS and Micro SD card socket. **Table 2-10** lists the pin assignment of Micro SD card socket to

the HPS.

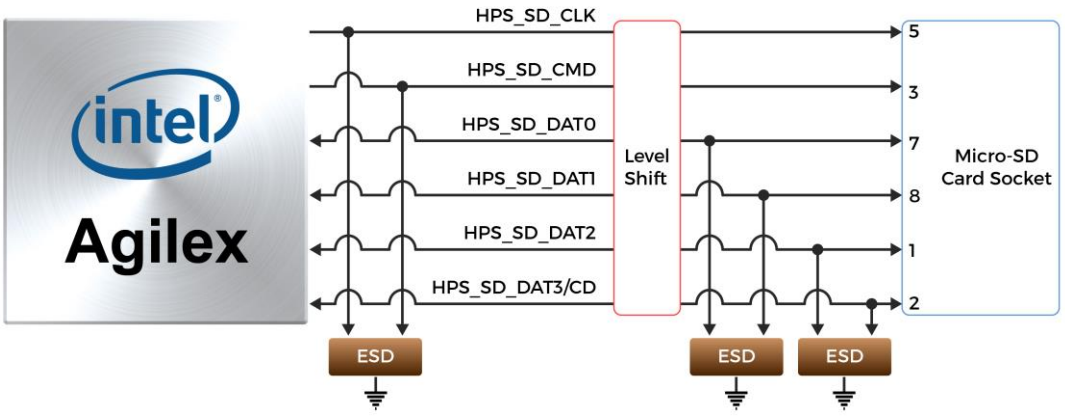

Figure 2-8 Pin-out of Micro SD Card socket

Table 2-10 Micro SD Card Socket Header Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
HPS_SD_CLK	HPS SD Clock	1.8-V	PIN_AB9
HPS_SD_CMD	HPS SD Command Line	1.8-V	PIN_V3
HPS_SD_DATA[0]	HPS SD Data[0]	1.8-V	PIN_AD9
HPS_SD_DATA[1]	HPS SD Data[1]	1.8-V	PIN_T3
HPS_SD_DATA[2]	HPS SD Data[2]	1.8-V	PIN_AC10
HPS_SD_DATA[3]	HPS SD Data[3]	1.8-V	PIN_P3

2.5 FMC Connector

The FPGA Mezzanine Card (FMC) interface provides a mechanism to extend the peripheral-set of an FPGA host board by means of add-on daughter cards, which can address today's high-speed signaling requirements as well as low-speed device interface support. The FMC interfaces support JTAG, clock outputs and inputs, high-speed serial I/O (transceivers), and single-ended or differential signaling.

There is one FMC connector on the Apollo Agilex board, it is a **High Pin Count (HPC)** size of connector, The HPC connector on Apollo Agilex board can provides 169 user-define, single-ended signals (80 pair differential I/O) and 10 serial transceiver pairs. **Figure 2-9** is the FPGA I/O connected to the FMC connector on the Apollo Agilex

board.

Below we will introduce according to the individual functions of FMC connector.

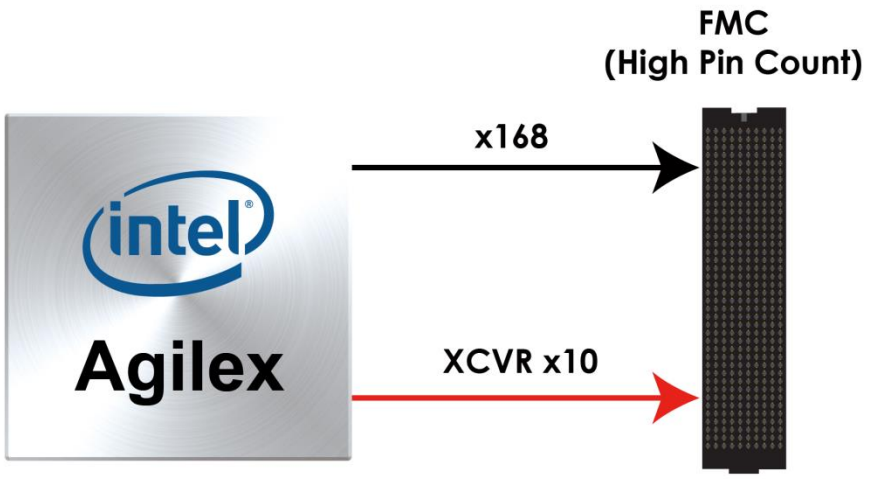

Figure 2-9 FMC connector on Apollo Agilex board

- **Clock Interface**

Table 2-11 shows the FPGA clock interface pin placement on the FMC connector.

Table 2-11 FMC clock input interface distribution

Signal Name	FMC Clock input pin name	FPGA Clock Input Pin Placement	FPGA Pin Assignment
FMC_CLK_M2C_p0	CLK0_M2C_P	CLK_B_2D_0P	CG10
FMC_CLK_M2C_n0	CLK0_M2C_N	CLK_B_2D_0N	CE10
FMC_CLK_M2C_p1	CLK1_M2C_P	CLK_T_2C_1P	DA22
FMC_CLK_M2C_n1	CLK1_M2C_N	CLK_T_2C_1N	DC22
FMC_HA_p1	HA01_P_CC	CLK_B_2C_0P	CG24
FMC_HA_n1	HA01_N_CC	CLK_B_2C_0N	CE24
FMC_HA_p23	HA23_P	CLK_B_2C_1P	CN22
FMC_HA_p23	HA23_N	CLK_B_2C_1P	CL22
FMC_HB_p1	HB01_P	CLK_T_2C_0P	CU24
FMC_HB_n1	HB01_N	CLK_T_2C_0N	CR24
FMC_LA_p0	LA00_P_CC	CLK_T_2D_0P	CU10
FMC_LA_n0	LA00_N_CC	CLK_T_2D_0N	CR10

■ Power Supply

The Apollo Agilex board provides 12V, 3.3V and 1.2V(VADJ) power through FMC ports. **Table 2-12** indicates the maximum power consumption for the FMC connector.

CAUTION: Before powering on the Apollo Agilex board with a daughter card, please check to see if there is a short circuit between the power pins and FPGA I/O.

Table 2-12 Power Supply of the FMC

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	3A
1.2V(VADJ)	4A

■ JTAG Chain on FMC

The JTAG chain on the Apollo Agilex board supports JTAG interface extension to the FMC connector so that the JTAG device on the user's FMC daughter card can be joined with JTAG chain on the Apollo Agilex board. Users can enable this feature through the switch (**SW3.2**) on the Apollo Agilex board. In the board's default setting, the JTAG interface of the FMC connector is bypassed to keep the Apollo Agilex board JTAG chain to maintain close loop. For detailed setting, please refer to ***Section 2.2: JTAG Interface Switch***.

■ Adjustable I/O Standards

Some of the FPGA pin's I/O standard connected with the HPC (High Pin Count) part of the FMC connector can be set to voltages: 1.5V and 1.2V. This function can be achieved because the VCCIO power pin of the FPGA bank where these FPGA I/Os are located can adjust the input voltage through the 3 pin header (**JP1**). For detailed setting, please refer to Section 2.2: **FMC_VCCIO Select Header**.

■ Transceiver Channels Speed

There are 10 E-Tile transceivers connected to the Agilex SoC FPGA on the FMC

connector and the maximum transmission speed is **16 G bps**. For details, please to see "E-Tile Transceiver PHY Overview".

■ Component Information of the FMC Connector

For information on the FMC part number used on the Apollo Agilex board and the male connector connected to it, refer to **Table 1-1** in the section 1.6.

■ FPGA Pin Assignments for FMC Connector

Figure 2-10 shows the pin out table of the FMC connector on the Apollo Agilex and **Table 2-13** lists the FMC connector pin assignments, signal names and functions.

	K	J	H	G	F	E	D	C	B	A
1	FMC_VREFB	GND	FMC_VREFA	GND	M2C_PG	GND	C2M_PG	GND	NC	GND
2	GND	CLK3_BIDIR_P	NC	CLK_M2C_P1	GND	HA_P1	GND	DP_C2M_P0	GND	DP_M2C_P1
3	GND	CLK3_BIDIR_N	GND	CLK_M2C_N1	GND	HA_N1	GND	DP_C2M_N0	GND	DP_M2C_N1
4	CLK2_BIDIR_P	GND	CLK_M2C_P0	GND	HA_P0	GND	GBTCLK_M2C_P0	GND	DP_M2C_P9	GND
5	CLK2_BIDIR_N	GND	CLK_M2C_N0	GND	HA_N0	GND	GBTCLK_M2C_N0	GND	DP_M2C_N9	GND
6	GND	HA_P3	GND	LA_P0	GND	HA_P5	GND	DP_M2C_P0	GND	DP_M2C_P2
7	HA_P2	HA_N3	LA_P2	LA_N0	HA_P4	HA_N5	GND	DP_M2C_N0	GND	DP_M2C_N2
8	HA_N2	GND	LA_N2	GND	HA_N4	GND	LA_P1	GND	DP_M2C_P8	GND
9	GND	HA_P7	GND	LA_P3	GND	HA_P9	LA_N1	GND	DP_M2C_N8	GND
10	HA_P6	HA_N7	LA_P4	LA_N3	HA_P8	HA_N9	GND	LA_P6	GND	DP_M2C_P3
11	HA_N6	GND	LA_N4	GND	HA_N8	GND	LA_P5	LA_N6	GND	DP_M2C_N3
12	GND	HA_P11	GND	LA_P8	GND	HA_P13	LA_N5	GND	DP_M2C_P7	GND
13	HA_P10	HA_N11	LA_P7	LA_N8	HA_P12	HA_N13	GND	GND	DP_M2C_N7	GND
14	HA_N10	GND	LA_N7	GND	HA_N12	GND	LA_P9	LA_P10	GND	DP_M2C_P4
15	GND	HA_P14	GND	LA_P12	GND	HA_P16	LA_N9	LA_N10	GND	DP_M2C_N4
16	HA_P17	HA_N14	LA_P11	LA_N12	HA_P15	HA_N16	GND	GND	DP_M2C_P6	GND
17	HA_N17	GND	LA_N11	GND	HA_N15	GND	LA_P13	GND	DP_M2C_N6	GND
18	GND	HA_P18	GND	LA_P16	GND	HA_P20	LA_N13	LA_P14	GND	DP_M2C_P5
19	HA_P21	HA_N18	LA_P15	LA_N16	HA_P19	HA_N20	GND	LA_N14	GND	DP_M2C_N5
20	HA_N21	GND	LA_N15	GND	HA_N19	GND	LA_P17	GND	GBTCLK_M2C_P1	GND
21	GND	HA_P22	GND	LA_P20	GND	HB_P3	LA_N17	GND	GBTCLK_M2C_N1	GND
22	HA_P23	HA_N22	LA_P19	LA_N20	HB_P2	HB_N3	GND	LA_P18	GND	DP_C2M_P1
23	HA_N23	GND	LA_N19	GND	HB_N2	GND	LA_P23	LA_N18	GND	DP_C2M_N1
24	GND	HB_P1	GND	LA_P22	GND	HB_P5	LA_N23	GND	DP_C2M_P9	GND
25	HB_P0	HB_N1	LA_P21	LA_N22	HB_P4	HB_N5	GND	GND	DP_C2M_N9	GND
26	HB_N0	GND	LA_N21	GND	HB_N4	GND	LA_P26	LA_P27	GND	DP_C2M_P2
27	GND	HB_P7	GND	LA_P25	GND	HB_P9	LA_N26	LA_N27	GND	DP_C2M_N2
28	HB_P6	HB_N7	LA_P24	LA_N25	HB_P8	HB_N9	GND	GND	DP_C2M_P8	GND
29	HB_N6	GND	LA_N24	GND	HB_N8	GND	JTAG_TCK	GND	DP_C2M_N8	GND
30	GND	HB_P11	GND	LA_P29	GND	HB_P13	JTAG_TDI	SCL	GND	DP_C2M_P3
31	HB_P10	HB_N11	LA_P28	LA_N29	HB_P12	HB_N13	JTAG_TDO	SDA	GND	DP_C2M_N3
32	HB_N10	GND	LA_N28	GND	HB_N12	GND	VCC3P3	GND	DP_C2M_P7	GND
33	GND	HB_P15	GND	LA_P31	GND	HB_P19	JTAG_TMS	GND	DP_C2M_N7	GND
34	HB_P14	HB_N15	LA_P30	LA_N31	HB_P16	HB_N19	JTAG_TRST	GA0	GND	DP_C2M_P4
35	HB_N14	GND	LA_N30	GND	HB_N16	GND	GA1	VCC12	GND	DP_C2M_N4
36	GND	HB_P18	GND	LA_P33	GND	HB_P21	VCC3P3	GND	DP_C2M_P6	GND
37	HB_P17	HB_N18	LA_P32	LA_N33	HB_P20	HB_N21	GND	VCC12	DP_C2M_N6	GND
38	HB_N17	GND	LA_N32	GND	HB_N20	GND	VCC3P3	GND	GND	DP_C2M_P5
39	GND	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	DP_C2M_N5
40	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	NC	GND

Figure 2-10 FMC pin out table

Table 2-13 FMC Connector Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard

FMC_CLK2_BIDIR_p	PIN_CM15	FMC data bus	1.2V
FMC_CLK2_BIDIR_n	PIN_CK15	FMC data bus	1.2V
FMC_CLK3_BIDIR_p	PIN_CM11	FMC data bus	1.2V
FMC_CLK3_BIDIR_n	PIN_CK11	FMC data bus	1.2V
FMC_CLK_M2C_p[0] *(3)	PIN_CG10	Clock from mezzanine module to carrier card positive 0	1.2V or 1.5V*(1)
FMC_CLK_M2C_n[0] *(3)	PIN_CE10	Clock from mezzanine module to carrier card negative 0	1.2V or 1.5V*(1)
FMC_CLK_M2C_p[1] *(3)	PIN_DC22	Clock from mezzanine module to carrier card positive 1	1.2V or 1.5V*(1)
FMC_CLK_M2C_n[1] *(3)	PIN_DA22	Clock from mezzanine module to carrier card negative 1	1.2V or 1.5V*(1)
FMC_HA_p[0]	PIN_CN20	FMC HA bank data p0	1.2V or 1.5V*(1)
FMC_HA_p[1] *(3)	PIN_CG24	FMC HA bank data p1	1.2V or 1.5V*(1)
FMC_HA_p[2]	PIN_CM25	FMC HA bank data p2	1.2V or 1.5V*(1)
FMC_HA_p[3]	PIN_CN28	FMC HA bank data p3	1.2V or 1.5V*(1)
FMC_HA_p[4]	PIN_CH25	FMC HA bank data p4	1.2V or 1.5V*(1)
FMC_HA_p[5]	PIN_CN26	FMC HA bank data p5	1.2V or 1.5V*(1)
FMC_HA_p[6]	PIN_CN18	FMC HA bank data p6	1.2V or 1.5V*(1)
FMC_HA_p[7]	PIN_CM19	FMC HA bank data p7	1.2V or 1.5V*(1)
FMC_HA_p[8]	PIN_CG22	FMC HA bank data p8	1.2V or 1.5V*(1)
FMC_HA_p[9]	PIN_CN24	FMC HA bank data p9	1.2V or 1.5V*(1)
FMC_HA_p[10]	PIN_CG18	FMC HA bank data p10	1.2V or 1.5V*(1)
FMC_HA_p[11]	PIN_CH17	FMC HA bank data p11	1.2V or 1.5V*(1)
FMC_HA_p[12]	PIN_CH27	FMC HA bank data p12	1.2V or 1.5V*(1)
FMC_HA_p[13]	PIN_CG26	FMC HA bank data p13	1.2V or 1.5V*(1)

FMC_HA_p[14]	PIN_CG28	FMC HA bank data p14	1.2V or 1.5V*(1)
FMC_HA_p[15]	PIN_CG20	FMC HA bank data p15	1.2V or 1.5V*(1)
FMC_HA_p[16]	PIN_CM17	FMC HA bank data p16	1.2V or 1.5V*(1)
FMC_HA_p[17]	PIN_CM27	FMC HA bank data p17	1.2V or 1.5V*(1)
FMC_HA_p[18]	PIN_CH21	FMC HA bank data p18	1.2V or 1.5V*(1)
FMC_HA_p[19]	PIN_CH29	FMC HA bank data p19	1.2V or 1.5V*(1)
FMC_HA_p[20]	PIN_CH19	FMC HA bank data p20	1.2V or 1.5V*(1)
FMC_HA_p[21]	PIN_CM29	FMC HA bank data p21	1.2V or 1.5V*(1)
FMC_HA_p[22]	PIN_CM21	FMC HA bank data p22	1.2V or 1.5V*(1)
FMC_HA_p[23] *(3)	PIN_CN22	FMC HA bank data p23	1.2V or 1.5V*(1)
FMC_HA_n[0]	PIN_CL20	FMC HA bank data n0	1.2V or 1.5V*(1)
FMC_HA_n[1] *(3)	PIN_CE24	FMC HA bank data n1	1.2V or 1.5V*(1)
FMC_HA_n[2]	PIN_CK25	FMC HA bank data n2	1.2V or 1.5V*(1)
FMC_HA_n[3]	PIN_CL28	FMC HA bank data n3	1.2V or 1.5V*(1)
FMC_HA_n[4]	PIN_CF25	FMC HA bank data n4	1.2V or 1.5V*(1)
FMC_HA_n[5]	PIN_CL26	FMC HA bank data n5	1.2V or 1.5V*(1)
FMC_HA_n[6]	PIN_CL18	FMC HA bank data n6	1.2V or 1.5V*(1)
FMC_HA_n[7]	PIN_CK19	FMC HA bank data n7	1.2V or 1.5V*(1)
FMC_HA_n[8]	PIN_CE22	FMC HA bank data n8	1.2V or 1.5V*(1)
FMC_HA_n[9]	PIN_CL24	FMC HA bank data n9	1.2V or 1.5V*(1)
FMC_HA_n[10]	PIN_CE18	FMC HA bank data n10	1.2V or 1.5V*(1)
FMC_HA_n[11]	PIN_CF17	FMC HA bank data n11	1.2V or 1.5V*(1)
FMC_HA_n[12]	PIN_CF27	FMC HA bank data n12	1.2V or 1.5V*(1)
FMC_HA_n[13]	PIN_CE26	FMC HA bank data n13	1.2V or 1.5V*(1)
FMC_HA_n[14]	PIN_CE28	FMC HA bank data n14	1.2V or 1.5V*(1)
FMC_HA_n[15]	PIN_CE20	FMC HA bank data n15	1.2V or 1.5V*(1)
FMC_HA_n[16]	PIN_CK17	FMC HA bank data n16	1.2V or 1.5V*(1)
FMC_HA_n[17]	PIN_CK27	FMC HA bank data n17	1.2V or 1.5V*(1)

FMC_HA_n[18]	PIN_CF21	FMC HA bank data n18	1.2V or 1.5V*(1)
FMC_HA_n[19]	PIN_CF29	FMC HA bank data n19	1.2V or 1.5V*(1)
FMC_HA_n[20]	PIN_CF19	FMC HA bank data n20	1.2V or 1.5V*(1)
FMC_HA_n[21]	PIN_CK29	FMC HA bank data n21	1.2V or 1.5V*(1)
FMC_HA_n[22]	PIN_CK21	FMC HA bank data n22	1.2V or 1.5V*(1)
FMC_HA_n[23] *(3)	PIN_CL22	FMC HA bank data n23	1.2V or 1.5V*(1)
FMC_HB_p[0]	PIN_DC20	FMC HB bank data p0	1.2V or 1.5V*(1)
FMC_HB_p[1]	PIN_CU24	FMC HB bank data p1	1.2V or 1.5V*(1)
FMC_HB_p[2]	PIN_DB29	FMC HB bank data p2	1.2V or 1.5V*(1)
FMC_HB_p[3]	PIN_DB17	FMC HB bank data p3	1.2V or 1.5V*(1)
FMC_HB_p[4]	PIN_DB27	FMC HB bank data p4	1.2V or 1.5V*(1)
FMC_HB_p[5]	PIN_CV17	FMC HB bank data p5	1.2V or 1.5V*(1)
FMC_HB_p[6]	PIN_DB25	FMC HB bank data p6	1.2V or 1.5V*(1)
FMC_HB_p[7]	PIN_DB21	FMC HB bank data p7	1.2V or 1.5V*(1)
FMC_HB_p[8]	PIN_CV25	FMC HB bank data p8	1.2V or 1.5V*(1)
FMC_HB_p[9]	PIN_CV19	FMC HB bank data p9	1.2V or 1.5V*(1)
FMC_HB_p[10]	PIN_CV29	FMC HB bank data p10	1.2V or 1.5V*(1)
FMC_HB_p[11]	PIN_CV21	FMC HB bank data p11	1.2V or 1.5V*(1)
FMC_HB_p[12]	PIN_DC18	FMC HB bank data p12	1.2V or 1.5V*(1)
FMC_HB_p[13]	PIN_DC24	FMC HB bank data p13	1.2V or 1.5V*(1)
FMC_HB_p[14]	PIN_CU18	FMC HB bank data p14	1.2V or 1.5V*(1)
FMC_HB_p[15]	PIN_DC26	FMC HB bank data p15	1.2V or 1.5V*(1)
FMC_HB_p[16]	PIN_CU20	FMC HB bank data p16	1.2V or 1.5V*(1)
FMC_HB_p[17]	PIN_CV27	FMC HB bank data p17	1.2V or 1.5V*(1)
FMC_HB_p[18]	PIN_DC28	FMC HB bank data p18	1.2V or 1.5V*(1)
FMC_HB_p[19]	PIN_CU26	FMC HB bank data p19	1.2V or 1.5V*(1)
FMC_HB_p[20]	PIN_CU22	FMC HB bank data p20	1.2V or 1.5V*(1)
FMC_HB_p[21]	PIN_CU28	FMC HB bank data p21	1.2V or 1.5V*(1)

FMC_HB_n[0]	PIN_DA20	FMC HB bank data n0	1.2V or 1.5V*(1)
FMC_HB_n[1]	PIN_CR24	FMC HB bank data n1	1.2V or 1.5V*(1)
FMC_HB_n[2]	PIN_CY29	FMC HB bank data n2	1.2V or 1.5V*(1)
FMC_HB_n[3]	PIN_CY17	FMC HB bank data n3	1.2V or 1.5V*(1)
FMC_HB_n[4]	PIN_CY27	FMC HB bank data n4	1.2V or 1.5V*(1)
FMC_HB_n[5]	PIN_CT17	FMC HB bank data n5	1.2V or 1.5V*(1)
FMC_HB_n[6]	PIN_CY25	FMC HB bank data n6	1.2V or 1.5V*(1)
FMC_HB_n[7]	PIN_CY21	FMC HB bank data n7	1.2V or 1.5V*(1)
FMC_HB_n[8]	PIN_CT25	FMC HB bank data n8	1.2V or 1.5V*(1)
FMC_HB_n[9]	PIN_CT19	FMC HB bank data n9	1.2V or 1.5V*(1)
FMC_HB_n[10]	PIN_CT29	FMC HB bank data n10	1.2V or 1.5V*(1)
FMC_HB_n[11]	PIN_CT21	FMC HB bank data n11	1.2V or 1.5V*(1)
FMC_HB_n[12]	PIN_DA18	FMC HB bank data n12	1.2V or 1.5V*(1)
FMC_HB_n[13]	PIN_DA24	FMC HB bank data n13	1.2V or 1.5V*(1)
FMC_HB_n[14]	PIN_CR18	FMC HB bank data n14	1.2V or 1.5V*(1)
FMC_HB_n[15]	PIN_DA26	FMC HB bank data n15	1.2V or 1.5V*(1)
FMC_HB_n[16]	PIN_CR20	FMC HB bank data n16	1.2V or 1.5V*(1)
FMC_HB_n[17]	PIN_CT27	FMC HB bank data n17	1.2V or 1.5V*(1)
FMC_HB_n[18]	PIN_DA28	FMC HB bank data n18	1.2V or 1.5V*(1)
FMC_HB_n[19]	PIN_CR26	FMC HB bank data n19	1.2V or 1.5V*(1)
FMC_HB_n[20]	PIN_CR22	FMC HB bank data n20	1.2V or 1.5V*(1)
FMC_HB_n[21]	PIN_CR28	FMC HB bank data n21	1.2V or 1.5V*(1)
FMC_LA_p[0] *(3)	PIN_CU10	FMC LA bank data p0	1.2V
FMC_LA_p[1]	PIN_DC6	FMC LA bank data p1	1.2V
FMC_LA_p[2]	PIN_CV13	FMC LA bank data p2	1.2V
FMC_LA_p[3]	PIN_DC10	FMC LA bank data p3	1.2V
FMC_LA_p[4]	PIN_CU6	FMC LA bank data p4	1.2V
FMC_LA_p[5]	PIN_DB11	FMC LA bank data p5	1.2V

FMC_LA_p[6]	PIN_CU14	FMC LA bank data p6	1.2V
FMC_LA_p[7]	PIN_DB13	FMC LA bank data p7	1.2V
FMC_LA_p[8]	PIN_DC12	FMC LA bank data p8	1.2V
FMC_LA_p[9]	PIN_DA4	FMC LA bank data p9	1.2V
FMC_LA_p[10]	PIN_DB5	FMC LA bank data p10	1.2V
FMC_LA_p[11]	PIN_DB15	FMC LA bank data p11	1.2V
FMC_LA_p[12]	PIN_DC14	FMC LA bank data p12	1.2V
FMC_LA_p[13]	PIN_CU4	FMC LA bank data p13	1.2V
FMC_LA_p[14]	PIN_CV1	FMC LA bank data p14	1.2V
FMC_LA_p[15]	PIN_CV11	FMC LA bank data p15	1.2V
FMC_LA_p[16]	PIN_DB7	FMC LA bank data p16	1.2V
FMC_LA_p[17]	PIN_CU8	FMC LA bank data p17	1.2V
FMC_LA_p[18]	PIN_CV7	FMC LA bank data p18	1.2V
FMC_LA_p[19]	PIN_CV15	FMC LA bank data p19	1.2V
FMC_LA_p[20]	PIN_CV5	FMC LA bank data p20	1.2V
FMC_LA_p[21]	PIN_CN4	FMC LA bank data p21	1.2V
FMC_LA_p[22]	PIN_CH5	FMC LA bank data p22	1.2V
FMC_LA_p[23]	PIN_CG4	FMC LA bank data p23	1.2V
FMC_LA_p[24]	PIN_CN6	FMC LA bank data p24	1.2V
FMC_LA_p[25]	PIN_CM3	FMC LA bank data p25	1.2V
FMC_LA_p[26]	PIN_CG6	FMC LA bank data p26	1.2V
FMC_LA_p[27]	PIN_CM7	FMC LA bank data p27	1.2V
FMC_LA_p[28]	PIN_CG8	FMC LA bank data p28	1.2V
FMC_LA_p[29]	PIN_CH3	FMC LA bank data p29	1.2V
FMC_LA_p[30]	PIN_CH11	FMC LA bank data p30	1.2V
FMC_LA_p[31]	PIN_CM5	FMC LA bank data p31	1.2V
FMC_LA_p[32]	PIN_CG14	FMC LA bank data p32	1.2V
FMC_LA_p[33]	PIN_CH7	FMC LA bank data p33	1.2V

FMC_LA_n[0] *(3)	PIN_CR10	FMC LA bank data n0	1.2V
FMC_LA_n[1]	PIN_DA6	FMC LA bank data n1	1.2V
FMC_LA_n[2]	PIN_CT13	FMC LA bank data n2	1.2V
FMC_LA_n[3]	PIN_DA10	FMC LA bank data n3	1.2V
FMC_LA_n[4]	PIN_CR6	FMC LA bank data n4	1.2V
FMC_LA_n[5]	PIN_CY11	FMC LA bank data n5	1.2V
FMC_LA_n[6]	PIN_CR14	FMC LA bank data n6	1.2V
FMC_LA_n[7]	PIN_CY13	FMC LA bank data n7	1.2V
FMC_LA_n[8]	PIN_DA12	FMC LA bank data n8	1.2V
FMC_LA_n[9]	PIN_CY3	FMC LA bank data n9	1.2V
FMC_LA_n[10]	PIN_CY5	FMC LA bank data n10	1.2V
FMC_LA_n[11]	PIN_CY15	FMC LA bank data n11	1.2V
FMC_LA_n[12]	PIN_DA14	FMC LA bank data n12	1.2V
FMC_LA_n[13]	PIN_CR4	FMC LA bank data n13	1.2V
FMC_LA_n[14]	PIN_CT1	FMC LA bank data n14	1.2V
FMC_LA_n[15]	PIN_CT11	FMC LA bank data n15	1.2V
FMC_LA_n[16]	PIN_CY7	FMC LA bank data n16	1.2V
FMC_LA_n[17]	PIN_CR8	FMC LA bank data n17	1.2V
FMC_LA_n[18]	PIN_CT7	FMC LA bank data n18	1.2V
FMC_LA_n[19]	PIN_CT15	FMC LA bank data n19	1.2V
FMC_LA_n[20]	PIN_CT5	FMC LA bank data n20	1.2V
FMC_LA_n[21]	PIN_CL4	FMC LA bank data n21	1.2V
FMC_LA_n[22]	PIN_CF5	FMC LA bank data n22	1.2V
FMC_LA_n[23]	PIN_CE4	FMC LA bank data n23	1.2V
FMC_LA_n[24]	PIN_CL6	FMC LA bank data n24	1.2V
FMC_LA_n[25]	PIN_CK3	FMC LA bank data n25	1.2V
FMC_LA_n[26]	PIN_CE6	FMC LA bank data n26	1.2V
FMC_LA_n[27]	PIN_CK7	FMC LA bank data n27	1.2V

FMC_LA_n[28]	PIN_CE8	FMC LA bank data n28	1.2V
FMC_LA_n[29]	PIN_CF3	FMC LA bank data n29	1.2V
FMC_LA_n[30]	PIN_CF11	FMC LA bank data n30	1.2V
FMC_LA_n[31]	PIN_CK5	FMC LA bank data n31	1.2V
FMC_LA_n[32]	PIN_CE14	FMC LA bank data n32	1.2V
FMC_LA_n[33]	PIN_CF7	FMC LA bank data n33	1.2V
FMC_GBTCLK_M2C_p[0]	PIN_AJ14	LVDS input from the installed FMC card to dedicated reference clock inputs	DIFFERENTIAL LVPECL
FMC_GBTCLK_M2C_p[1]	PIN_AR16	LVDS input from the installed FMC card to dedicated reference clock inputs	DIFFERENTIAL LVPECL
FMC_DP_C2M_p[0]	PIN_AK1	Transmit pair p0 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[1]	PIN_AL4	Transmit pair p1 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[2]	PIN_AP1	Transmit pair p2 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[3]	PIN_AR4	Transmit pair p3 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[4]	PIN_AV1	Transmit pair p4 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[5]	PIN_AW4	Transmit pair p5 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[6]	PIN_BB1	Transmit pair p6 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[7]	PIN_BC4	Transmit pair p7 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_C2M_p[8]	PIN_BF1	Transmit pair p8 of the FPGA transceiver	High Speed Differential I/O

FMC_DP_C2M_p[9]	PIN_BG4	Transmit pair p9 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[0]	PIN_AK7	Receiver pair p0 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[1]	PIN_AL10	Receiver pair p1 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[2]	PIN_AP7	Receiver pair p2 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[3]	PIN_AR10	Receiver pair p3 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[4]	PIN_AV7	Receiver pair p4 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[5]	PIN_AW10	Receiver pair p5 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[6]	PIN_BB7	Receiver pair p6 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[7]	PIN_BC10	Receiver pair p7 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[8]	PIN_BF7	Receiver pair p8 of the FPGA transceiver	High Speed Differential I/O
FMC_DP_M2C_p[9]	PIN_BG10	Receiver pair p9 of the FPGA transceiver	High Speed Differential I/O
FMC_GA[0]	PIN_CT3	FMC geographical address 0	3.3 V*(2)
FMC_GA[1]	PIN_CV3	FMC geographical address 1	3.3 V*(2)
FMC_SCL	PIN_CL14	Management serial clock line	3.3 V*(2)
FMC_SDA	PIN_CM13	Management serial data line	3.3 V*(2)
FMC_RES[0]	PIN_CL12	Reserved	1.2 V

- *(1): The FMC_VCCIO value depends on the setting of JP2, which can adjust the FMC_VCCIO to **1.2V or 1.5V**. Please refer to section 2.2 : "*FMC_VCCIO Select Header*" for details.

- *(2): There are level shift ICs that convert FMC_VCCIO to 3.3V between the FPGA pins and the FMC pins.
- *(3): FPGA dedicated clock input pin.

2.6 FMC+ Connector

In addition to an FMC connector on the Apollo Agilex board, there is also an FMC + connector for expanding FPGA I/Os (See **Figure 2-11**). The main difference between FMC + and FMC specifications is that the number of FMC + transceiver can provide up to 24 pairs (**High Serial Pin Count version, HSPC**), but in the Apollo Agilex board it provides **16** pair transceivers.

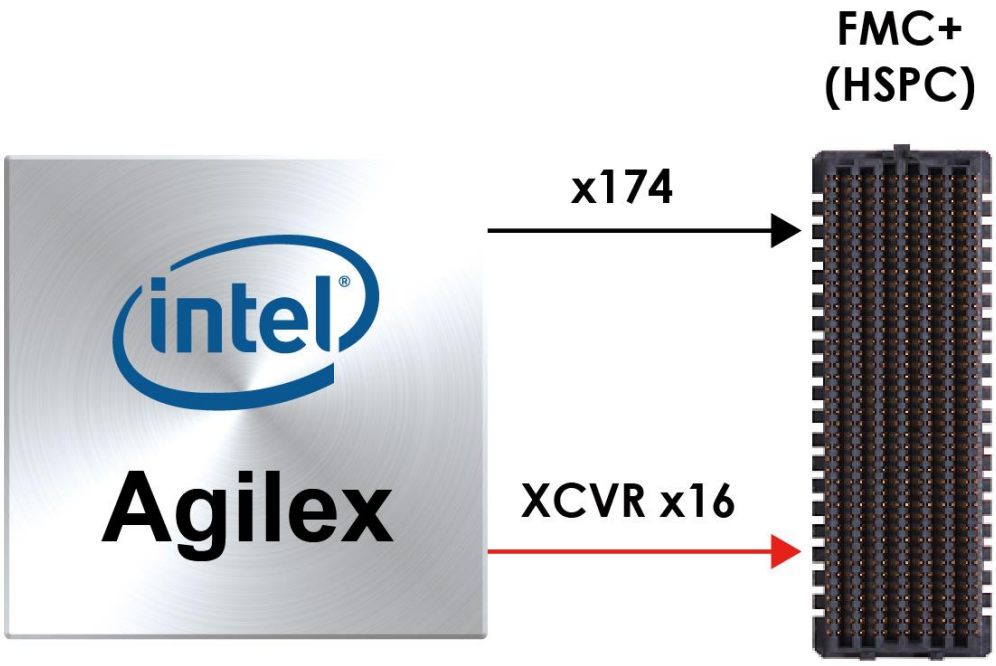

Figure 2-11 FMC+ connector on Apollo Agilex board

As the number of transceivers increases, the connector size of the FMC+ becomes a 14x40 array, compared to the 10x40 array of the FMC.

Below we will introduce according to the individual functions of FMC+ connector.

- **Clock Interface**

Table 2-14 shows the FPGA dedicated clock input pin placement on the FMC+

connector.

Table 2-14 FMCP clock input interface distribution

Signal Name	FMC Clock in/out pin name	FPGA Clock Input Pin Placement	FPGA Pin Assignment
FMCP_CLK_M2C_p0	CLK0_M2C_P	CLK_T_2A_1P	DC52
FMCP_CLK_M2C_n0	CLK0_M2C_N	CLK_T_2A_1N	DA52
FMCP_CLK_M2C_p1	CLK1_M2C_P	CLK_T_2B_1P	DC38
FMCP_CLK_M2C_n1	CLK1_M2C_N	CLK_T_2B_1N	DA38
FMCP_HA_p1	HA01_P_CC	CLK_B_2B_0P	CG36
FMCP_HA_n1	HA01_N_CC	CLK_B_2B_0N	CE36
FMCP_HA_p12	HA_P12	CLK_B_2B_1P	CN38
FMCP_HA_n12	HA_P12	CLK_B_2B_1N	CL38
FMCP_HB_p1	HB_P11	CLK_T_2B_0P	CU36
FMCP_HB_n1	HB_P11	CLK_T_2B_0P	CR36
FMCP_LA_p0	LA00_P_CC	CLK_B_2A_0P	CG50
FMCP_LA_p0	LA00_N_CC	CLK_B_2A_0N	CE50

■ Power Supply

The Apollo Agilex board provides 12V, 3.3V and 1.2V(VADJ) power through FMC+ port. **Table 2-15** indicates the maximum power consumption for the FMC+ connector.

CAUTION: Before powering on the Apollo Agilex board with a daughter card, please check to see if there is a short circuit between the power pins and FPGA I/O.

Table 2-15 Power Supply of the FMC

Supplied Voltage	Max. Current Limit
12V	1A
3.3V	3A
1.2V(VADJ)	4A

■ JTAG Chain on FMC

The JTAG chain on the Apollo Agilex board supports JTAG interface extension to the

FMC+ connector so that the JTAG device on the user's FMC+ daughter card can be joined with JTAG chain on the Apollo Agilex board. Users can enable this feature through the switch (**SW3.1**) on the Apollo Agilex board. In the board's default setting, the JTAG interface of the FMC connector is bypassed to keep the Apollo Agilex board JTAG chain to maintain close loop. For detailed setting, please refer to Section 2.2: **JTAG Interface Switch.**

■ Transceiver Channels in the FMC+ connector

There are **16 P-tiles** transceivers connected to the Agiiex SoC FPGA on the FMC+ connector. **P-tiles transceivers are designed to support the PCI Express standard (Gen3 and Gen 4)**. Users can use these P-tiles transceivers and the PCIe hard IP in the Agilex SoC FPGA to implement the PCIe Gen4 x16 applications. To achieve this feature, users will also need a PCIe Gen4 interface with FMC+ connector card (Terasic P16E-FMCP FMC+ daughter). The P16E-FMCP FMC+ daughter card allows the FPGA boards equipped with the FMC+ connector and support the PCIe interface to connect with the PC (See Figure 2-x and Figure 2-x).. Users can refer to the website of the P16E-FMCP to acquire this card.

Figure 2-12 The P16E-FMCP FMC+ daughter card

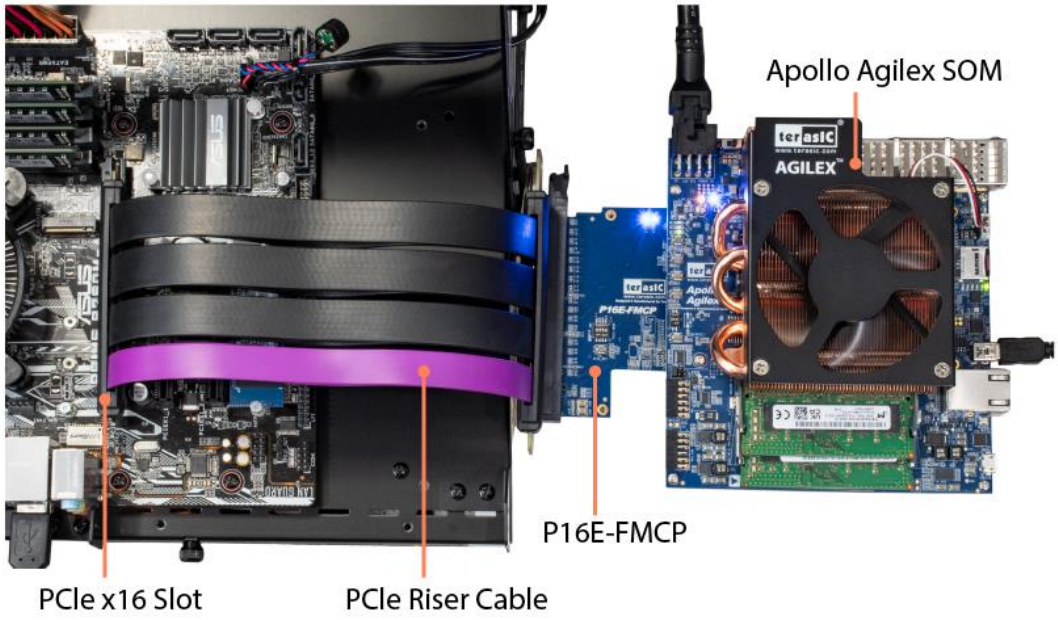

Figure 2-13 Using P16E-FMCP to establish PCIe connection between Apollo Agilex and Host PC

■ FPGA Pin Assignments for FMCP Connector

Figure 2-14 shows the pin out table of the FMC connector on the Apollo Agilex and **Table 2-16** lists the FMC connector pin assignments, signal names and function.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	RES1	FMC_VREFB	GND	FMC_VREFA	GND	M2C_PG	GND	C2M_PG	GND	GND	GND	FMCP_PRSNT_M2C_L	GND
2	NC	GND	GND	CLK3_BIDIR_P	FMCP_PRSNT_M2C_L	CLK_M2C_P1	GND	HA_P1	GND	DP_C2M_P0	GND	DP_M2C_P1	GND	NC
3	NC	GND	GND	CLK3_BIDIR_N	GND	CLK_M2C_N1	GND	HA_N1	GND	DP_C2M_N0	GND	DP_M2C_N1	GND	NC
4	GND	GBTCLK_M2C_P4	CLK2_BIDIR_P	GND	CLK_M2C_P0	GND	HA_P0	GND	GBTCLK_M2C_P0	GND	DP_M2C_P9	GND	NC	GND
5	GND	GBTCLK_M2C_N4	CLK2_BIDIR_N	GND	CLK_M2C_N0	GND	HA_N0	GND	GBTCLK_M2C_N0	GND	DP_M2C_N9	GND	NC	GND
6	NC	GND	GND	HA_P3	GND	LA_P0	GND	HA_P5	GND	DP_M2C_P0	GND	DP_M2C_P2	GND	NC
7	NC	GND	HA_P2	HA_N3	LA_P2	LA_N0	HA_P4	HA_N5	GND	DP_M2C_N0	GND	DP_M2C_N2	GND	NC
8	GND	GBTCLK_M2C_P3	HA_N2	GND	LA_N2	GND	HA_N4	GND	LA_P1	GND	DP_M2C_P8	GND	NC	GND
9	GND	GBTCLK_M2C_N3	GND	HA_P7	GND	LA_P3	GND	HA_P9	LA_N1	GND	DP_M2C_N8	GND	NC	GND
10	NC	GND	HA_P6	HA_N7	LA_P4	LA_N3	HA_P8	HA_N9	GND	LA_P6	GND	DP_M2C_P3	GND	DP_M2C_P10
11	NC	GND	HA_N6	GND	LA_N4	GND	HA_N8	GND	LA_P5	LA_N6	GND	DP_M2C_N3	GND	DP_M2C_N10
12	GND	GBTCLK_M2C_P2	GND	HA_P11	GND	LA_P8	GND	HA_P13	LA_N5	GND	DP_M2C_P7	GND	DP_M2C_P11	GND
13	GND	GBTCLK_M2C_N2	HA_P10	HA_N11	LA_P7	LA_N8	HA_P12	HA_N13	GND	GND	DP_M2C_N7	GND	DP_M2C_N11	GND
14	NC	GND	HA_N10	GND	LA_N7	GND	HA_N12	GND	LA_P9	LA_P10	GND	DP_M2C_P4	GND	DP12_M2C_P
15	NC	GND	GND	HA_P14	GND	LA_P12	GND	HA_P16	LA_N9	LA_N10	GND	DP_M2C_N4	GND	DP12_M2C_N
16	GND	SYNC_C2M_P	HA_P17	HA_N14	LA_P11	LA_N12	HA_P15	HA_N16	GND	GND	DP_M2C_P6	GND	DP13_M2C_P	GND
17	GND	SYNC_C2M_N	HA_N17	GND	LA_N11	GND	HA_N15	GND	LA_P13	GND	DP_M2C_N6	GND	DP13_M2C_N	GND
18	DP_C2M_P14	GND	GND	HA_P18	GND	LA_P16	GND	HA_P20	LA_N13	LA_P14	GND	DP_M2C_P5	GND	DP14_M2C_P
19	DP_C2M_N14	GND	HA_P21	HA_N18	LA_P15	LA_N16	HA_P19	HA_N20	GND	LA_N14	GND	DP_M2C_N5	GND	DP14_M2C_N
20	GND	REFCLK_C2M_P	HA_N21	GND	LA_N15	GND	HA_N19	GND	LA_P17	GND	GBTCLK_M2C_P1	GND	NC	GND
21	GND	REFCLK_C2M_N	GND	HA_P22	GND	LA_P20	GND	HB_P3	LA_N17	GND	GBTCLK_M2C_N1	GND	NC	GND
22	DP_C2M_P15	GND	HA_P23	HA_N22	LA_P19	LA_N20	HB_P2	HB_N3	GND	LA_P18	GND	DP_C2M_P1	GND	DP15_M2C_P
23	DP_C2M_N15	GND	HA_N23	GND	LA_N19	GND	HB_N2	GND	LA_P23	LA_N18	GND	DP_C2M_N1	GND	DP15_M2C_N
24	GND	REFCLK_M2C_P	GND	HB_P1	GND	LA_P22	GND	HB_P5	LA_N23	GND	DP_C2M_P9	GND	DP_C2M_P10	GND
25	GND	REFCLK_M2C_N	HB_P0	HB_N1	LA_P21	LA_N22	HB_P4	HB_N5	GND	GND	DP_C2M_N9	GND	DP_C2M_N10	GND
26	NC	GND	HB_N0	GND	LA_N21	GND	HB_N4	GND	LA_P26	LA_P27	GND	DP_C2M_P2	GND	DP_C2M_P11
27	NC	GND	GND	HB_P7	GND	LA_P25	GND	HB_P9	LA_N26	LA_N27	GND	DP_C2M_N2	GND	DP_C2M_N11
28	GND	SYNC_M2C_P	HB_P6	HB_N7	LA_P24	LA_N25	HB_P8	HB_N9	GND	GND	DP_C2M_P8	GND	DP_C2M_P12	GND
29	GND	SYNC_M2C_N	HB_N6	GND	LA_N24	GND	HB_N8	GND	JTAG_TCK	GND	DP_C2M_N8	GND	DP_C2M_N12	GND
30	NC	GND	GND	HB_P11	GND	LA_P29	GND	HB_P13	JTAG_TDI	SCL	GND	DP_C2M_P3	GND	DP_C2M_P13
31	NC	GND	HB_P10	HB_N11	LA_P28	LA_N29	HB_P12	HB_N13	JTAG_TDO	SDA	GND	DP_C2M_N3	GND	DP_C2M_N13
32	GND	GND	HB_N10	GND	LA_N28	GND	HB_N12	GND	VCC3P3	GND	DP_C2M_P7	GND	NC	GND
33	GND	GND	GND	HB_P15	GND	LA_P31	GND	HB_P19	JTAG_TMS	GND	DP_C2M_N7	GND	NC	GND
34	NC	GND	HB_P14	HB_N15	LA_P30	LA_N31	HB_P16	HB_N19	JTAG_TRST	GA0	GND	DP_C2M_P4	GND	NC
35	NC	GND	HB_N14	GND	LA_N30	GND	HB_N16	GND	GA1	VCC12	GND	DP_C2M_N4	GND	NC
36	GND	12P0V	GND	HB_P18	GND	LA_P33	GND	HB_P21	VCC3P3	GND	DP_C2M_P6	GND	NC	GND
37	GND	12P0V	HB_P17	HB_N18	LA_P32	LA_N33	HB_P20	HB_N21	GND	VCC12	DP_C2M_N6	GND	NC	GND
38	NC	GND	HB_N17	GND	LA_N32	GND	HB_N20	GND	VCC3P3	GND	GND	DP_C2M_P5	GND	NC
39	NC	GND	GND	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	DP_C2M_N5	GND	NC
40	GND	12P0V	NC	GND	VCCIO_FMC	GND	VCCIO_FMC	GND	VCC3P3	GND	RES0	GND	3P3V	GND

Figure 2-14 FMC+ pin out table

Table 2-16 FMCP Connector Pin Assignments, Signal Names and Functions

Signal Name	FPGA Pin Number	Description	I/O Standard
FMCP_CLK2_BIDIR_p*(1)	PIN_DC54	FMCP data bus	1.2 V
FMCP_CLK2_BIDIR_n*(1)	PIN_DA54	FMCP data bus	1.2 V
FMCP_CLK3_BIDIR_p*(1)	PIN_CU54	FMCP data bus	1.2 V
FMCP_CLK3_BIDIR_n*(1)	PIN_CR54	FMCP data bus	1.2 V
FMCP_CLK_M2C_p[0]	PIN_DC52	Clock from mezzanine module to carrier card positive 0	True Differential Signaling
FMCP_CLK_M2C_n[0]		Clock from mezzanine module to carrier card negative 0	True Differential Signaling
FMCP_CLK_M2C_p[1]	PIN_DC38	Clock from mezzanine module to carrier card positive 1	True Differential Signaling
FMCP_CLK_M2C_n[1]		Clock from mezzanine module to carrier card negative 1	True Differential Signaling
FMCP_HA_p[0]	PIN_CN40	FMCP HA bank data p0	1.2 V
FMCP_HA_p[1] *(1)	PIN_CG36	FMCP HA bank data p1	1.2 V
FMCP_HA_p[2]	PIN_CG40	FMCP HA bank data p2	1.2 V
FMCP_HA_p[3]	PIN_CG34	FMCP HA bank data p3	1.2 V
FMCP_HA_p[4]	PIN_CH35	FMCP HA bank data p4	1.2 V
FMCP_HA_p[5]	PIN_CH39	FMCP HA bank data p5	1.2 V
FMCP_HA_p[6]	PIN_CN42	FMCP HA bank data p6	1.2 V
FMCP_HA_p[7]	PIN_CH43	FMCP HA bank data p7	1.2 V
FMCP_HA_p[8]	PIN_CG42	FMCP HA bank data p8	1.2 V
FMCP_HA_p[9]	PIN_CH41	FMCP HA bank data p9	1.2 V
FMCP_HA_p[10]	PIN_CG38	FMCP HA bank data p10	1.2 V

FMCP_HA_p[11]	PIN_CM41	FMCP HA bank data p11	1.2 V
FMCP_HA_p[12] *(1)	PIN_CN38	FMCP HA bank data p12	1.2 V
FMCP_HA_p[13]	PIN_CM43	FMCP HA bank data p13	1.2 V
FMCP_HA_p[14]	PIN_CN36	FMCP HA bank data p14	1.2 V
FMCP_HA_p[15]	PIN_CM35	FMCP HA bank data p15	1.2 V
FMCP_HA_p[16]	PIN_CM39	FMCP HA bank data p16	1.2 V
FMCP_HA_p[17]	PIN_CM31	FMCP HA bank data p17	1.2 V
FMCP_HA_p[18]	PIN_CN34	FMCP HA bank data p18	1.2 V
FMCP_HA_p[19]	PIN_CM33	FMCP HA bank data p19	1.2 V
FMCP_HA_p[20]	PIN_CG32	FMCP HA bank data p20	1.2 V
FMCP_HA_p[21]	PIN_CH31	FMCP HA bank data p21	1.2 V
FMCP_HA_p[22]	PIN_CN32	FMCP HA bank data p22	1.2 V
FMCP_HA_p[23]	PIN_CH33	FMCP HA bank data p23	1.2 V
FMCP_HA_n[0]	PIN_CL40	FMCP HA bank data n0	1.2 V
FMCP_HA_n[1] *(1)	PIN_CE36	FMCP HA bank data n1	1.2 V
FMCP_HA_n[2]	PIN_CE40	FMCP HA bank data n2	1.2 V
FMCP_HA_n[3]	PIN_CE34	FMCP HA bank data n3	1.2 V
FMCP_HA_n[4]	PIN_CF35	FMCP HA bank data n4	1.2 V
FMCP_HA_n[5]	PIN_CF39	FMCP HA bank data n5	1.2 V
FMCP_HA_n[6]	PIN_CL42	FMCP HA bank data n6	1.2 V
FMCP_HA_n[7]	PIN_CF43	FMCP HA bank data n7	1.2 V
FMCP_HA_n[8]	PIN_CE42	FMCP HA bank data n8	1.2 V
FMCP_HA_n[9]	PIN_CF41	FMCP HA bank data n9	1.2 V
FMCP_HA_n[10]	PIN_CE38	FMCP HA bank data n10	1.2 V
FMCP_HA_n[11]	PIN_CK41	FMCP HA bank data n11	1.2 V
FMCP_HA_n[12] *(1)	PIN_CL38	FMCP HA bank data n12	1.2 V
FMCP_HA_n[13]	PIN_CK43	FMCP HA bank data n13	1.2 V
FMCP_HA_n[14]	PIN_CL36	FMCP HA bank data n14	1.2 V

FMCP_HA_n[15]	PIN_CK35	FMCP HA bank data n15	1.2 V
FMCP_HA_n[16]	PIN_CK39	FMCP HA bank data n16	1.2 V
FMCP_HA_n[17]	PIN_CK31	FMCP HA bank data n17	1.2 V
FMCP_HA_n[18]	PIN_CL34	FMCP HA bank data n18	1.2 V
FMCP_HA_n[19]	PIN_CK33	FMCP HA bank data n19	1.2 V
FMCP_HA_n[20]	PIN_CE32	FMCP HA bank data n20	1.2 V
FMCP_HA_n[21]	PIN_CF31	FMCP HA bank data n21	1.2 V
FMCP_HA_n[22]	PIN_CL32	FMCP HA bank data n22	1.2 V
FMCP_HA_n[23]	PIN_CF33	FMCP HA bank data n23	1.2 V
FMCP_HB_p[0]	PIN_DC40	FMCP HB bank data p0	1.2 V
FMCP_HB_p[1] *(1)	PIN_CU36	FMCP HB bank data p1	1.2 V
FMCP_HB_p[2]	PIN_DC42	FMCP HB bank data p2	1.2 V
FMCP_HB_p[3]	PIN_CV39	FMCP HB bank data p3	1.2 V
FMCP_HB_p[4]	PIN_DB33	FMCP HB bank data p4	1.2 V
FMCP_HB_p[5]	PIN_CV41	FMCP HB bank data p5	1.2 V
FMCP_HB_p[6]	PIN_CV33	FMCP HB bank data p6	1.2 V
FMCP_HB_p[7]	PIN_DB43	FMCP HB bank data p7	1.2 V
FMCP_HB_p[8]	PIN_CV35	FMCP HB bank data p8	1.2 V
FMCP_HB_p[9]	PIN_CV43	FMCP HB bank data p9	1.2 V
FMCP_HB_p[10]	PIN_DB31	FMCP HB bank data p10	1.2 V
FMCP_HB_p[11]	PIN_DB39	FMCP HB bank data p11	1.2 V
FMCP_HB_p[12]	PIN_CU38	FMCP HB bank data p12	1.2 V
FMCP_HB_p[13]	PIN_DB41	FMCP HB bank data p13	1.2 V
FMCP_HB_p[14]	PIN_DB35	FMCP HB bank data p14	1.2 V
FMCP_HB_p[15]	PIN_DC34	FMCP HB bank data p15	1.2 V
FMCP_HB_p[16]	PIN_CU40	FMCP HB bank data p16	1.2 V
FMCP_HB_p[17]	PIN_CV31	FMCP HB bank data p17	1.2 V
FMCP_HB_p[18]	PIN_CU32	FMCP HB bank data p18	1.2 V

FMCP_HB_p[19]	PIN_DC36	FMCP HB bank data p19	1.2 V
FMCP_HB_p[20]	PIN_CU42	FMCP HB bank data p20	1.2 V
FMCP_HB_p[21]	PIN_DC32	FMCP HB bank data p21	1.2 V
FMCP_HB_n[0]	PIN_DA40	FMCP HB bank data n0	1.2 V
FMCP_HB_n[1] *(1)	PIN_CR36	FMCP HB bank data n1	1.2 V
FMCP_HB_n[2]	PIN_DA42	FMCP HB bank data n2	1.2 V
FMCP_HB_n[3]	PIN_CT39	FMCP HB bank data n3	1.2 V
FMCP_HB_n[4]	PIN_CY33	FMCP HB bank data n4	1.2 V
FMCP_HB_n[5]	PIN_CT41	FMCP HB bank data n5	1.2 V
FMCP_HB_n[6]	PIN_CT33	FMCP HB bank data n6	1.2 V
FMCP_HB_n[7]	PIN_CY43	FMCP HB bank data n7	1.2 V
FMCP_HB_n[8]	PIN_CT35	FMCP HB bank data n8	1.2 V
FMCP_HB_n[9]	PIN_CT43	FMCP HB bank data n9	1.2 V
FMCP_HB_n[10]	PIN_CY31	FMCP HB bank data n10	1.2 V
FMCP_HB_n[11]	PIN_CY39	FMCP HB bank data n11	1.2 V
FMCP_HB_n[12]	PIN_CR38	FMCP HB bank data n12	1.2 V
FMCP_HB_n[13]	PIN_CY41	FMCP HB bank data n13	1.2 V
FMCP_HB_n[14]	PIN_CY35	FMCP HB bank data n14	1.2 V
FMCP_HB_n[15]	PIN_DA34	FMCP HB bank data n15	1.2 V
FMCP_HB_n[16]	PIN_CR40	FMCP HB bank data n16	1.2 V
FMCP_HB_n[17]	PIN_CT31	FMCP HB bank data n17	1.2 V
FMCP_HB_n[18]	PIN_CR32	FMCP HB bank data n18	1.2 V
FMCP_HB_n[19]	PIN_DA36	FMCP HB bank data n19	1.2 V
FMCP_HB_n[20]	PIN_CR42	FMCP HB bank data n20	1.2 V
FMCP_HB_n[21]	PIN_DA32	FMCP HB bank data n21	1.2 V
FMCP_LA_p[0] *(1)	PIN_CG50	FMCP LA bank data p0	1.2 V
FMCP_LA_p[1]	PIN_CN54	FMCP LA bank data p1	1.2 V
FMCP_LA_p[2]	PIN_CM45	FMCP LA bank data p2	1.2 V

FMCP_LA_p[3]	PIN_CN46	FMCP LA bank data p3	1.2 V
FMCP_LA_p[4]	PIN_CH45	FMCP LA bank data p4	1.2 V
FMCP_LA_p[5]	PIN_CM49	FMCP LA bank data p5	1.2 V
FMCP_LA_p[6]	PIN_CG46	FMCP LA bank data p6	1.2 V
FMCP_LA_p[7]	PIN_CH47	FMCP LA bank data p7	1.2 V
FMCP_LA_p[8]	PIN_CG48	FMCP LA bank data p8	1.2 V
FMCP_LA_p[9]	PIN_CH49	FMCP LA bank data p9	1.2 V
FMCP_LA_p[10]	PIN_CH53	FMCP LA bank data p10	1.2 V
FMCP_LA_p[11]	PIN_CG52	FMCP LA bank data p11	1.2 V
FMCP_LA_p[12]	PIN_CM57	FMCP LA bank data p12	1.2 V
FMCP_LA_p[13]	PIN_CG54	FMCP LA bank data p13	1.2 V
FMCP_LA_p[14]	PIN_CH55	FMCP LA bank data p14	1.2 V
FMCP_LA_p[15]	PIN_CG56	FMCP LA bank data p15	1.2 V
FMCP_LA_p[16]	PIN_CH57	FMCP LA bank data p16	1.2 V
FMCP_LA_p[17]	PIN_CN56	FMCP LA bank data p17	1.2 V
FMCP_LA_p[18]	PIN_CM55	FMCP LA bank data p18	1.2 V
FMCP_LA_p[19]	PIN_CM47	FMCP LA bank data p19	1.2 V
FMCP_LA_p[20]	PIN_CM53	FMCP LA bank data p20	1.2 V
FMCP_LA_p[21]	PIN_DB49	FMCP LA bank data p21	1.2 V
FMCP_LA_p[22]	PIN_DB57	FMCP LA bank data p22	1.2 V
FMCP_LA_p[23]	PIN_DC56	FMCP LA bank data p23	1.2 V
FMCP_LA_p[24]	PIN_DB47	FMCP LA bank data p24	1.2 V
FMCP_LA_p[25]	PIN_DB53	FMCP LA bank data p25	1.2 V
FMCP_LA_p[26]	PIN_CV49	FMCP LA bank data p26	1.2 V
FMCP_LA_p[27]	PIN_DB55	FMCP LA bank data p27	1.2 V
FMCP_LA_p[28]	PIN_DB45	FMCP LA bank data p28	1.2 V
FMCP_LA_p[29]	PIN_CV53	FMCP LA bank data p29	1.2 V
FMCP_LA_p[30]	PIN_CV47	FMCP LA bank data p30	1.2 V

FMCP_LA_p[31]	PIN_DC50	FMCP LA bank data p31	1.2 V
FMCP_LA_p[32]	PIN_DC46	FMCP LA bank data p32	1.2 V
FMCP_LA_p[33]	PIN_DC48	FMCP LA bank data p33	1.2 V
FMCP_LA_n[0] *(1)	PIN_CE50	FMCP LA bank data n0	1.2 V
FMCP_LA_n[1]	PIN_CL54	FMCP LA bank data n1	1.2 V
FMCP_LA_n[2]	PIN_CK45	FMCP LA bank data n2	1.2 V
FMCP_LA_n[3]	PIN_CL46	FMCP LA bank data n3	1.2 V
FMCP_LA_n[4]	PIN_CF45	FMCP LA bank data n4	1.2 V
FMCP_LA_n[5]	PIN_CK49	FMCP LA bank data n5	1.2 V
FMCP_LA_n[6]	PIN_CE46	FMCP LA bank data n6	1.2 V
FMCP_LA_n[7]	PIN_CF47	FMCP LA bank data n7	1.2 V
FMCP_LA_n[8]	PIN_CE48	FMCP LA bank data n8	1.2 V
FMCP_LA_n[9]	PIN_CF49	FMCP LA bank data n9	1.2 V
FMCP_LA_n[10]	PIN_CF53	FMCP LA bank data n10	1.2 V
FMCP_LA_n[11]	PIN_CE52	FMCP LA bank data n11	1.2 V
FMCP_LA_n[12]	PIN_CK57	FMCP LA bank data n12	1.2 V
FMCP_LA_n[13]	PIN_CE54	FMCP LA bank data n13	1.2 V
FMCP_LA_n[14]	PIN_CF55	FMCP LA bank data n14	1.2 V
FMCP_LA_n[15]	PIN_CE56	FMCP LA bank data n15	1.2 V
FMCP_LA_n[16]	PIN_CF57	FMCP LA bank data n16	1.2 V
FMCP_LA_n[17]	PIN_CL56	FMCP LA bank data n17	1.2 V
FMCP_LA_n[18]	PIN_CK55	FMCP LA bank data n18	1.2 V
FMCP_LA_n[19]	PIN_CK47	FMCP LA bank data n19	1.2 V
FMCP_LA_n[20]	PIN_CK53	FMCP LA bank data n20	1.2 V
FMCP_LA_n[21]	PIN_CY49	FMCP LA bank data n21	1.2 V
FMCP_LA_n[22]	PIN_CY57	FMCP LA bank data n22	1.2 V
FMCP_LA_n[23]	PIN_DA56	FMCP LA bank data n23	1.2 V
FMCP_LA_n[24]	PIN_CY47	FMCP LA bank data n24	1.2 V

FMCP_LA_n[25]	PIN_CY53	FMCP LA bank data n25	1.2 V
FMCP_LA_n[26]	PIN_CT49	FMCP LA bank data n26	1.2 V
FMCP_LA_n[27]	PIN_CY55	FMCP LA bank data n27	1.2 V
FMCP_LA_n[28]	PIN_CY45	FMCP LA bank data n28	1.2 V
FMCP_LA_n[29]	PIN_CT53	FMCP LA bank data n29	1.2 V
FMCP_LA_n[30]	PIN_CT47	FMCP LA bank data n30	1.2 V
FMCP_LA_n[31]	PIN_DA50	FMCP LA bank data n31	1.2 V
FMCP_LA_n[32]	PIN_DA46	FMCP LA bank data n32	1.2 V
FMCP_LA_n[33]	PIN_DA48	FMCP LA bank data n33	1.2 V
FMCP_GBTCLK_M2C_p[0]	PIN_AJ48	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_GBTCLK_M2C_p[1]	PIN_AE48	LVDS input from the installed FMCP card to dedicated reference clock input pin	HCSL
FMCP_DP_C2M_p[0]	PIN_BP55	Transmit pair p0 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[1]	PIN_BN52	Transmit pair p1 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[2]	PIN_BK55	Transmit pair p2 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[3]	PIN_BJ52	Transmit pair p3 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[4]	PIN_BF55	Transmit pair p4 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[5]	PIN_BE52	Transmit pair p5 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[6]	PIN_BB55	Transmit pair p6 of the FPGA transceiver	High Speed Differential I/O

FMCP_DP_C2M_p[7]	PIN_BA52	Transmit pair p7 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[8]	PIN_AV55	Transmit pair p8 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[9]	PIN_AU52	Transmit pair p9 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[10]	PIN_AP55	Transmit pair p10 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[11]	PIN_AN52	Transmit pair p11 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[12]	PIN_AK55	Transmit pair p12 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[13]	PIN_AJ52	Transmit pair p13 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[14]	PIN_AF55	Transmit pair p14 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_C2M_p[15]	PIN_AE52	Transmit pair p15 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[0]	PIN_BP61	Receiver pair p0 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[1]	PIN_BN58	Receiver pair p1 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[2]	PIN_BK61	Receiver pair p2 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[3]	PIN_BJ58	Receiver pair p3 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[4]	PIN_BF61	Receiver pair p4 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[5]	PIN_BE58	Receiver pair p5 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[6]	PIN_BB61	Receiver pair p6 of the FPGA transceiver	High Speed Differential I/O

FMCP_DP_M2C_p[7]	PIN_BA58	Receiver pair p7 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[8]	PIN_AV61	Receiver pair p8 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[9]	PIN_AU58	Receiver pair p9 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[10]	PIN_AP61	Receiver pair p10 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[11]	PIN_AN58	Receiver pair p11 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[12]	PIN_AK61	Receiver pair p12 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[13]	PIN_AJ58	Receiver pair p13 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[14]	PIN_AF61	Receiver pair p14 of the FPGA transceiver	High Speed Differential I/O
FMCP_DP_M2C_p[15]	PIN_AE58	Receiver pair p15 of the FPGA transceiver	High Speed Differential I/O
FMCP_REFCLK_C2M_p	PIN_CV55	Reference clock from carrier card mezzanine module to positive	DIFFERENTIAL 1.2-V SSTL
FMCP_REFCLK_M2C_p	PIN_CU46	Reference clock from mezzanine module to carrier card positive	True Differential Signaling
FMCP_GA[0]	PIN_CL48	FMCP geographical address 0	3.3 V*(2)
FMCP_GA[1]	PIN_CN48	FMCP geographical address 1	3.3 V*(2)
FMCP_SCL	PIN_CL52	Management serial clock line	3.3 V*(2)
FMCP_SDA	PIN_CU56	Management serial data line	3.3 V*(2)

FMCP_RES[0]	PIN_BU58	Reserved	1.8 V*(3)
FMCP_RES[1]	PIN_CR56	Reserved	1.2 V
FMCP_SYNC_C2M_p	PIN_CV45	Synchronize signal from carrier card to mezzanine module positive	DIFFERENTIAL 1.2-V SSTL
FMCP_SYNC_M2C_p	PIN_CN50	Synchronize signal from mezzanine module to carrier card positive	True Differential Signaling

- *(1): FPGA dedicated clock input pin.
  *(2): There are level shift ICs that convert FMCP_VCCIO to 3.3V between the FPGA pins and the FMC pins.
  *(3): For PCIe Applications

2.7 Clock Circuit

The development board includes a 50 MHz TCXO, a 125 MHz OSC, a 100Mhz OSC and two programmable clock generators. **Figure 2-15** shows the default frequencies of on-board all external clocks going to the Agilex SoC FPGA.

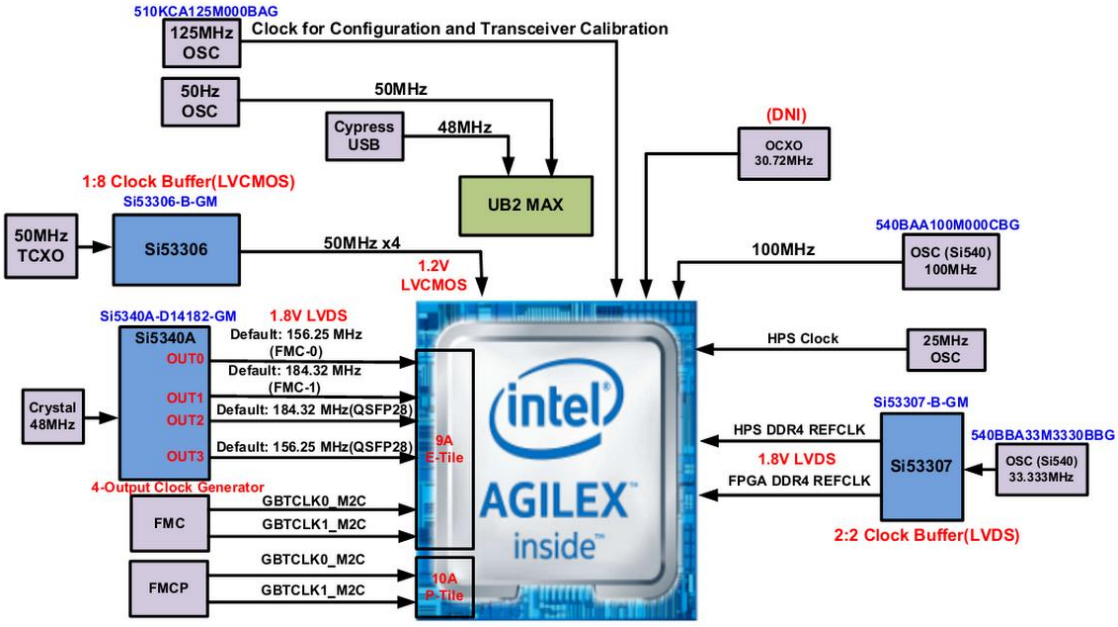

Figure 2-15 Clock circuit of the FPGA Board

A clock buffer is used to duplicate the 50 MHz TCXO output clock, so there are four 50MHz clocks fed into different FPGA banks. The programming clock generator (Si5340A) with low-jitter clock outputs are used to provide special and high- quality clock signals for high-speed transceivers. Through I2C serial interface, the clock generator controllers in the Agilex SoC FPGA can be used to program the Si5340A to generate FMC and FMC+ connector reference clock and QSFP28 reference clocks respectively.

For memory interface, the board provides a 33.333Mhz clock and fan out it to two different clocks to the Agilex FPGA via clock buffer (Si53307). The two clocks are used for the reference clock of the four DDR4 SODIMMs.

One oscillator provides a 125 MHz clock used as configuration or used as the clock for transceiver calibration. Besides, there is one 100 MHz clock source to use as the FPGA input clock.

Finally, the Apollo Agilex board has reserved a high stability OCXO oscillator (U45, not installed), which is reserved for use when users need CRPI applications.

Table 2-17 Clock source and clock pin to the FPGA

Source	Schematic Signal Name	Default Frequency	I/O Standard	FPGA Pin Number	Application
U20 Si53306	CLK_50_B3C	50.0 MHz	1.2V	PIN_G26	User application
	CLK_50_B3A		1.2V	PIN_U52	User application
	CLK_50_B2A		1.2V	PIN_CN52	User application
	CLK_50_B2D		1.2V	PIN_DC8	User application
Y8 OSC	OSC_CLK_1	125MHz	1.8V	PIN_CC60	Clock for configuration and transceiver

					calibration
Y7 OSC	CLK_100_B2A_p CLK_100_B2A_n	100Mhz	True Differential Signaling	PIN_CU50 PIN_CR50	User application
Y4 OSC and U59 Clock Buffer	DDR4A_REFCLK_p	33.33Mhz	True Differential Signaling	PIN_L10	DDR4 reference clock for A port
	DDR4B_REFCLK_p	33.33Mhz	True Differential Signaling	PIN_L40	DDR4 reference clock for B port
U24 Si5340A	FMC_REFCLK0_p	156.25MHz	DIFFERENTIAL LVPECL	PIN_AT13	FMC connector reference clock 0
	FMC_REFCLK1_p	184.32MHz	DIFFERENTIAL LVPECL	PIN_AK13	FMC connector reference clock 1
	QSFP28_REFCLK_p	156.25MHz	DIFFERENTIAL LVPECL	PIN_AJ12	QSFP28 port reference clock port
	QSFP28RSV_REFCLK_p	184.32MHz	DIFFERENTIAL LVPECL	PIN_AR14	Reserved clock for QSFP28 port
U45 High Stability OCXO(Not installed)	CLK_30M72	30.72MHz	1.2V	PIN_CN8 (Reserved)	Reserved for CPRI application

2.8 USB to UART

The Apollo Agilex board provides three UART functions (See **Figure 2-16**). Two of them are connected to HPS fabric and FPGA, allowing host to communicate and debug with the HPS fabric or FPGA through the UART interface. The last one is to connect to the system MAX10 device. It allows users to monitor various status of the board such as temperature and voltage value from the Host. The Apollo Agilex uses a USB hub to allow three USB to UART interface (HPS fabric, FPGA and system MAX10) and USB Blaster II circuit to share a Mini USB connector to connect to the host. Users only need one Mini USB cable to establish several UART and JTAG connections with the Host to transmit data.

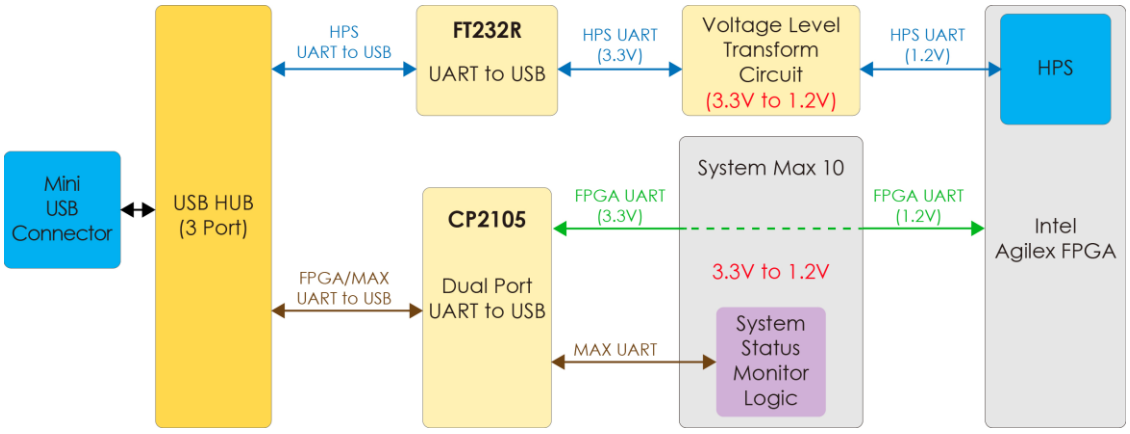

Figure 2-16 Three UART interface on the Apollo Agilex board

■ USB to UART for HPS Fabric

The Apollo Agilex board provides a UART interface for users to communicate and transfer data with HPS through the host. This interface is mainly implemented through a USB to serial UART chip (FT232R). It can convert commands and data from the host via USB protocol to the UART interface and send it to HPS. Please note that due to space constraints,

For more information about the USB UART chip is available on the manufacturer's website, or in the directory \Datasheets\UART_TO_USB\DS_FT232R.pdf of Apollo Agilex system CD. **Figure 2-17** shows the connections between the HPS, FT232R chip, and the USB Mini-B connector.

Table 2-18 lists the pin assignment of UART interface connected to the HPS.

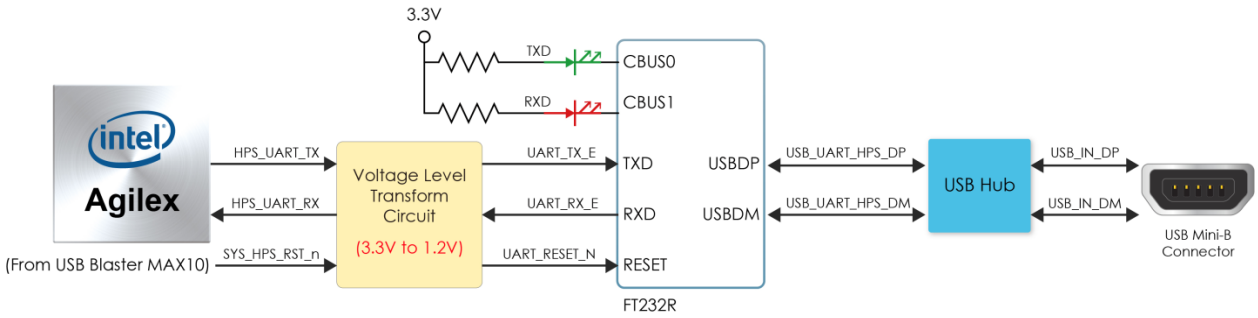

Figure 2-17 Connections between the HPS of Apollo Agilex and FT232R Chip

Table 2-18 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_K29	HPS UART Receiver	1.2V
HPS_UART_TX	PIN_F32	HPS UART Transmitter	1.2V

■ USB to UART for FPGA

The Apollo Agilex board is also equipped with a UART interface for FPGA (with hardware flow control: CTS/RTS), allowing users to communicate with the FPGA and the Host through UART. This UART interface is converted to USB interface via a dual UART to USB (CP2105). For detailed chip information, please refer to \Datasheets\UART_TO_USB\CP2105-F01-GM.pdf.

Table 2-18 lists the pin assignment of UART interface connected to the HPS.

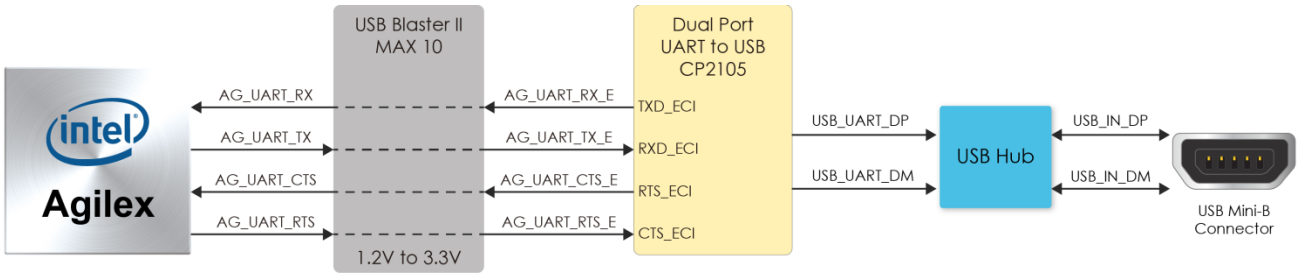

Figure 2-18 Connections between the HPS of Apollo Agilex and FT232R Chip

Table 2-19 Pin Assignment of UART Interface

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_UART_RX	PIN_K29	HPS UART Receiver	1.2V
HPS_UART_TX	PIN_F32	HPS UART Transmitter	1.2V

■ USB to UART for System MAX10

The last USB to UART interface is connected with the System MAX10. It allows users to monitor the status of the board from the host through the UART interface. As shown in **Figure 2-19**, the Apollo Agilex board provides several sensors to monitor the status of the board, such as FPGA temperature, board power monitor, and fan speed status. These interfaces are connected to the System MAX10 FPGA on the board. The board management logic (Dashboard) in the system MAX10 FPGA will monitor these status and perform corresponding control according to the status. For example, when the temperature of the FPGA increases, the system will automatically increase the fan speed to reduce the temperature. When the temperature of the FPGA continues to exceed the working range (such as a fan failure condition), the FPGA power will be cut to protect the board.

See chapter 3 for details. Terasic also provide a “board information IP” that allow user can place it in the Agilex FPGA to read these board status. Please refer to the section 2.5 of the Apollo Agilex demonstration manual.

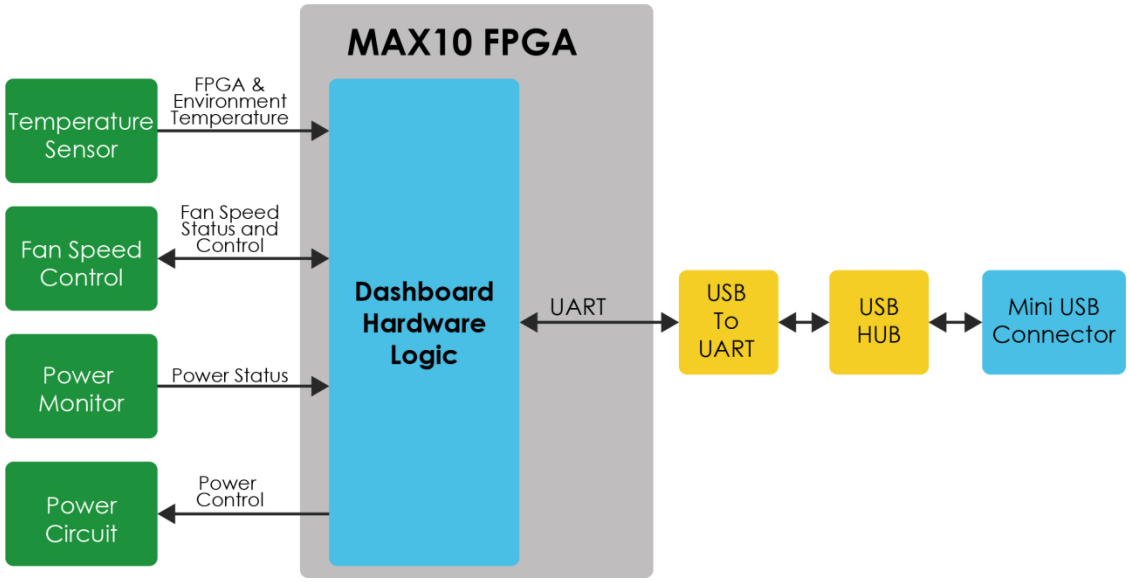

Figure 2-19 Block diagram of the system status interface

2.9 DDR4 SODIMM Socket

The development board supports two independent banks of banks of DDR4 SDRAM SO-DIMM (**DDR4 SO-DIMM Socket A**, and **DDR4 SO-DIMM Socket B**). Each DDR4

SO-DIMM can support 16GB DDR4 SO-DIMM memory (Single Rank). The I/O bank where DDR4 SO-DIMM Socket A is located can implement Intel Agilex FPGA EMIF IP with the Intel Agilex FPGA Hard Processor Subsystem (HPS). If HPS EMIF is not used in a system, the DDR4 SO-DIMM Socket A can be used for the EMIF of the FPGA fabric. The DDR4 SO-DIMM Socket A and B can run at the fastest clock frequency of 1600MHz clock (**for B1E1 FPGA device and single rank DDR4 SO-DIMM**) for a maximum theoretical bandwidth up to 205 Gbps.

Table 2-20 shows the Maximum capacity and speed supported by each DDR4 SO-DIMM socket. **Figure 2-20** shows the connections between the DDR4 SO-DIMM socket and Agilex SoC FPGA.

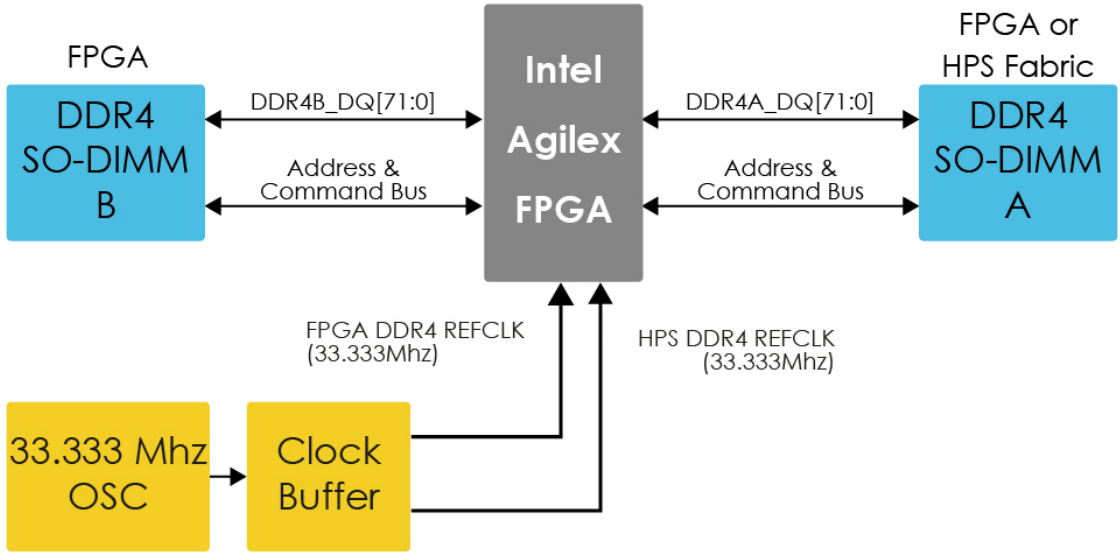

Figure 2-20 Maximum capacity and speed supported by each DDR4 SO-DIMM socket

The pin assignments for DDR4 SDRAM Bank A and Bank B are listed in **Table 2-21** and **Table 2-22** respectively.

Table 2-20 Pin Assignment of UART Interface

	DDR4 SO-DIMM Socket A (HPA Fabric and FPGA)	DDR4 SO-DIMM Socket B (FPGA)
Support Rank	Single	
Support ECC	Yes	
Speed for B2E2 device	2666MT/s	
Speed for B1E1 device	3200MT/s	

Standard Capacity	8GB+ECC(singe rank)
Maximum Capacity	16GB+ECC (single rank) (MTA9ASF2G72HZ-3G2B2)

Table 2-21 DDR4A Bank Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
DDR4A_DQ0	Data [0]	1.2-V POD	PIN_J6
DDR4A_DQ1	Data [1]	1.2-V POD	PIN_H9
DDR4A_DQ2	Data [2]	1.2-V POD	PIN_F9
DDR4A_DQ3	Data [3]	1.2-V POD	PIN_G10
DDR4A_DQ4	Data [4]	1.2-V POD	PIN_H5
DDR4A_DQ5	Data [5]	1.2-V POD	PIN_J10
DDR4A_DQ6	Data [6]	1.2-V POD	PIN_G6
DDR4A_DQ7	Data [7]	1.2-V POD	PIN_F5
DDR4A_DQ8	Data [8]	1.2-V POD	PIN_C6
DDR4A_DQ9	Data [9]	1.2-V POD	PIN_A6
DDR4A_DQ10	Data [10]	1.2-V POD	PIN_B9
DDR4A_DQ11	Data [11]	1.2-V POD	PIN_A10
DDR4A_DQ12	Data [12]	1.2-V POD	PIN_D5
DDR4A_DQ13	Data [13]	1.2-V POD	PIN_B5
DDR4A_DQ14	Data [14]	1.2-V POD	PIN_C10
DDR4A_DQ15	Data [15]	1.2-V POD	PIN_D9
DDR4A_DQ16	Data [16]	1.2-V POD	PIN_D13
DDR4A_DQ17	Data [17]	1.2-V POD	PIN_B13
DDR4A_DQ18	Data [18]	1.2-V POD	PIN_B17
DDR4A_DQ19	Data [19]	1.2-V POD	PIN_A16
DDR4A_DQ20	Data [20]	1.2-V POD	PIN_A12
DDR4A_DQ21	Data [21]	1.2-V POD	PIN_C12
DDR4A_DQ22	Data [22]	1.2-V POD	PIN_D17
DDR4A_DQ23	Data [23]	1.2-V POD	PIN_C16
DDR4A_DQ24	Data [24]	1.2-V POD	PIN_F17
DDR4A_DQ25	Data [25]	1.2-V POD	PIN_F13

DDR4A_DQ26	Data [26]	1.2-V POD	PIN_G16
DDR4A_DQ27	Data [27]	1.2-V POD	PIN_H17
DDR4A_DQ28	Data [28]	1.2-V POD	PIN_G12
DDR4A_DQ29	Data [29]	1.2-V POD	PIN_H13
DDR4A_DQ30	Data [30]	1.2-V POD	PIN_J12
DDR4A_DQ31	Data [31]	1.2-V POD	PIN_J16
DDR4A_DQ32	Data [32]	1.2-V POD	PIN_N20
DDR4A_DQ33	Data [33]	1.2-V POD	PIN_M23
DDR4A_DQ34	Data [34]	1.2-V POD	PIN_N24
DDR4A_DQ35	Data [35]	1.2-V POD	PIN_P19
DDR4A_DQ36	Data [36]	1.2-V POD	PIN_L20
DDR4A_DQ37	Data [37]	1.2-V POD	PIN_L24
DDR4A_DQ38	Data [38]	1.2-V POD	PIN_P23
DDR4A_DQ39	Data [39]	1.2-V POD	PIN_M19
DDR4A_DQ40	Data [40]	1.2-V POD	PIN_T23
DDR4A_DQ41	Data [41]	1.2-V POD	PIN_V19
DDR4A_DQ42	Data [42]	1.2-V POD	PIN_U24
DDR4A_DQ43	Data [43]	1.2-V POD	PIN_W20
DDR4A_DQ44	Data [44]	1.2-V POD	PIN_U20
DDR4A_DQ45	Data [45]	1.2-V POD	PIN_T19
DDR4A_DQ46	Data [46]	1.2-V POD	PIN_V23
DDR4A_DQ47	Data [47]	1.2-V POD	PIN_W24
DDR4A_DQ48	Data [48]	1.2-V POD	PIN_W30
DDR4A_DQ49	Data [49]	1.2-V POD	PIN_U30
DDR4A_DQ50	Data [50]	1.2-V POD	PIN_W26
DDR4A_DQ51	Data [51]	1.2-V POD	PIN_V31
DDR4A_DQ52	Data [52]	1.2-V POD	PIN_T27
DDR4A_DQ53	Data [53]	1.2-V POD	PIN_T31
DDR4A_DQ54	Data [54]	1.2-V POD	PIN_V27
DDR4A_DQ55	Data [55]	1.2-V POD	PIN_U26
DDR4A_DQ56	Data [56]	1.2-V POD	PIN_L30
DDR4A_DQ57	Data [57]	1.2-V POD	PIN_L26
DDR4A_DQ58	Data [58]	1.2-V POD	PIN_N26
DDR4A_DQ59	Data [59]	1.2-V POD	PIN_P27
DDR4A_DQ60	Data [60]	1.2-V POD	PIN_M27

DDR4A_DQ61	Data [61]	1.2-V POD	PIN_M31
DDR4A_DQ62	Data [62]	1.2-V POD	PIN_N30
DDR4A_DQ63	Data [63]	1.2-V POD	PIN_P31
DDR4A_DQ64	Data [64]	1.2-V POD	PIN_V9
DDR4A_DQ65	Data [65]	1.2-V POD	PIN_T9
DDR4A_DQ66	Data [66]	1.2-V POD	PIN_U10
DDR4A_DQ67	Data [67]	1.2-V POD	PIN_W10
DDR4A_DQ68	Data [68]	1.2-V POD	PIN_W6
DDR4A_DQ69	Data [69]	1.2-V POD	PIN_T5
DDR4A_DQ70	Data [70]	1.2-V POD	PIN_U6
DDR4A_DQ71	Data [71]	1.2-V POD	PIN_V5
DDR4A_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_G8
DDR4A_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_J8
DDR4A_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_A8
DDR4A_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_C8
DDR4A_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_B15
DDR4A_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_D15
DDR4A_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_F15
DDR4A_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_H15
DDR4A_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2-V POD	PIN_L22
DDR4A_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2-V POD	PIN_N22
DDR4A_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2-V POD	PIN_U22
DDR4A_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2-V POD	PIN_W22

DDR4A_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2-V POD	PIN_T29
DDR4A_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2-V POD	PIN_V29
DDR4A_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2-V POD	PIN_M29
DDR4A_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2-V POD	PIN_P29
DDR4A_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2-V POD	PIN_U8
DDR4A_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2-V POD	PIN_W8
DDR4A_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_F7
DDR4A_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_B7
DDR4A_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_A14
DDR4A_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_G14
DDR4A_DBI_n4	Data Bus Inversion [4]	1.2-V POD	PIN_M21
DDR4A_DBI_n5	Data Bus Inversion [5]	1.2-V POD	PIN_T21
DDR4A_DBI_n6	Data Bus Inversion [6]	1.2-V POD	PIN_U28
DDR4A_DBI_n7	Data Bus Inversion [7]	1.2-V POD	PIN_L28
DDR4A_DBI_n8	Data Bus Inversion [8]	1.2-V POD	PIN_T7
DDR4A_A0	Address [0]	SSTL-12	PIN_T17
DDR4A_A1	Address [1]	SSTL-12	PIN_V17
DDR4A_A2	Address [2]	SSTL-12	PIN_U16
DDR4A_A3	Address [3]	SSTL-12	PIN_W16
DDR4A_A4	Address [4]	SSTL-12	PIN_T15
DDR4A_A5	Address [5]	SSTL-12	PIN_V15

DDR4A_A6	Address [6]	SSTL-12	PIN_U14
DDR4A_A7	Address [7]	SSTL-12	PIN_W14
DDR4A_A8	Address [8]	SSTL-12	PIN_T13
DDR4A_A9	Address [9]	SSTL-12	PIN_V13
DDR4A_A10	Address [10]	SSTL-12	PIN_U12
DDR4A_A11	Address [11]	SSTL-12	PIN_W12
DDR4A_A12	Address [12]	SSTL-12	PIN_P9
DDR4A_A13	Address [13]	SSTL-12	PIN_L8
DDR4A_A14	Address [14]/ WE_n	SSTL-12	PIN_N8
DDR4A_A15	Address [15]/ CAS_n	SSTL-12	PIN_M7
DDR4A_A16	Address [16]/ RAS_n	SSTL-12	PIN_P7
DDR4A_BA0	Bank Select [0]	SSTL-12	PIN_N6
DDR4A_BA1	Bank Select [1]	SSTL-12	PIN_M5
DDR4A_BG0	Bank Group Select [0]	SSTL-12	PIN_P5
DDR4A_BG1	Bank Group Select [1]	SSTL-12	PIN_M17
DDR4A_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_M13
DDR4A_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_P13
DDR4A_CKE	Clock Enable pin	SSTL-12	PIN_L14
DDR4A_ODT	On Die Termination	SSTL-12	PIN_M15
DDR4A_CS_n	Chip Select	SSTL-12	PIN_L16
DDR4A_PAR	Command and Address Parity Input	SSTL-12	PIN_N12
DDR4A_ALERT_n	Register ALERT_n output	1.2 V	PIN_L6
DDR4A_ACT_n	Activation Command Input	SSTL-12	PIN_N16

DDR4A_RESET_n	Chip Reset	1.2 V	PIN_P17
DDR4A_EVENT_n	Chip Temperature Event	1.2 V	PIN_F29
DDR4A_SDA	Chip I2C Serial Data Bus	1.2 V	PIN_J28
DDR4A_SCL	Chip I2C Serial Clock	1.2 V	PIN_G30
DDR4A_REFCLK_p	DDR4 A port Reference Clock p	LVDS	PIN_L10
DDR4A_REFCLK_n	DDR4 A port Reference Clock n	LVDS	PIN_N10
DDR4A_RZQ	External precision resistor	1.2 V	PIN_M9

Table 2-22 DDR4B Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	FPGA Pin Number
DDR4B_DQ0	Data [0]	1.2-V POD	PIN_F33
DDR4B_DQ1	Data [1]	1.2-V POD	PIN_J34
DDR4B_DQ2	Data [2]	1.2-V POD	PIN_G38
DDR4B_DQ3	Data [3]	1.2-V POD	PIN_H37
DDR4B_DQ4	Data [4]	1.2-V POD	PIN_H33
DDR4B_DQ5	Data [5]	1.2-V POD	PIN_J38
DDR4B_DQ6	Data [6]	1.2-V POD	PIN_F37
DDR4B_DQ7	Data [7]	1.2-V POD	PIN_G34
DDR4B_DQ8	Data [8]	1.2-V POD	PIN_H41
DDR4B_DQ9	Data [9]	1.2-V POD	PIN_H45
DDR4B_DQ10	Data [10]	1.2-V POD	PIN_G44
DDR4B_DQ11	Data [11]	1.2-V POD	PIN_G40
DDR4B_DQ12	Data [12]	1.2-V POD	PIN_J40
DDR4B_DQ13	Data [13]	1.2-V POD	PIN_F45
DDR4B_DQ14	Data [14]	1.2-V POD	PIN_F41
DDR4B_DQ15	Data [15]	1.2-V POD	PIN_J44
DDR4B_DQ16	Data [16]	1.2-V POD	PIN_B41
DDR4B_DQ17	Data [17]	1.2-V POD	PIN_A40

DDR4B_DQ18	Data [18]	1.2-V POD	PIN_D45
DDR4B_DQ19	Data [19]	1.2-V POD	PIN_A44
DDR4B_DQ20	Data [20]	1.2-V POD	PIN_C44
DDR4B_DQ21	Data [21]	1.2-V POD	PIN_C40
DDR4B_DQ22	Data [22]	1.2-V POD	PIN_B45
DDR4B_DQ23	Data [23]	1.2-V POD	PIN_D41
DDR4B_DQ24	Data [24]	1.2-V POD	PIN_A38
DDR4B_DQ25	Data [25]	1.2-V POD	PIN_C34
DDR4B_DQ26	Data [26]	1.2-V POD	PIN_D33
DDR4B_DQ27	Data [27]	1.2-V POD	PIN_B37
DDR4B_DQ28	Data [28]	1.2-V POD	PIN_D37
DDR4B_DQ29	Data [29]	1.2-V POD	PIN_B33
DDR4B_DQ30	Data [30]	1.2-V POD	PIN_A34
DDR4B_DQ31	Data [31]	1.2-V POD	PIN_C38
DDR4B_DQ32	Data [32]	1.2-V POD	PIN_H51
DDR4B_DQ33	Data [33]	1.2-V POD	PIN_G48
DDR4B_DQ34	Data [34]	1.2-V POD	PIN_G52
DDR4B_DQ35	Data [35]	1.2-V POD	PIN_H47
DDR4B_DQ36	Data [36]	1.2-V POD	PIN_J48
DDR4B_DQ37	Data [37]	1.2-V POD	PIN_F47
DDR4B_DQ38	Data [38]	1.2-V POD	PIN_F51
DDR4B_DQ39	Data [39]	1.2-V POD	PIN_J52
DDR4B_DQ40	Data [40]	1.2-V POD	PIN_B51
DDR4B_DQ41	Data [41]	1.2-V POD	PIN_C48
DDR4B_DQ42	Data [42]	1.2-V POD	PIN_D51
DDR4B_DQ43	Data [43]	1.2-V POD	PIN_C52
DDR4B_DQ44	Data [44]	1.2-V POD	PIN_A48
DDR4B_DQ45	Data [45]	1.2-V POD	PIN_B47
DDR4B_DQ46	Data [46]	1.2-V POD	PIN_A52
DDR4B_DQ47	Data [47]	1.2-V POD	PIN_D47
DDR4B_DQ48	Data [48]	1.2-V POD	PIN_A54
DDR4B_DQ49	Data [49]	1.2-V POD	PIN_B55
DDR4B_DQ50	Data [50]	1.2-V POD	PIN_D59
DDR4B_DQ51	Data [51]	1.2-V POD	PIN_F61
DDR4B_DQ52	Data [52]	1.2-V POD	PIN_C54

DDR4B_DQ53	Data [53]	1.2-V POD	PIN_D55
DDR4B_DQ54	Data [54]	1.2-V POD	PIN_H61
DDR4B_DQ55	Data [55]	1.2-V POD	PIN_C58
DDR4B_DQ56	Data [56]	1.2-V POD	PIN_F55
DDR4B_DQ57	Data [57]	1.2-V POD	PIN_H59
DDR4B_DQ58	Data [58]	1.2-V POD	PIN_F59
DDR4B_DQ59	Data [59]	1.2-V POD	PIN_J54
DDR4B_DQ60	Data [60]	1.2-V POD	PIN_G54
DDR4B_DQ61	Data [61]	1.2-V POD	PIN_H55
DDR4B_DQ62	Data [62]	1.2-V POD	PIN_G58
DDR4B_DQ63	Data [63]	1.2-V POD	PIN_J58
DDR4B_DQ64	Data [64]	1.2-V POD	PIN_N58
DDR4B_DQ65	Data [65]	1.2-V POD	PIN_L58
DDR4B_DQ66	Data [66]	1.2-V POD	PIN_P55
DDR4B_DQ67	Data [67]	1.2-V POD	PIN_N54
DDR4B_DQ68	Data [68]	1.2-V POD	PIN_P59
DDR4B_DQ69	Data [69]	1.2-V POD	PIN_M59
DDR4B_DQ70	Data [70]	1.2-V POD	PIN_M55
DDR4B_DQ71	Data [71]	1.2-V POD	PIN_L54
DDR4B_DQS0	Data Strobe p[0]	DIFFERENTIAL 1.2-V POD	PIN_F35
DDR4B_DQS_n0	Data Strobe n[0]	DIFFERENTIAL 1.2-V POD	PIN_H35
DDR4B_DQS1	Data Strobe p[1]	DIFFERENTIAL 1.2-V POD	PIN_G42
DDR4B_DQS_n1	Data Strobe n[1]	DIFFERENTIAL 1.2-V POD	PIN_J42
DDR4B_DQS2	Data Strobe p[2]	DIFFERENTIAL 1.2-V POD	PIN_A42
DDR4B_DQS_n2	Data Strobe n[2]	DIFFERENTIAL 1.2-V POD	PIN_C42
DDR4B_DQS3	Data Strobe p[3]	DIFFERENTIAL 1.2-V POD	PIN_B35
DDR4B_DQS_n3	Data Strobe n[3]	DIFFERENTIAL 1.2-V POD	PIN_D35

DDR4B_DQS4	Data Strobe p[4]	DIFFERENTIAL 1.2-V POD	PIN_F49
DDR4B_DQS_n4	Data Strobe n[4]	DIFFERENTIAL 1.2-V POD	PIN_H49
DDR4B_DQS5	Data Strobe p[5]	DIFFERENTIAL 1.2-V POD	PIN_B49
DDR4B_DQS_n5	Data Strobe n[5]	DIFFERENTIAL 1.2-V POD	PIN_D49
DDR4B_DQS6	Data Strobe p[6]	DIFFERENTIAL 1.2-V POD	PIN_A56
DDR4B_DQS_n6	Data Strobe n[6]	DIFFERENTIAL 1.2-V POD	PIN_C56
DDR4B_DQS7	Data Strobe p[7]	DIFFERENTIAL 1.2-V POD	PIN_G56
DDR4B_DQS_n7	Data Strobe n[7]	DIFFERENTIAL 1.2-V POD	PIN_J56
DDR4B_DQS8	Data Strobe p[8]	DIFFERENTIAL 1.2-V POD	PIN_L56
DDR4B_DQS_n8	Data Strobe n[8]	DIFFERENTIAL 1.2-V POD	PIN_N56
DDR4B_DBI_n0	Data Bus Inversion [0]	1.2-V POD	PIN_G36
DDR4B_DBI_n1	Data Bus Inversion [1]	1.2-V POD	PIN_F43
DDR4B_DBI_n2	Data Bus Inversion [2]	1.2-V POD	PIN_B43
DDR4B_DBI_n3	Data Bus Inversion [3]	1.2-V POD	PIN_A36
DDR4B_DBI_n4	Data Bus Inversion [4]	1.2-V POD	PIN_G50
DDR4B_DBI_n5	Data Bus Inversion [5]	1.2-V POD	PIN_A50
DDR4B_DBI_n6	Data Bus Inversion [6]	1.2-V POD	PIN_B57
DDR4B_DBI_n7	Data Bus Inversion [7]	1.2-V POD	PIN_F57

DDR4B_DBI_n8	Data Bus Inversion [8]	1.2-V POD	PIN_M57
DDR4B_A0	Address [0]	SSTL-12	PIN_L40
DDR4B_A1	Address [1]	SSTL-12	PIN_T33
DDR4B_A2	Address [2]	SSTL-12	PIN_V33
DDR4B_A3	Address [3]	SSTL-12	PIN_U34
DDR4B_A4	Address [4]	SSTL-12	PIN_W34
DDR4B_A5	Address [5]	SSTL-12	PIN_T35
DDR4B_A6	Address [6]	SSTL-12	PIN_V35
DDR4B_A7	Address [7]	SSTL-12	PIN_U36
DDR4B_A8	Address [8]	SSTL-12	PIN_W36
DDR4B_A9	Address [9]	SSTL-12	PIN_T37
DDR4B_A10	Address [10]	SSTL-12	PIN_V37
DDR4B_A11	Address [11]	SSTL-12	PIN_U38
DDR4B_A12	Address [12]	SSTL-12	PIN_W38
DDR4B_A13	Address [13]	SSTL-12	PIN_P41
DDR4B_A14	Address [14]/ WE_n	SSTL-12	PIN_L42
DDR4B_A15	Address [15]/ CAS_n	SSTL-12	PIN_N42
DDR4B_A16	Address [16]/ RAS_n	SSTL-12	PIN_M43
DDR4B_BA0	Bank Select [0]	SSTL-12	PIN_N44
DDR4B_BA1	Bank Select [1]	SSTL-12	PIN_M45
DDR4B_BG0	Bank Group Select [0]	SSTL-12	PIN_P45
DDR4B_BG1	Bank Group Select [1]	SSTL-12	PIN_M33
DDR4B_CK	Clock p	DIFFERENTIAL 1.2-V SSTL	PIN_M37
DDR4B_CK_n	Clock n	DIFFERENTIAL 1.2-V SSTL	PIN_P37
DDR4B_CKE	Clock Enable pin	SSTL-12	PIN_L36
DDR4B_ODT	On Die Termination	SSTL-12	PIN_M35

DDR4B_CS_n	Chip Select	SSTL-12	PIN_L34
DDR4B_PAR	Command and Address Parity Input	SSTL-12	PIN_N38
DDR4B_ALERT_n	Register ALERT_n output	1.2 V	PIN_L44
DDR4B_ACT_n	Activation Command Input	SSTL-12	PIN_N34
DDR4B_RESET_n	Chip Reset	1.2 V	PIN_P33
DDR4B_EVENT_n	Chip Temperature Event	1.2 V	PIN_W56
DDR4B_SDA	Chip I2C Serial Data Bus	1.2 V	PIN_B21
DDR4B_SCL	Chip I2C Serial Clock	1.2 V	PIN_V55
DDR4B_REFCLK_p	DDR4 B socket Reference Clock p	LVDS	PIN_L40
DDR4B_REFCLK_n	DDR4 B socket Reference Clock n	LVDS	PIN_N40
DDR4B_RZQ	External precision resistor	1.2 V	PIN_M41

2.10 USB 2.0 OTG PHY

The board provides USB interfaces using the SMSC USB3320 controller. A Microchip USB3320 device is used to interface to a single Type AB Micro-USB connector. This device supports UTMI+ Low Pin Interface (ULPI) to communicate to USB 2.0 controller in HPS. As defined by OTG mode, the PHY can operate in Host or Device modes. When operating in Host mode, the interface will supply the power to the device through the Micro-USB interface. **Figure 2-21** shows the connections of USB PTG PHY to the HPS.

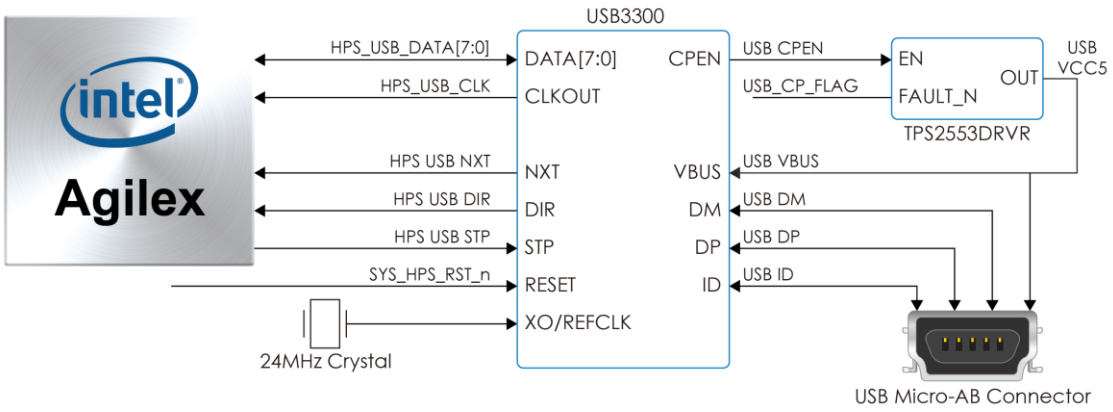

Figure 2-21 Connections between the HPS of Apollo Agilex and USB controller

Table 2-23 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_USB_CLK	PIN_AH5	60MHz Reference Clock Output	1.8V
HPS_USB_DATA[0]	PIN_AB1	HPS USB_DATA[0]	1.8V
HPS_USB_DATA[1]	PIN_AG4	HPS USB_DATA[1]	1.8V
HPS_USB_DATA[2]	PIN_AF5	HPS USB_DATA[2]	1.8V
HPS_USB_DATA[3]	PIN_AC2	HPS USB_DATA[3]	1.8V
HPS_USB_DATA[4]	PIN_AF1	HPS USB_DATA[4]	1.8V
HPS_USB_DATA[5]	PIN_AB3	HPS USB_DATA[5]	1.8V
HPS_USB_DATA[6]	PIN_AF3	HPS USB_DATA[6]	1.8V
HPS_USB_DATA[7]	PIN_AA2	HPS USB_DATA[7]	1.8V
HPS_USB_DIR	PIN_AG6	Direction of the Data Bus	1.8V
HPS_USB_NXT	PIN_AD3	Throttle the Data	1.8V
HPS_USB_STP	PIN_AD1	Stop Data Stream on the Bus	1.8V

2.11 Gigabit Ethernet

The board supports Gigabit Ethernet transfer by an external Micrel KSZ9031RN PHY chip and HPS Ethernet MAC function. The KSZ9031RN chip with integrated 10/100/1000 Mbps Gigabit Ethernet transceiver also supports RGMII MAC interface. **Figure 2-22** shows the connections between the HPS, Gigabit Ethernet PHY, and RJ-45 connector.

For more information about the KSZ9031RN PHY chip and its datasheet, as well as the application notes, which are available on the manufacturer's website.

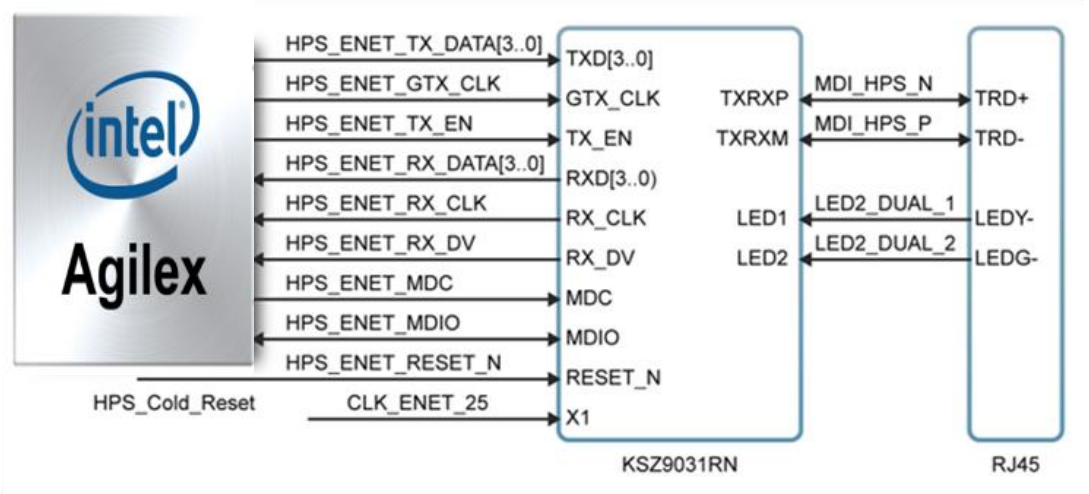

Figure 2-22 Connections between the HPS of Apollo Agilex and RGMII MAC

There are two LEDs, a green LED (LEDG) and a yellow LED (LEDY), which represent the status of the Ethernet PHY (KSZ9031RN). The LED control signals are connected to the LEDs on the RJ45 connector. The state and the definition of LEDG and LEDY are listed in **Table 2-24**. For instance, the connection from board to Gigabit Ethernet is established once the LEDG lights on.

Table 2-24 State and Definition of LED Mode Pins

LED (State)		LED (Definition)		Link /Activity
LEDG	LEDY	LEDG	LEDY	
H	H	OFF	OFF	Link off
L	H	ON	OFF	1000 Link / No Activity
Toggle	H	Blinking	OFF	1000 Link / Activity (RX, TX)
H	L	OFF	ON	100 Link / No Activity
H	Toggle	OFF	Blinking	100 Link / Activity (RX, TX)
L	L	ON	ON	10 Link/ No Activity
Toggle	Toggle	Blinking	Blinking	Link / Activity (RX, TX)

Table 2-25 Pin Assignment of Gigabit Ethernet PHY

Signal Name	FPGA Pin No	Description	I/O Standard
HPS_ENET_TX_CTL	PIN_V1	GMII and MII transmit enable	1.8V
HPS_ENET_TX_DATA[0]	PIN_AD5	MII transmit data[0]	1.8V

HPS_ENET_TX_DATA[1]	PIN_P1	MII transmit data[1]	1.8V
HPS_ENET_TX_DATA[2]	PIN_AF9	MII transmit data[2]	1.8V
HPS_ENET_TX_DATA[3]	PIN_W2	MII transmit data[3]	1.8V
HPS_ENET_RX_CTL	PIN_T1	GMII and MII receive data valid	1.8V
HPS_ENET_RX_DATA[0]	PIN_AF7	GMII and MII receive data[0]	1.8V
HPS_ENET_RX_DATA[1]	PIN_M1	GMII and MII receive data[1]	1.8V
HPS_ENET_RX_DATA[2]	PIN_AB5	GMII and MII receive data[2]	1.8V
HPS_ENET_RX_DATA[3]	PIN_U2	GMII and MII receive data[3]	1.8V
HPS_ENET_RX_CLK	PIN_AA4	GMII and MII receive clock	1.8V
HPS_ENET_MDIO	PIN_AD13	Management Data	1.8V
HPS_ENET_MDC	PIN_F3	Management Data Clock Reference	1.8V
HPS_ENET_TX_CLK	PIN_AC4	GMII Transmit Clock	1.8V

2.12 2x6 GPIO Header

The Apollo Agilex board provides two 2x6 pin GPIO headers (HPS and FPGA for each) to expand the I/O of Agilex SoC FPGA (See **Figure 2-24**). Each header has numbers of the digital FPGA I/O user pins connected to the Agilex SoC FPGA, two 3.3V power pins and two ground pins.

Note: The appearance of these two headers is same as the Terasic TMD header. However, but due to the different I/O voltage level or pin distribution, they do not support TMD interface daughter cards. The detailed I/O mapping will be introduced below.

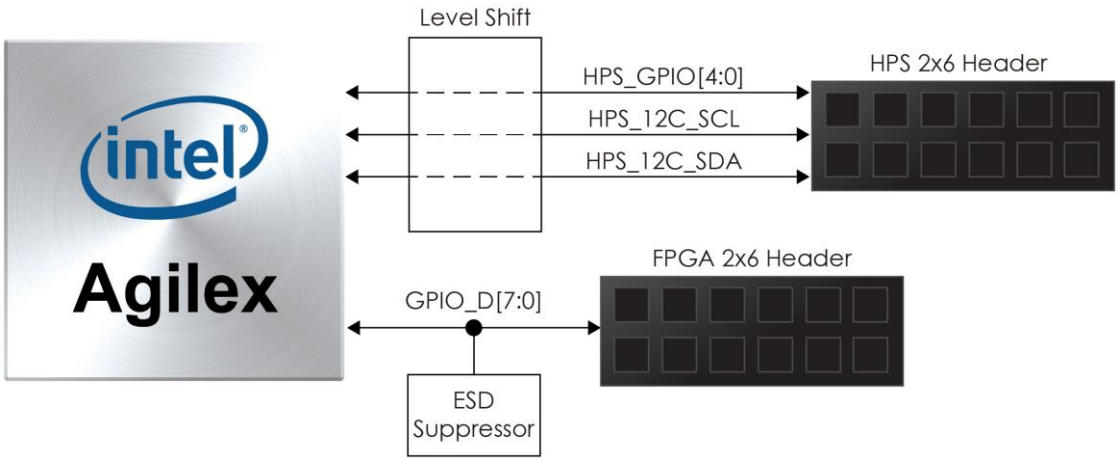

Figure 2-23 Connection between the 1x6 header and Stratix 10 FPGA

■ HPS 2x6 GPIO Header

The HPS 2x6 GPIO header expands 5 GPIO and 1 pair I2C interface of the HPS fabric for users. Users can control these I/Os though the HPS for their application. These HPS I/Os will be converted the voltage level from 1.8v to 3.3V by level translator circuit on the board so that users can connect more interfaces.

Table 2-26 Pin Assignment of USB OTG PHY

Signal Name	FPGA Pin No.	Description	I/O Standard
HPS_GPIO[0]	PIN_AD11	HPS GPIO0	3.3V(*1)
HPS_GPIO[1]	PIN_M3	HPS GPIO1	3.3V(*1)
HPS_GPIO[2]	PIN_AC12	HPS GPIO2	3.3V(*1)
HPS_GPIO[3]	PIN_H3	HPS GPIO3	3.3V(*1)
HPS_GPIO[4]	PIN_AD7	HPS GPIO4	3.3V(*1)
HPS_I2C_SCL	PIN_L2	HPS I2C Clock	3.3V(*1)
HPS_I2C_SDA	PIN_AB7	HPS I2C Data	3.3V(*1)

(*1) Due to the voltage level convert from 1.8v to 3.3V.

■ FPGA 2x6 GPIO Header

The FPGA 2x6 GPIO header expands 8 digital GPIO user pins connected to the Agilex SoC FPGA, two 3.3V power pins and two ground pins. There are two Transient Voltage Suppressor diode arrays used to implement ESD protection for 8 GPIO user pins.

There are two ESD suppressor used to implement ESD protection for 8 GPIO user pins.
Note, the I/O standard of these FPGA I/O are 1.2V.

Signal Name	FPGA Pin No.	Description	I/O Standard
GPIO_D[0]	PIN_M47	FPGA 2x6 header GPIO0	1.2V
GPIO_D[1]	PIN_P47	FPGA 2x6 header GPIO1	1.2V
GPIO_D[2]	PIN_L48	FPGA 2x6 header GPIO2	1.2V
GPIO_D[3]	PIN_N48	FPGA 2x6 header GPIO3	1.2V
GPIO_D[4]	PIN_M49	FPGA 2x6 header GPIO4	1.2V
GPIO_D[5]	PIN_P49	FPGA 2x6 header GPIO5	1.2V
GPIO_D[6]	PIN_L50	FPGA 2x6 header GPIO6	1.2V

GPIO_D[7]	PIN_N50	FPGA 2x6 header GPIO7	1.2V

Figure 2-24 Connection between the 1x6 header and Stratix 10 FPGA

2.13 QSFP28 Port

The development board has one QSFP28 connector that use four pair transceiver channels from the Agilex SoC FPGA device. The QSFP28 module receives the serial data from the Agilex SoC FPGA, and transform them to optical signals. A Low-Jitter programmable clock generator (Si5340A) will provide flexible clock for serial transceivers of the FPGA (See section 2.6). **Figure 2-25** shows the connections between the QSFP28 and Agilex SoC FPGA.

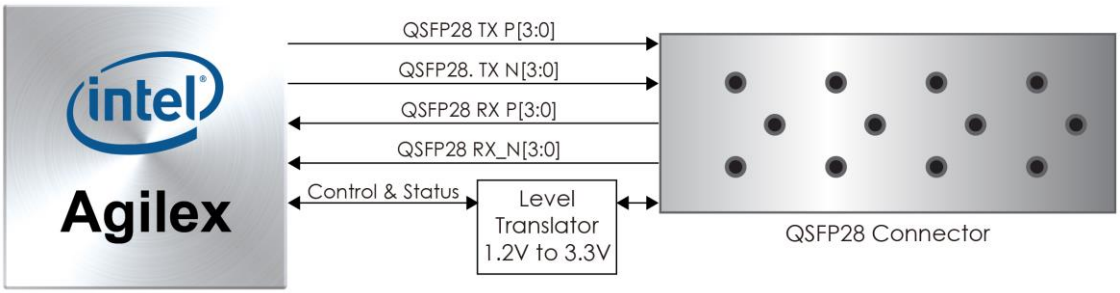

Figure 2-25 Connection between the QSFP28 and FPGA

Table 2-27 lists the QSFP28 pin assignments and signal names relative to the Agilex SoC FPGA.

Table 2-27 QSFP28 Pin Assignments, Schematic Signal Names, and Functions

Schematic Signal Name	Description	I/O Standard	Stratix 10 GX/SX Pin Number
QSFP28_TX_P0	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	PIN_BP1
QSFP28_TX_N0	Transmitter data of channel 0	HSSI DIFFERENTIAL I/O	PIN_BN2

QSFP28_RX_P0	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	PIN_BP7
QSFP28_RX_N0	Receiver data of channel 0	HSSI DIFFERENTIAL I/O	PIN_BN8
QSFP28_TX_P1	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	PIN_BR4
QSFP28_TX_N1	Transmitter data of channel 1	HSSI DIFFERENTIAL I/O	PIN_BT5
QSFP28_RX_P1	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	PIN_BR10
QSFP28_RX_N1	Receiver data of channel 1	HSSI DIFFERENTIAL I/O	PIN_BT11
QSFP28_TX_P2	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	PIN_BV1
QSFP28_TX_N2	Transmitter data of channel 2	HSSI DIFFERENTIAL I/O	PIN_BU2
QSFP28_RX_P2	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	PIN_BV7
QSFP28_RX_N2	Receiver data of channel 2	HSSI DIFFERENTIAL I/O	PIN_BU8
QSFP28_TX_P3	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	PIN_BW4
QSFP28_TX_N3	Transmitter data of channel 3	HSSI DIFFERENTIAL I/O	PIN_BY5

QSFP28_RX_P3	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	PIN_BW10
QSFP28_RX_N3	Receiver data of channel 3	HSSI DIFFERENTIAL I/O	PIN_BY11
QSFP28_REFCLK_p	QSFP28 transceiver reference clock p	LVDS	PIN_AJ12
QSFP28_REFCLK_n	QSFP28 transceiver reference clock n	LVDS	PIN_AH11
QSFP28_MOD_SEL_n	Module Select	3.0-V LVTTL	PIN_F19
QSFP28_RST_n	Module Reset	3.0-V LVTTL	PIN_J20
QSFP28_SCL	2-wire serial interface clock	3.0-V LVTTL	PIN_H19
QSFP28_SDA	2-wire serial interface data	3.0-V LVTTL	PIN_J22
QSFP28_LP_MODE	Low Power Mode	3.0-V LVTTL	PIN_G20
QSFP28_INTERRUPT_n	Interrupt	3.0-V LVTTL	PIN_H21
QSFP28_MOD_PRS_n	Module Present	3.0-V LVTTL	PIN_F21

Chapter 3

Dashboard GUI

The Apollo Agilex Dashboard GUI is a board management system. This system is connected from the Host to the system max on the Apollo Agilex board through the UART interface, and reads various status on the board. The reported status includes FPGA/Board temperature, fan speed, FPGA core power and 12V input power. **Figure 3-1** shows the block diagram of the Apollo Agilex Dashboard..

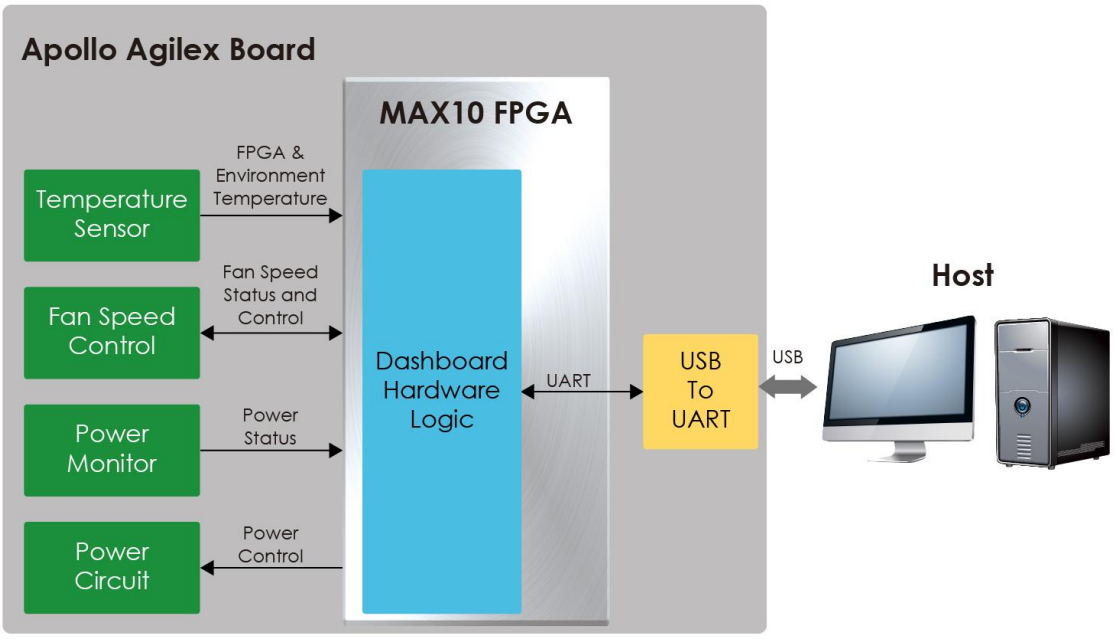

Figure 3-1 Block Diagram of the Apollo Agilex Dashboard

3.1 Setup for the Dashboard GUI

To use the dashboard system, users need to install the USB to UART driver on the host first, so that user can establish a connection with the Apollo Agilex board. This section will describe how to install USB to UART driver on the windows OS host.

■ Connection Setting

1. Connect the USB Mini USB connector of the Apollo Agilex board to the host PC USB port through mini USB cable.
2. Connect power to the Apollo Agilex board.
3. Power on the Apollo Agilex board.

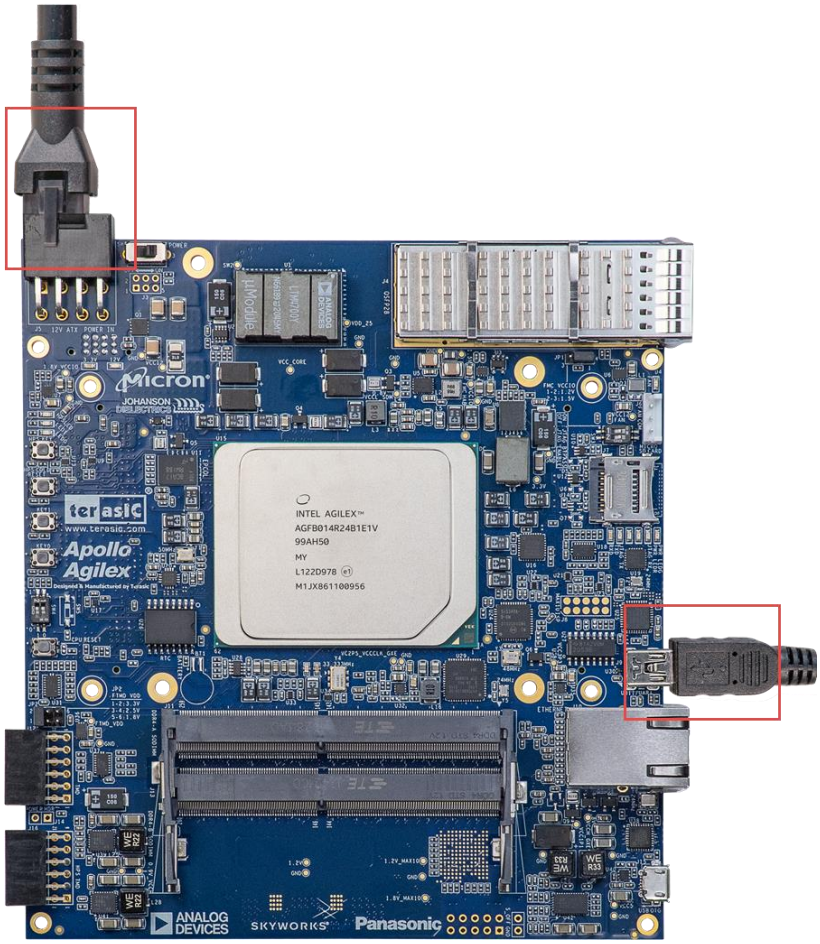

Figure 3-2 Connection setup for using dashboard system

■ Install Driver

Please refer to section **5.2** to install the driver the CP2105 which is the USB to UART port connected to the Dashboard GUI system.

3.2 Run Dashboard GUI

■ Dashboard GUI software location

Users can find it from the path: Tool\dashboard_gui\Dashboard.exe in the Apollo Agilex system CD and copy it to the host PC.

Execute the Dashboard.exe, a window will show as **Figure 3-3**. It will describe the detail functions as below.

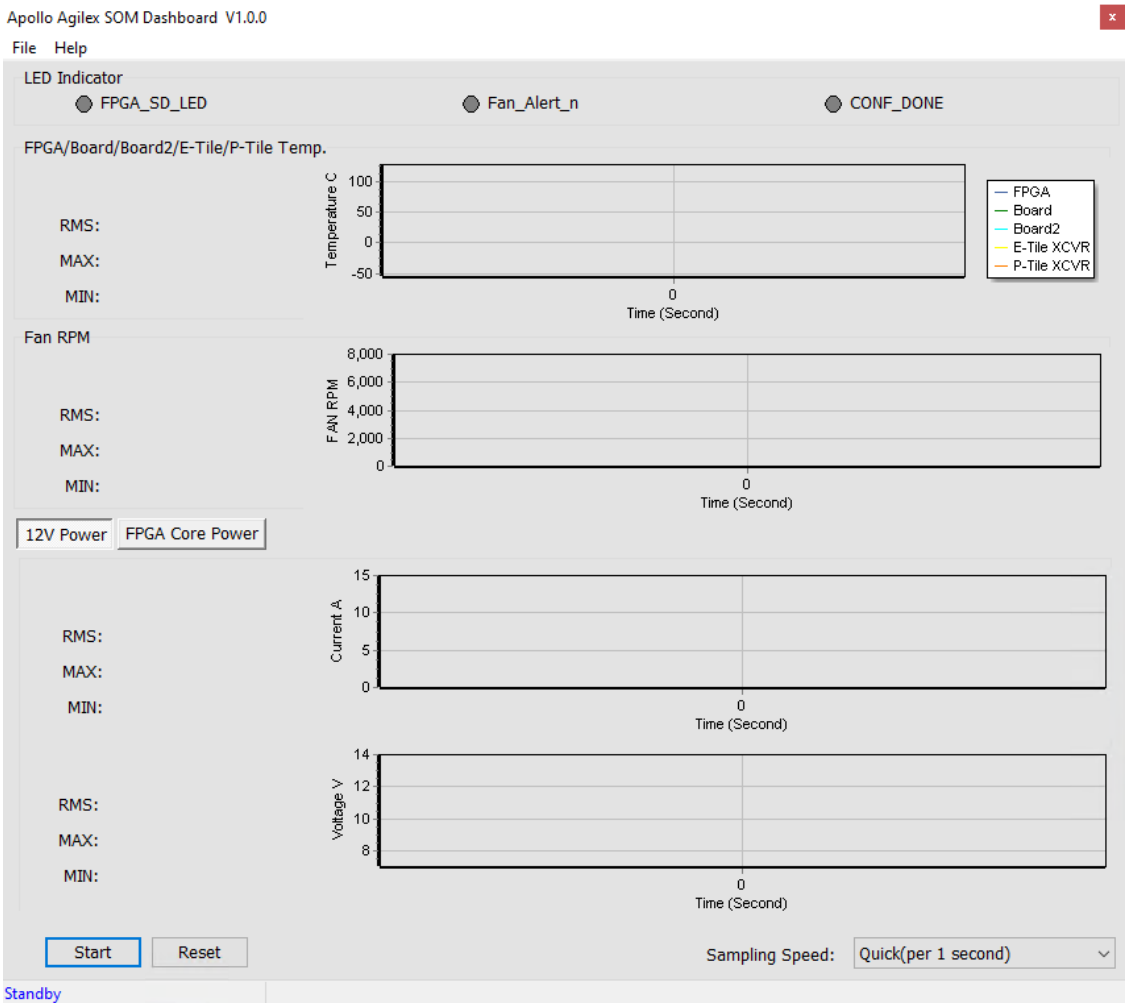

Figure 3-3 Dashboard GUI

■ Dashboard GUI function introduction

- **Start/Stop**: As shown in **Figure 3-4**, there is a Start button at the bottom-left of the GUI window. Click it to run the program (Start will change to Stop), it will show the Apollo Agilex board status. Users can press Stop button to stop the status data transmission and display.
- **Reset Button**: Press this button to clear the historical data shown in GUI, and

record the data again.

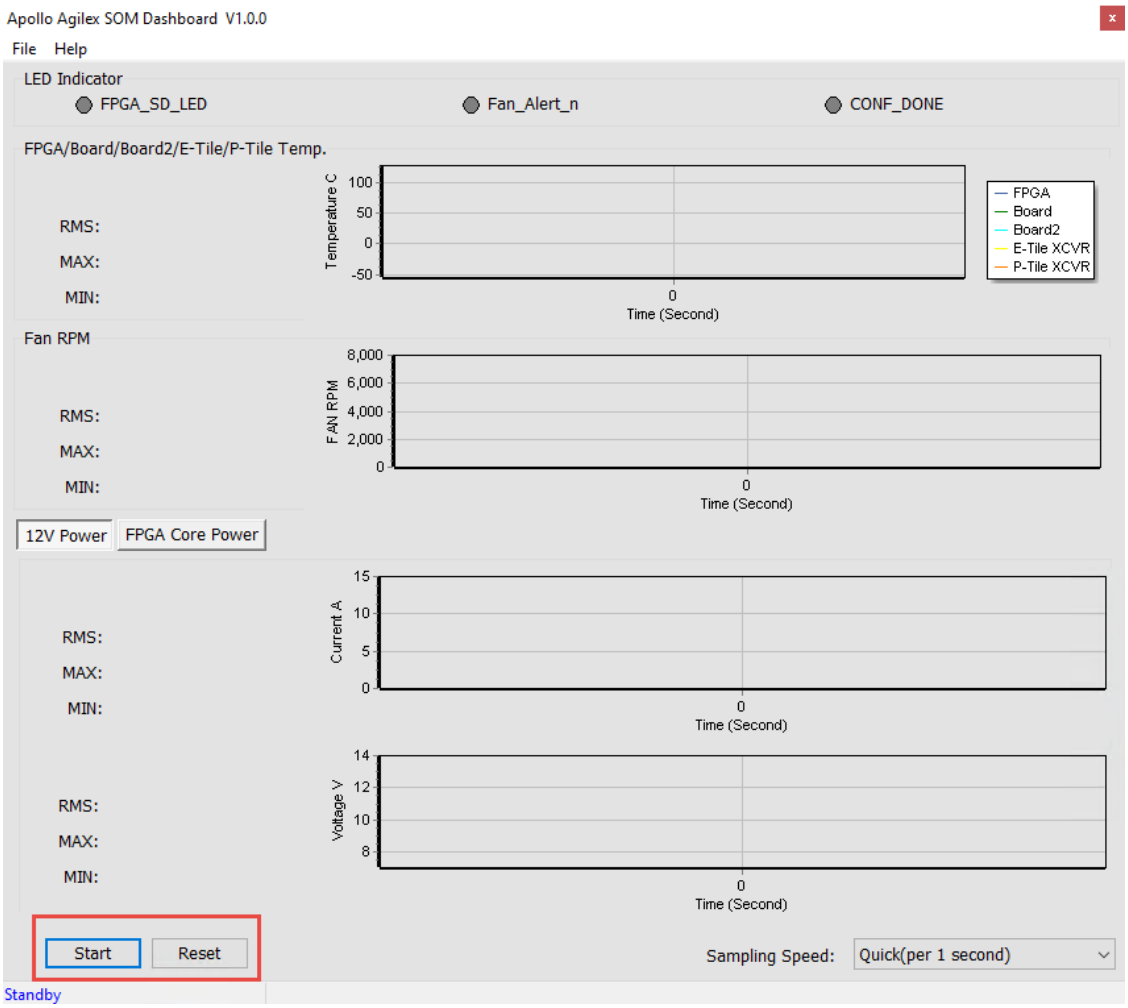

Figure 3-4 Start and Reset button

- **LED Indicator**:
  - **CONF_DONE** :As shown in **Figure 3-5**, once you press the “Start” button, it will show the status LED number on the Apollo Agilex board. For these LEDs function, please refer to section 2.2. Note that “**CONF_DONE**” stands for FPGA configure done status. There is no LED on Apollo Agilex board to display FPGA configure status. When this status is shown in green on the GUI, it means that FPGA configuration has been completed.
  - **Fan_Altert_n**: Illuminates when the fan is abnormal, such as when the fan speed is different from expected.
  - **FPGA_SD_LED:**

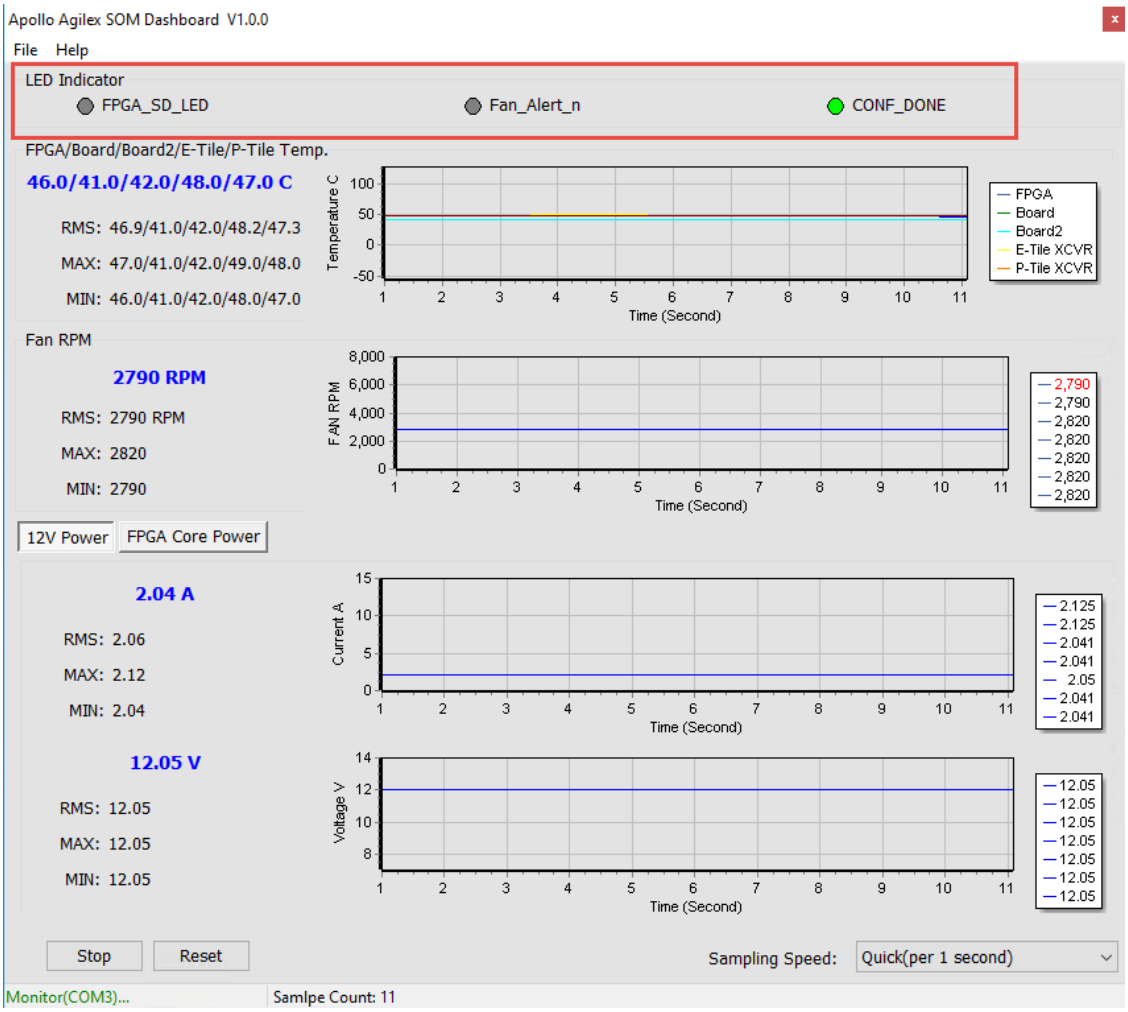

Figure 3-5 FPGA Status section

- **FPGA/Board/Transceivers(E-title and P-tile) Temperature**: The Dashboard GUI will real-time show the fan speed, Apollo Agilex board ambient and FPGA temperature. Users can know the board temperature in time. The information will be refreshed per 1 second, and displays through diagram and number, as shown in **Figure 3-6**.

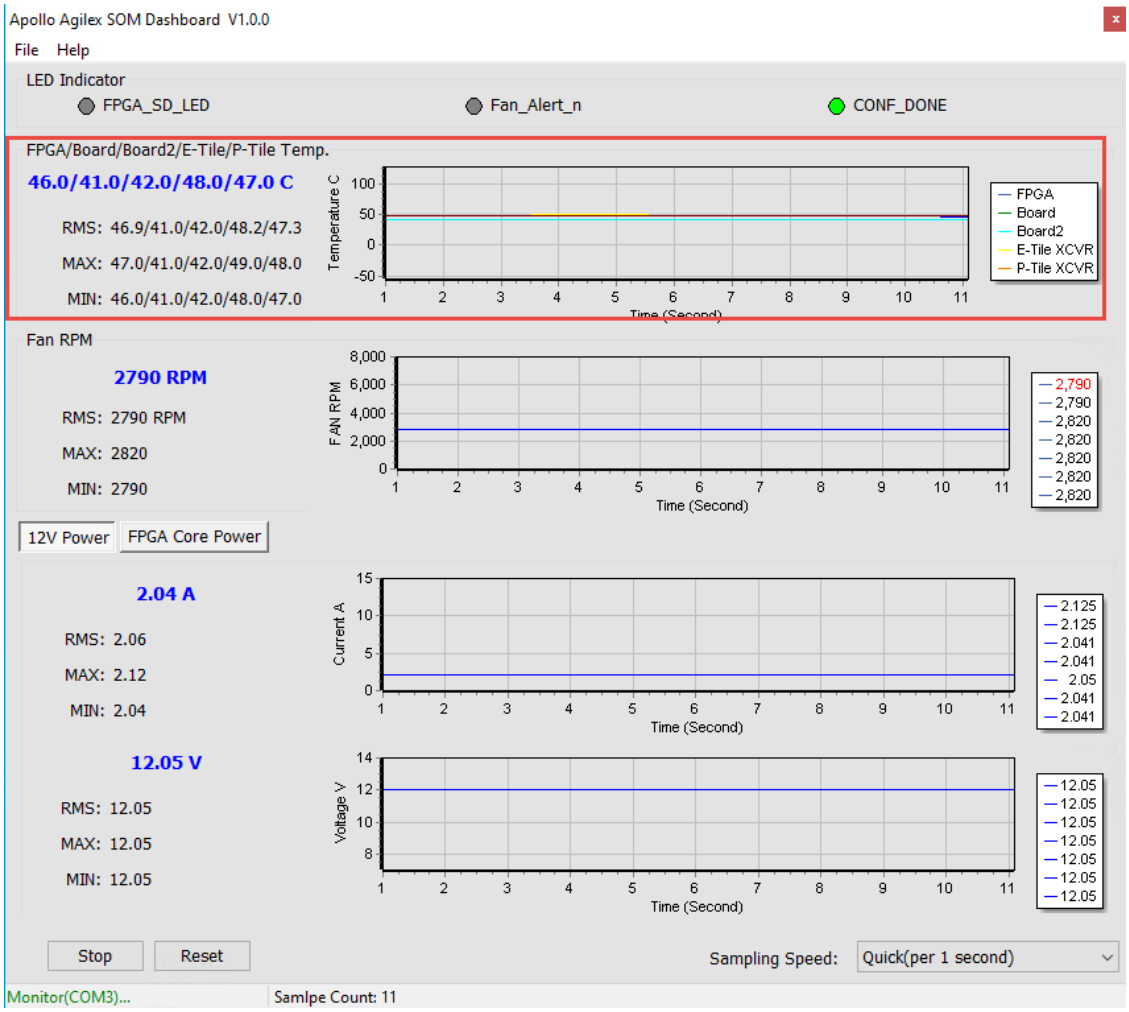

Figure 3-6 Temperature section

- **Fan RPM**: It displays the real-time speed of the fan on the Apollo Agilex board, as shown in **Figure 3-7**.

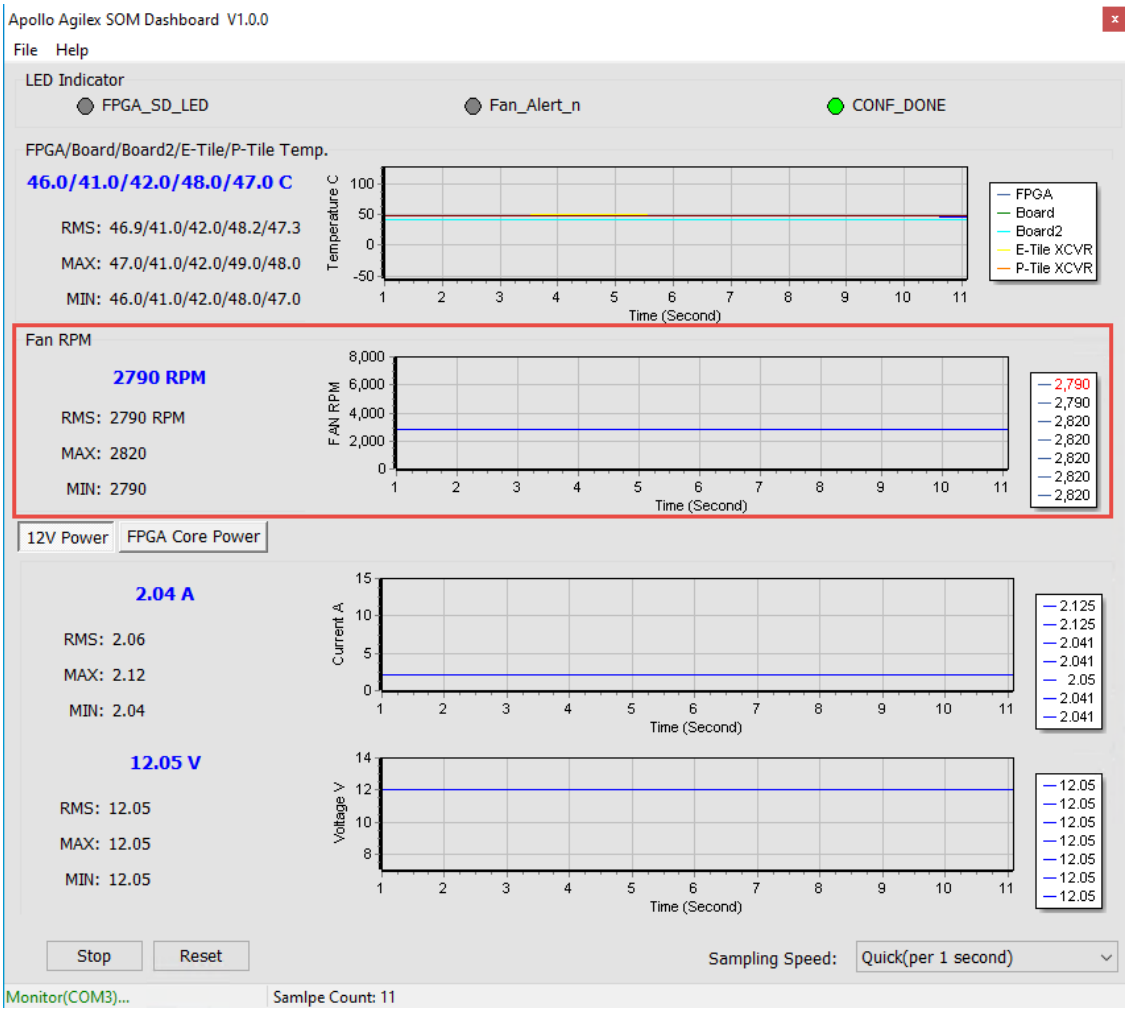

Figure 3-7 FAN RPM section

- **12V Power monitor**: It displays the real-time 12V Power voltage and consumption current on the Apollo Agilex board, as shown in **Figure 3-8**.

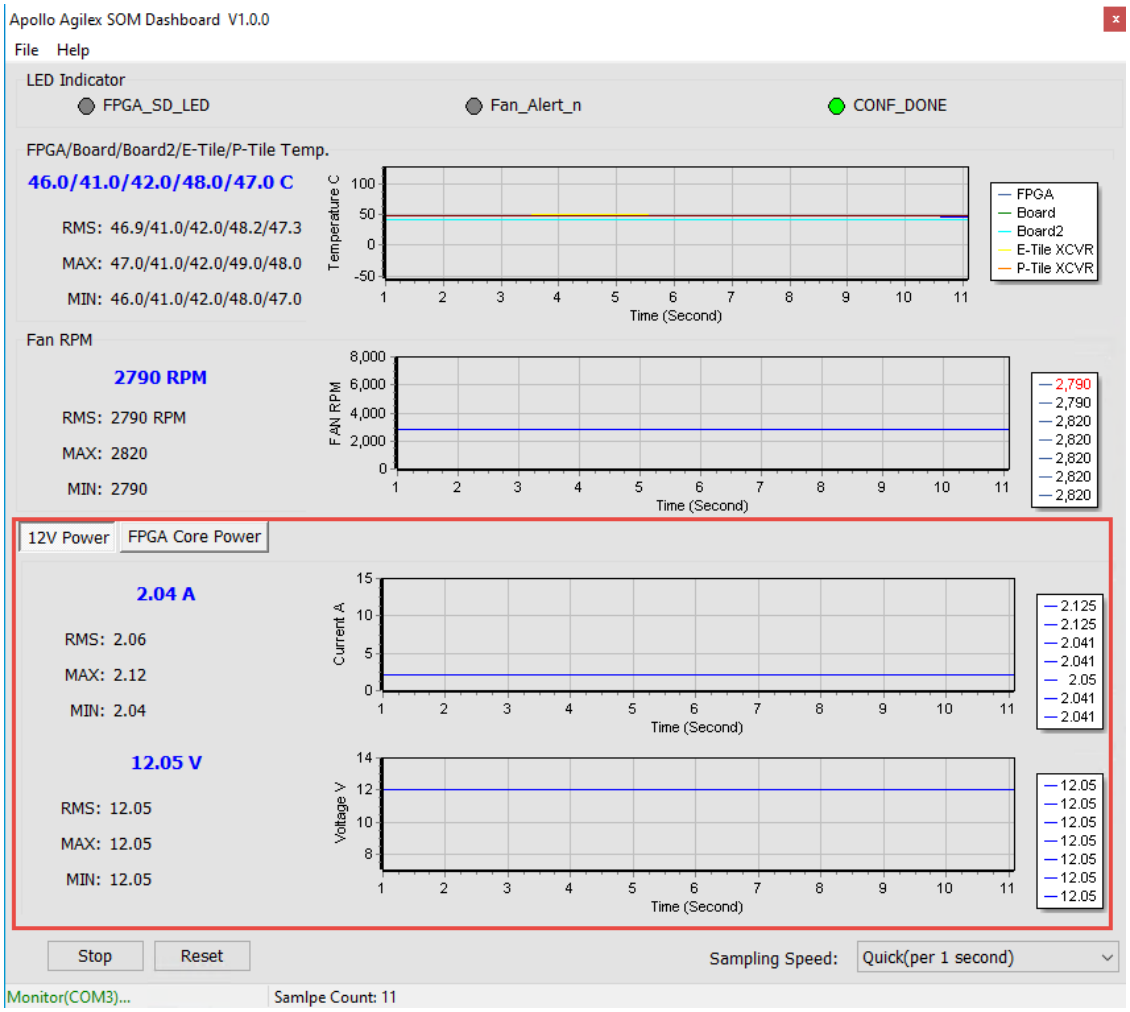

Figure 3-8 Power Monitor Section

- **Sampling Speed**: It can change interval time that the Dashboard GUI sample the board status. Users can adjust it to 1s/10s/1min/Full Speed (0.1s) to sample the board status, as shown in **Figure 3-9** and **Figure 3-10**.

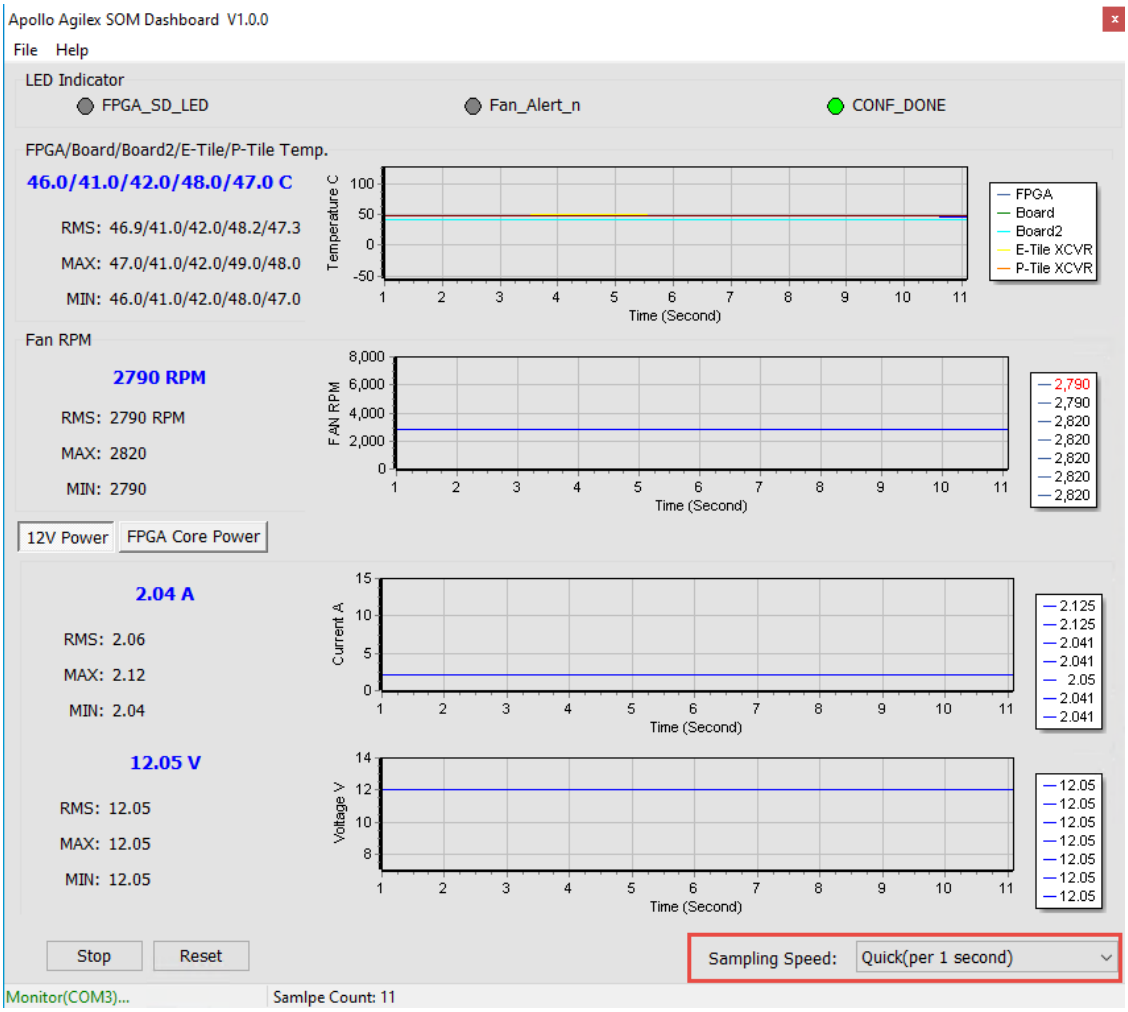

Figure 3-9 Sampling Speed section

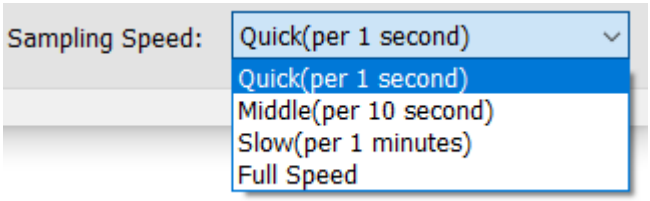

Figure 3-10 Options of Sampling Speed

- **Board Information**: There is a **File** page on the upper left of the Dashboard GUI program window, click the **Board Information** to get the current software version and the Apollo Agilex board version, as shown in **Figure 3-11**. Note, user needs to stop the system monitor (press the "**Stop**" button on the Dashboard GUI), then you can run the Board Information.

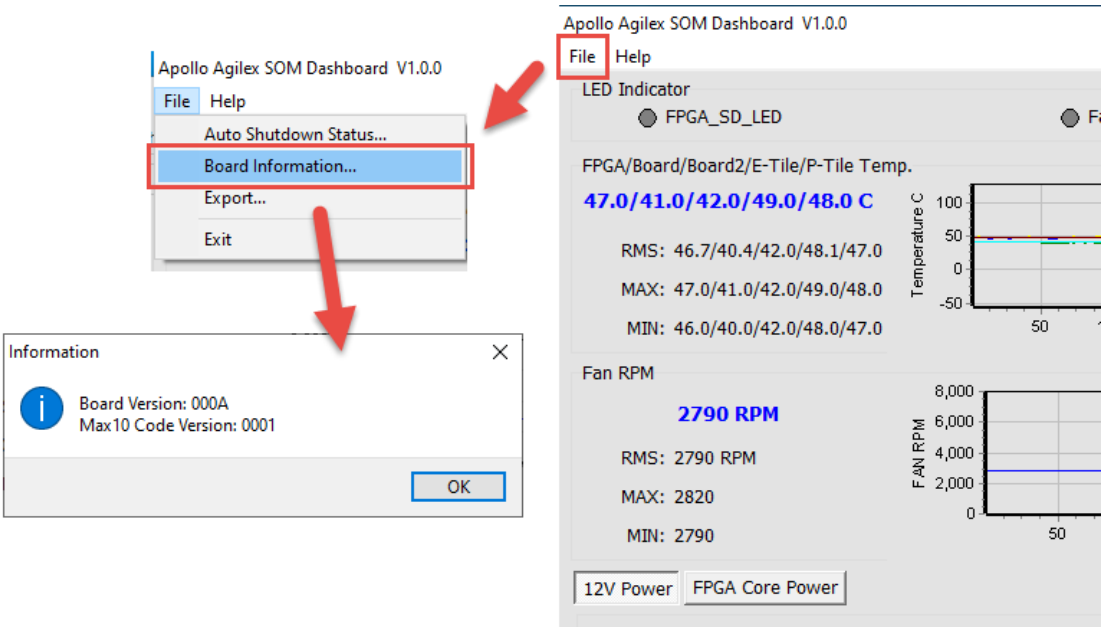

Figure 3-11 Board Information

- **Log File**: On the upper left of the Dashboard GUI program window, click the Export in the File page to save the board temperature, fan speed and voltage data in .csv format document, as shown in **Figure 3-12** and **Figure 3-13**.

Figure 3-12 Export the log file

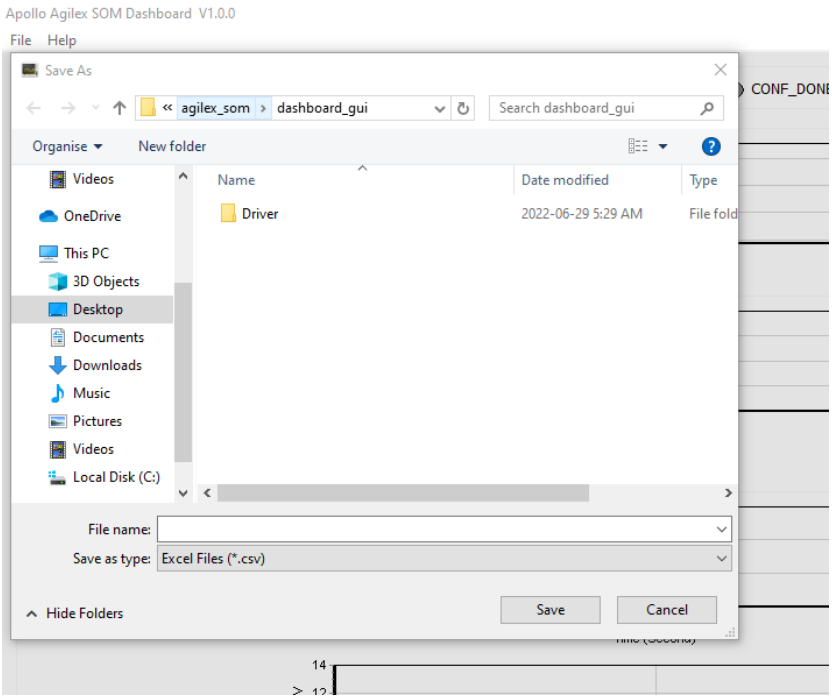

Figure 3-13 Export the log file in .csv format

Chapter 4

Transceiver Verification

This chapter describes how to verify the FPGA transceivers in the QSFP28 connector by using the test code provided in the Apollo Agilex board system CD.

4.1 Function of the Transceiver Test Code

The transceiver test code is used to verify the transceiver channels for the QSFP28 connector through an external loopback method. The transceiver channels are verified with PRBS31 test pattern and with the data rates at **25.8Gbps**.

4.2 Hardware Required

To enable an external loopback of the transceiver channels, QSFP28 loopback fixtures, as shown in **Figure 4-1**, are required. The fixture is available at: https://multilaneinc.com/product/ml4002-28/ .

Figure 4-1 QSFP28 Loopback Module

Figure 4-2 shows the FPGA board with four QSFP28 loopback module installed..

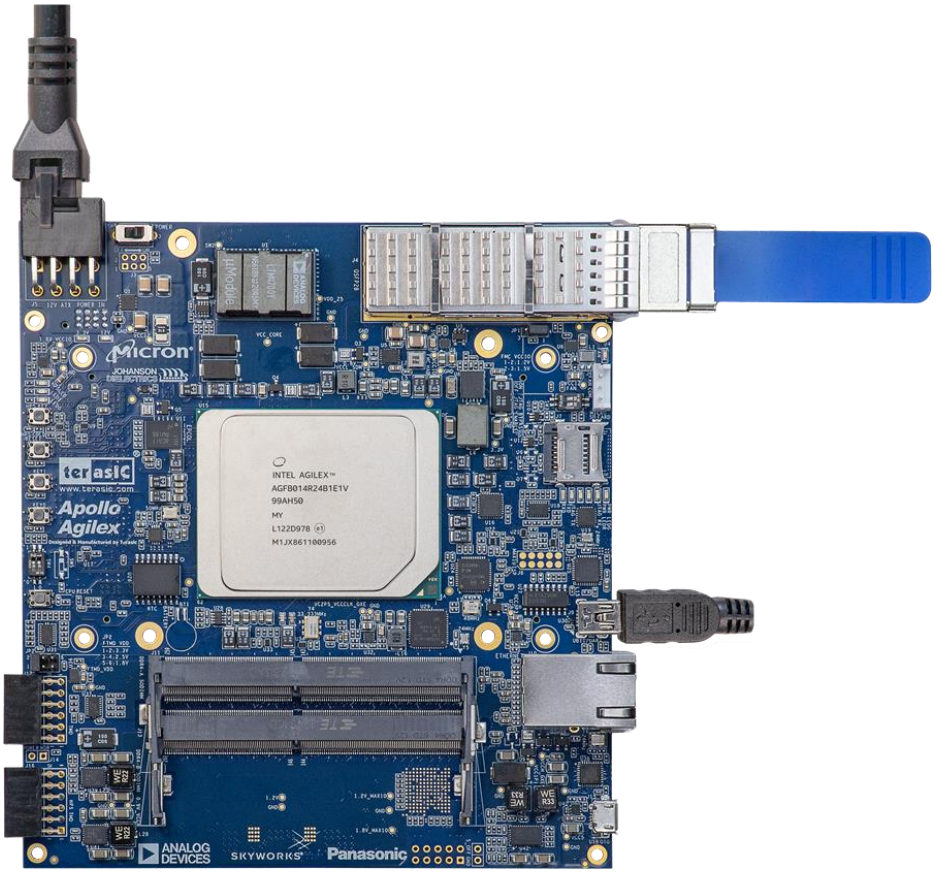

Figure 4-2 Test code setup

4.3 Execute the Test Code

The transceiver test code is available in the folder System CD\Tool\Transceiver_Test.

Here are the procedures to perform transceiver channel test:

1. Copy Transceiver_Test folder to your local disk.
2. Install the Windows Subsystem for Linux (WSL) on your windows for execute the demo batch file, please refer to the link below to install : http://www.terasic.com.tw/wiki/Getting_Start_Install_WSL

3. Make sure the power cable is not connected to the Apollo Agilex board.
4. Plug-in the QSFP28 loopback module on the QSFP28 connector of the Apollo Agilex board as shown in **Figure 4-2**.
5. Connect a USB cable to the Mini USB connector (J9) on the Apollo Agilex board and the Host Windows PC.
6. Power on the Apollo Agilex board.
7. Execute '**test.bat**" in the Transceiver_Test folder under your local disk.
8. The batch file will download .sof and .elf files, and start the test immediately. The test result is shown in the Nios-Terminal, as shown in **Figure 4-3**.
9. To terminate the test, press one of the KEY0 or KEY1 buttons on the FPGA board. The loopback test will terminate.

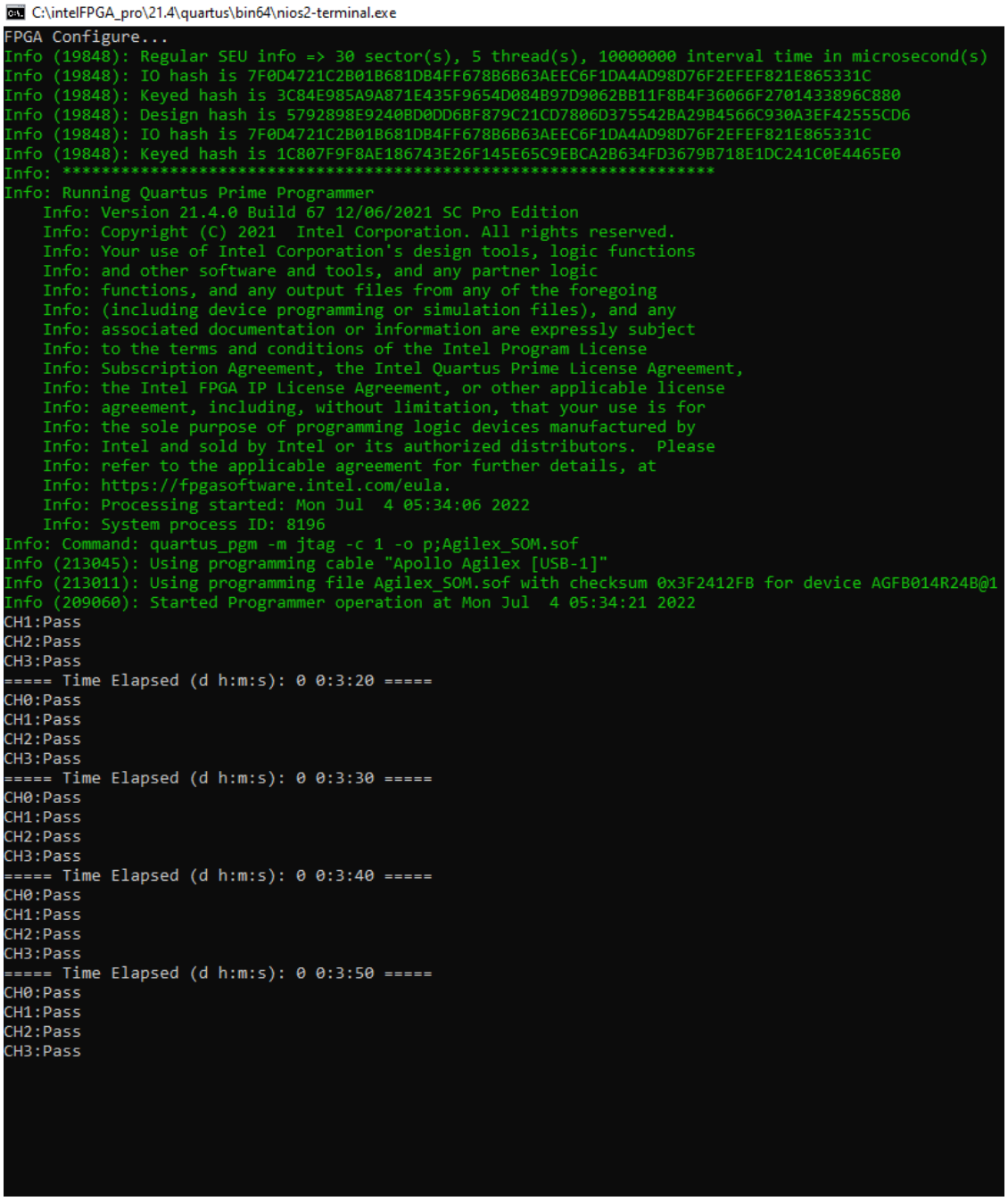

Figure 4-3 Test result

Chapter 5

Install Driver for the Board

5.1 Install the USB Blaster II Driver

The Apollo Agilex board equipped with an USB-Blaster II circuit, it interfaces a USB port on a host computer to an Agilex SoC FPGA on the board. The USB-Blaster II circuit sends configuration data from the PC via the JTAG interface to the FPGA. To use USB-Blaster II circuit, user need to install the driver on your operation system.

When user install the Quartus Prime software on your host, In the last step of the installation, the installer will ask whether to install the USB Blaster driver. If you click "yes", the driver should be installed automatically in your operation system (Windows). If you skip this step, you can also find the driver from the Quartus installation path after the Quartus installation is complete. The driver path is in *<Qaurtus Install Path>*\<*version*>*quartus**drivers**usb-blaster-ii* .

For linux users, please refer to this link to install : https://rocketboards.org/foswiki/Documentation/UsingUSBBlasterUnderLinux

5.2 Install USB to UART Driver

As described in Section 2.8 "**USB to UART**", the Apollo Agilex board has three USB to UART ports. They are implemented by a dual port to UART chip (CP2105) and a FT232R chip. The CP2105 is responsible for the UART channels of the FPGA and the system MAX 10, the FT232R for UART to USB for HPS. When the user connects the Mini USB cable to the Mini USB connector of the Apollo Agilex board, the "Device Manager" window on your Windows system should see three USB to UART devices as shown in the **Figure 5-1**. The chips corresponding to these com ports are as follows:

- CP2105: Standard and Enhanced COM Port
- FT232R: FT232R USB UART

The following content will introduce how to install the drivers of these two chips.

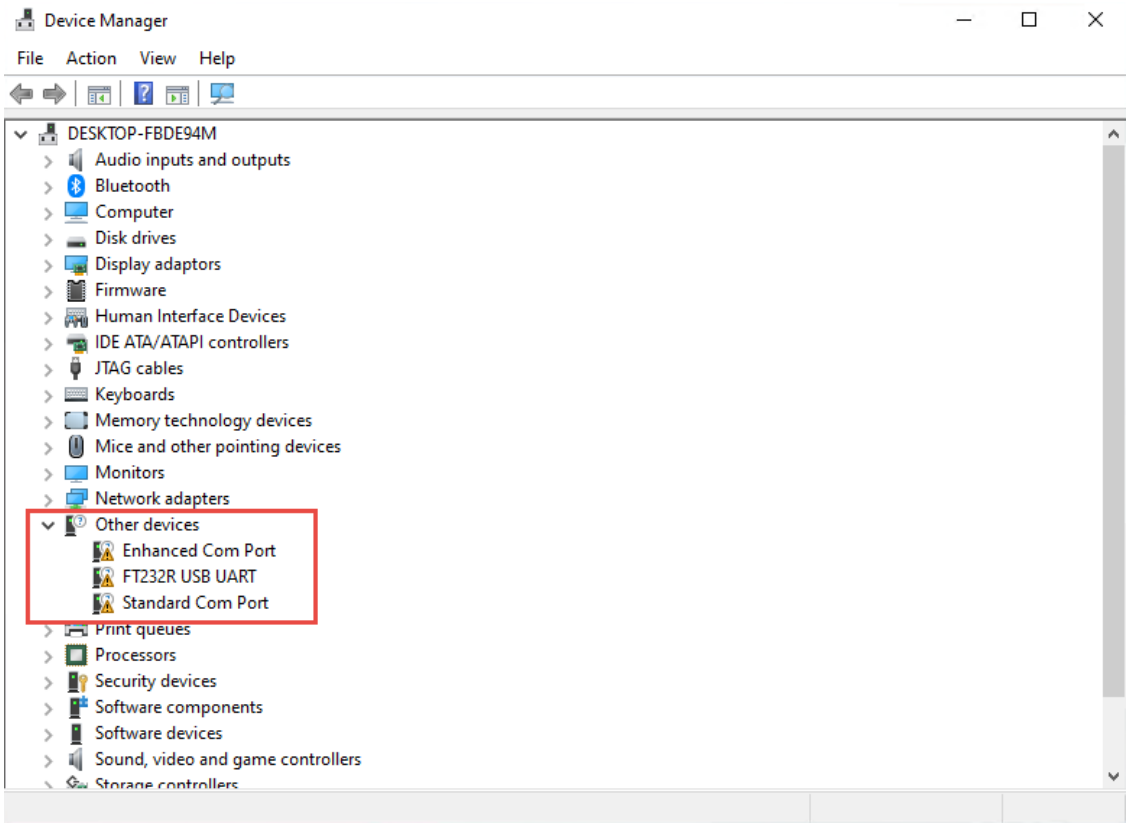

Figure 5-1 The USB to UART devices on the Device Manager

■ Install driver for CP2105

To install the driver for CP2105, users can find it from the path: *Tool\dashboard_gui\Driver* in the Apollo Agilex system CD and copy it to the host PC. User can also download the driver from manufacturer's download site. After the download is complete, select the driver suitable for your operating system and CPU version to start the installation as shown in **Figure 5-2** and **Figure 5-3**.

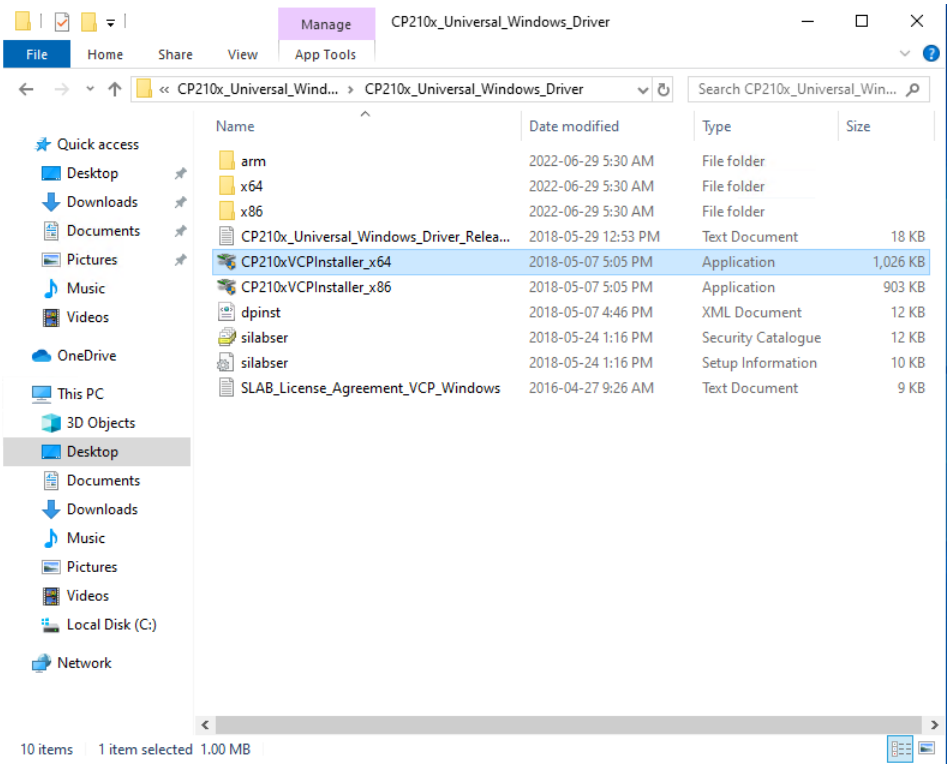

Figure 5-2 The driver for CP2105

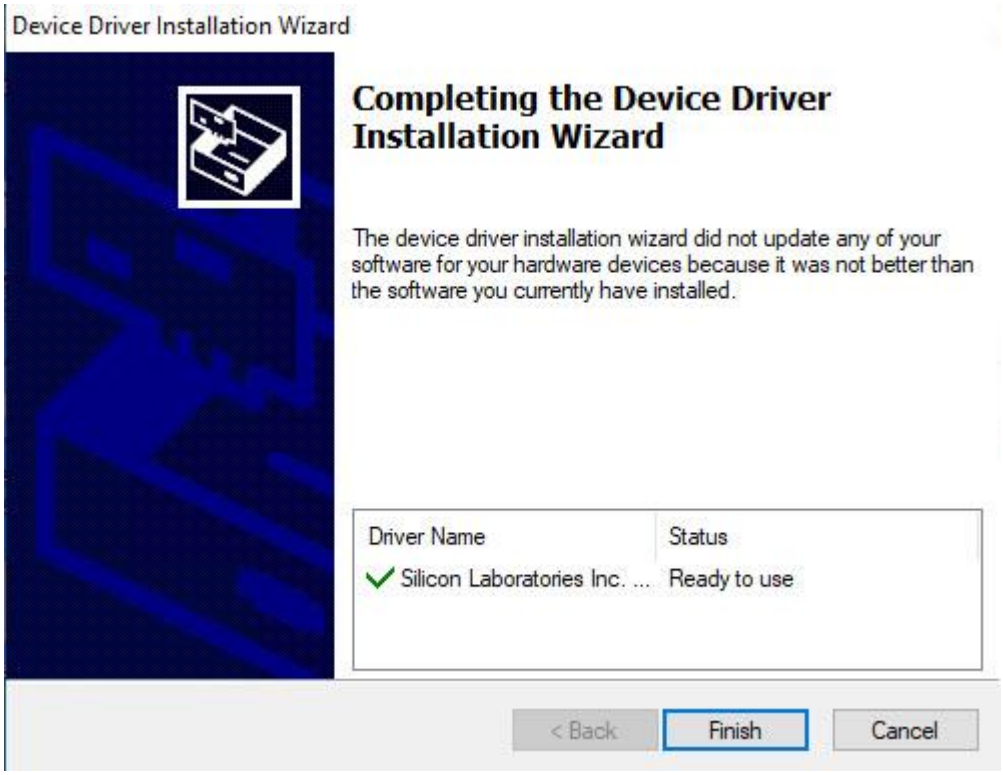

Figure 5-3 Completing device driver install

After the driver installation of CP2105 is completed, two USB to UART ports can be

seen in the “**Device Manager**” window in the Windows system of the user's computer. As shown in **Figure 5-4**, the **Enhanced** COM port is connected to the FPGA, and the **Standard** COM port is connected to the System MAX10. Note that the COM number (for example: COM3 and COM4) seen by each user should be different, because the hardware system of each user's computer is different

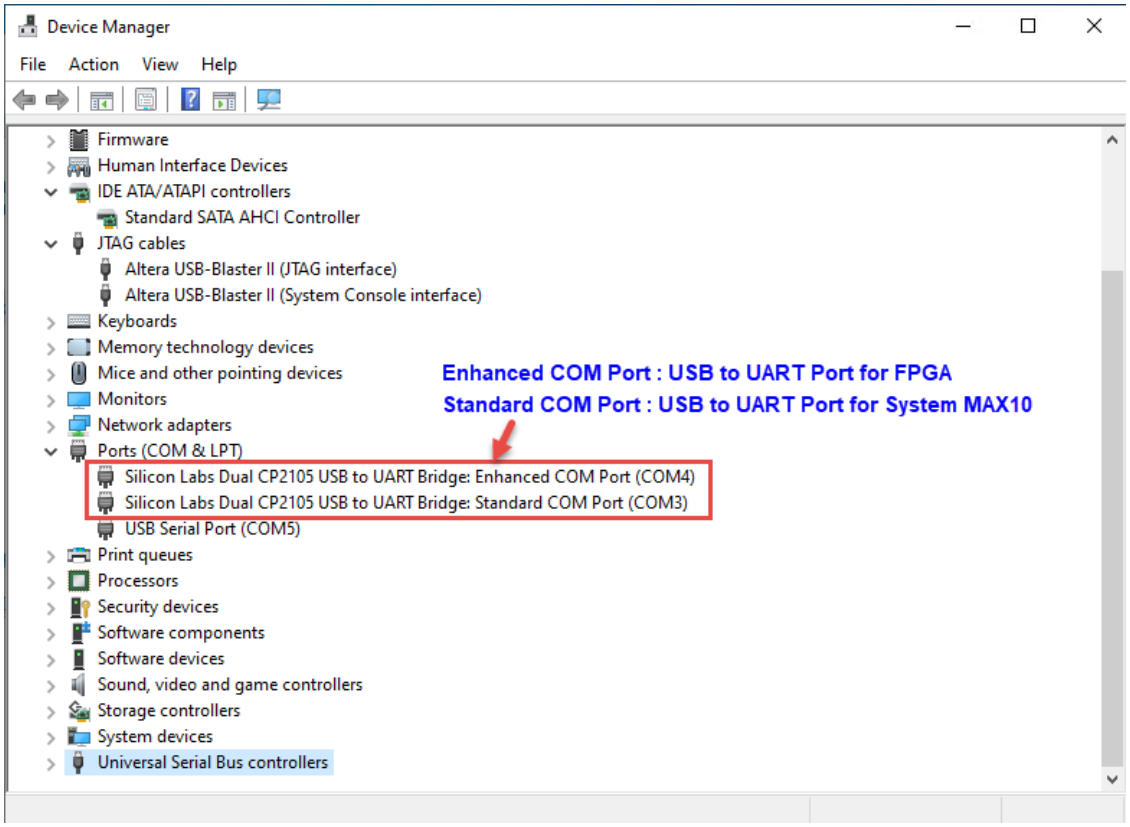

Figure 5-4 The CP2105 in the Device Manager

■ Install driver for FT232R

The FT232R chip is the USB to UART interface for HPS fabric. When the user's computer is connected to the Apollo Agilex board through the Mini USB cable for the first time, if the FT232R has no driver installed, the status on the “Device Manager” window will be as shown in **Figure 5-5**.

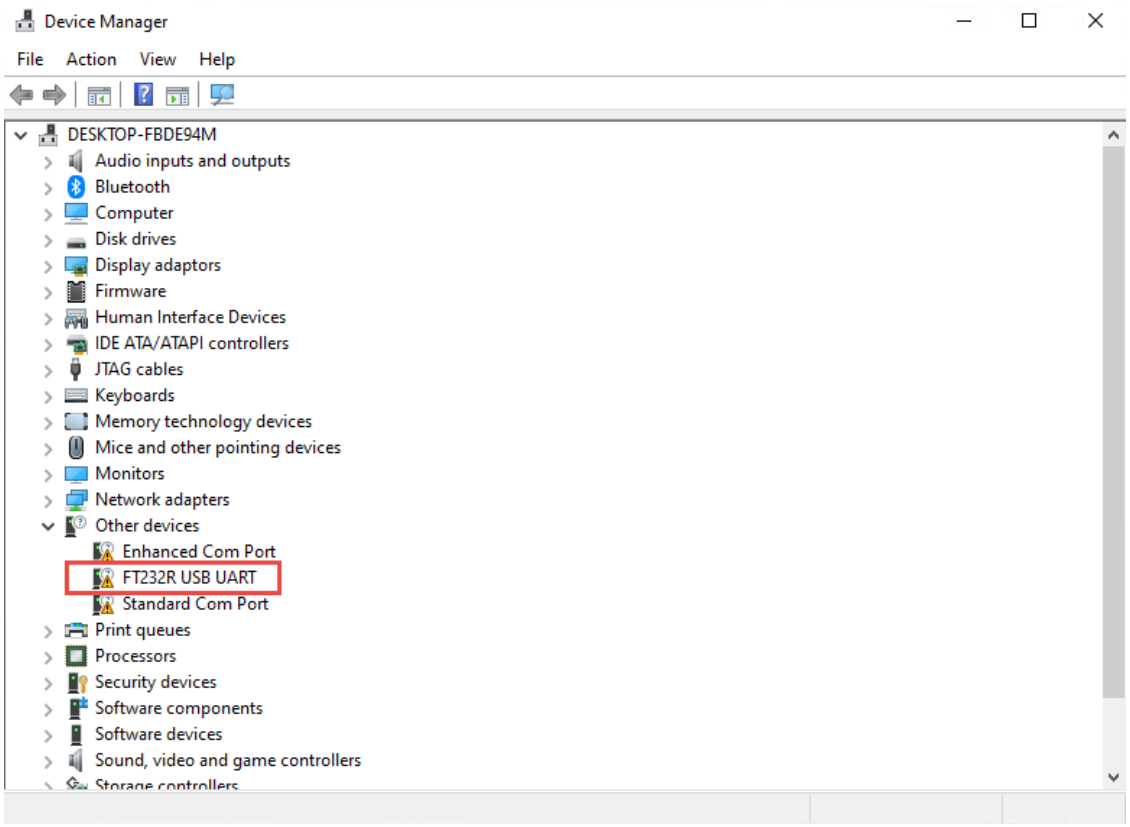

Figure 5-5 The FT232R in the Device Manager

Select the FT232R USB UART to update the driver software. The driver can be downloaded from http://www.ftdichip.com/Drivers/VCP.htm. Note, If the Windows operating system version of the user's computer is relatively new, sometimes Windows will automatically install this driver.

After the driver has been correctly installed, the USB Serial Port is recognized as a port such as COM5 (Open the Device Manager to know which COM port assigned in your computer).

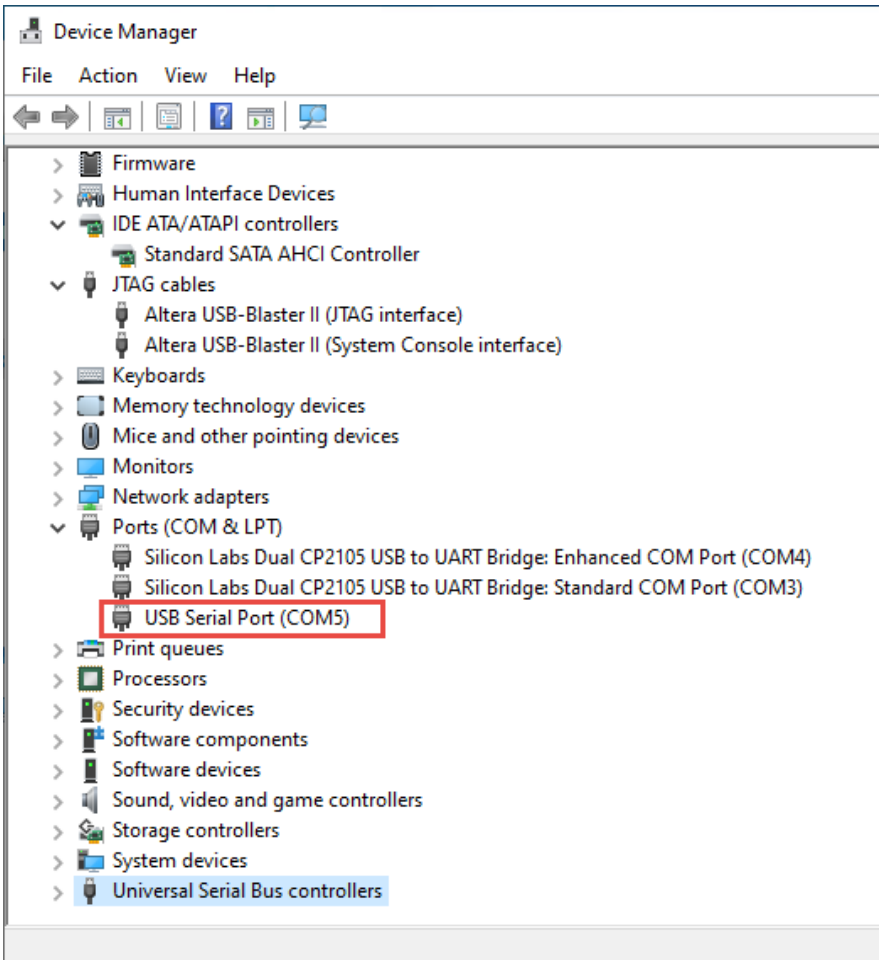

Figure 5-6 The USB to UART devices on the board

Chapter 6

Additional Information

6.1 Getting Help

Here are the addresses where you can get help if you encounter problems:

■ Terasic Technologies

No.80, Fenggong Rd., Hukou Township, Hsinchu County 303035. Taiwan

Email: support@terasic.com

Web: www.terasic.com

Apollo Agilex Web: agilex-som.terasic.com

■ Revision History

Date	Version	Changes
2022.07	First publication	
2022.08	V1.1	Modify section2.5