TC8220

Two-Pair N-Channel and P-Channel Enhancement-Mode MOSFET

Features

- High-voltage Vertical DMOS Technology
- Integrated Gate-to-source Resistor
- Integrated Gate-to-source Zener Diode
- Low Threshold, Low On-resistance
- Low Input and Output Capacitance
- Fast Switching Speeds
- Electrically Isolated N-channel and P-channel MOSFET Pairs

Applications

- High-voltage Pulsers
- Amplifiers
- Buffers
- Piezoelectric Transducer Drivers
- General Purpose Line Drivers
- Logic-level Interfaces

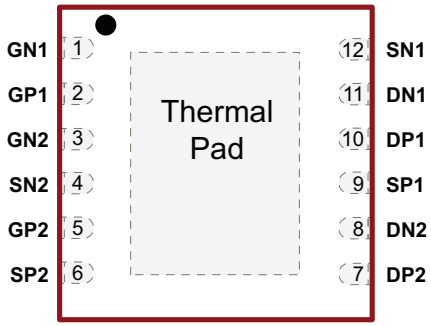
General Description

The TC8220 consists of six pairs of high-voltage, low-threshold N-channel and P-channel MOSFETs in a 12-lead DFN package. All MOSFETs have integrated the output drain high-voltage diodes, gate-to-source resistors, and gate-to-source Zener diode clamps which are desired for high-voltage pulser applications. The complimentary, high-speed, high-voltage, gate-clamped N-channel and P-channel MOSFET pairs utilize an advanced vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input and output capacitance, and fast switching speeds are desired.

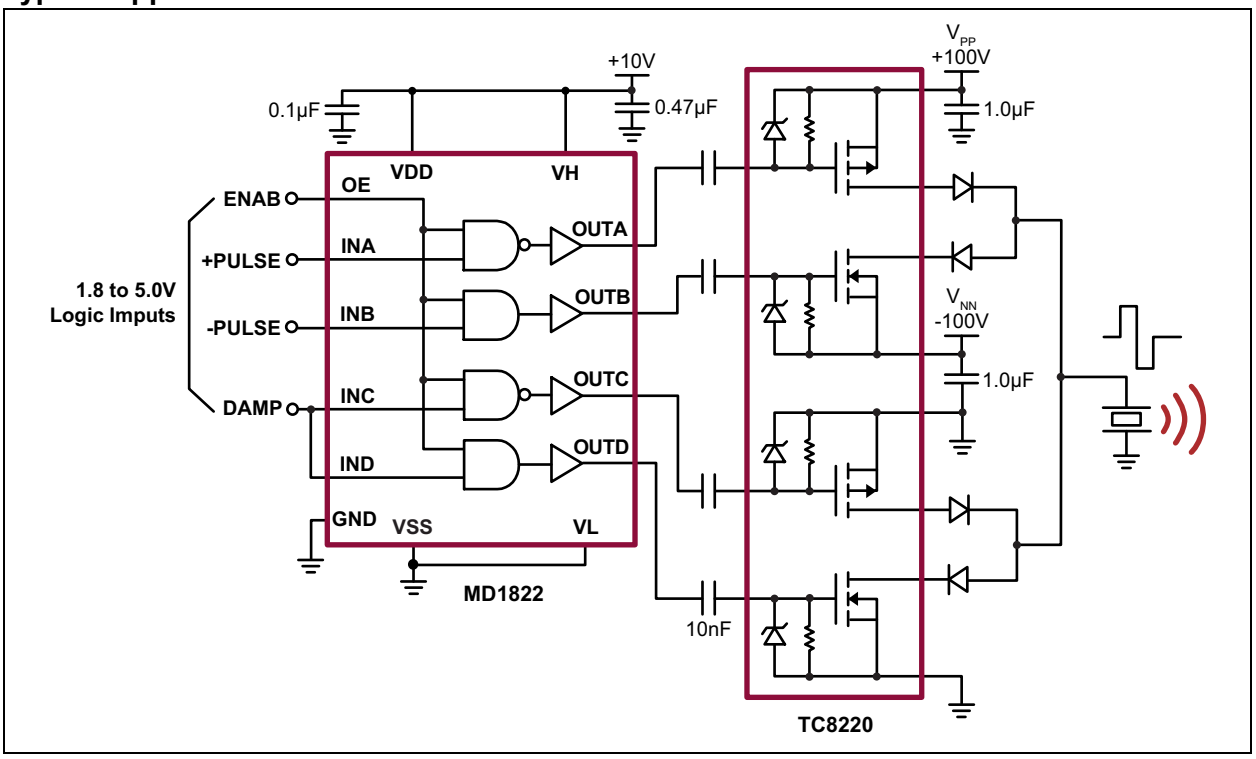
Package Type

12-lead DFN
(Top view)



See Table 2-1 for pin information.

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Operating Ambient Temperature, T_A .....–55°C to +150°C
Storage Temperature, T_S .....–55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1)						
Drain-to-Source Breakdown Voltage	BV_{DSS}	200	—	—	V	V_{GS} = 0V, I_D = 2 mA
Gate Threshold Voltage	$V_{GS(th)}$	1	—	2.4	V	V_{GS} = V_{DS}, I_D = 1 mA
Change in $V_{GS(th)}$ with Temperature (Note 2)	$\Delta V_{GS(th)}$	—	—	–4.5	mV/°C	V_{GS} = V_{DS}, I_D = 1 mA (Note 2)
Gate-to-Source Shunt Resistor	R_{GS}	10	—	50	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = 2 mA
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 2)
On-State Drain Current	$I_{D(ON)}$	1.3	—	—	A	V_{GS} = 5V, V_{DS} = 25V
		2.3	—	—		V_{GS} = 10V, V_{DS} = 50V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	6.5	Ω	V_{GS} = 5V, I_D = 150 mA
		—	—	6		V_{GS} = 10V, I_D = 1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1	%/°C	V_{GS} = 10V, I_D = 1A (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{DS} = 25V, I_D = 500 mA
Input Capacitance	C_{ISS}	—	56	—	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	13	—		
Reverse Transfer Capacitance	C_{RSS}	—	2	—		
Turn-On Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = 25V, I_D = 1A, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15		
Turn-Off Delay Time	$t_{d(OFF)}$	—	—	20		
Fall Time	t_f	—	—	15		
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	1.8	V	V_{GS} = 0V, I_{SD} = 500 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = 500 mA (Note 2)

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

P-CHANNEL ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
DC PARAMETER (Note 1)						
Drain-to-Source Breakdown Voltage	BV_{DSS}	–200	—	—	V	V_{GS} = 0V, I_D = –2 mA
Gate Threshold Voltage	$V_{GS(th)}$	–1	—	–2.4	V	V_{GS} = V_{DS}, I_D = –1 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	—	4.5	mV/°C	V_{GS} = V_{DS}, I_D = –1 mA (Note 2)
Gate-to-Source Shunt Resistor	R_{GS}	10	—	50	kΩ	I_{GS} = 100 µA
Gate-to-Source Zener Voltage	VZ_{GS}	13.2	—	25	V	I_{GS} = –2 mA
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	–10	µA	V_{DS} = Maximum rating, V_{GS} = 0V
		—	—	–1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (Note 2)
On-State Drain Current	$I_{D(ON)}$	–1.2	—	—	A	V_{GS} = –5V, V_{DS} = –25V
		–2.3	—	—		V_{GS} = –10V, V_{DS} = –50V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	—	8.5	Ω	V_{GS} = –5V, I_D = –150 mA
		—	—	7		V_{GS} = –10V, I_D = –1A
Change in $R_{DS(ON)}$ with Temperature	$\Delta_{RDS(ON)}$	—	—	1	%/°C	V_{GS} = –10V, I_D = –1A (Note 2)
AC PARAMETER (Note 2)						
Forward Transconductance	G_{FS}	400	—	—	mmho	V_{DS} = –25V, I_D = –500 mA
Input Capacitance	C_{ISS}	—	75	—	pF	V_{GS} = 0V, V_{DS} = –25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	21	—		
Reverse Transfer Capacitance	C_{RSS}	—	6.5	—		
Turn-on Delay Time	$t_{d(ON)}$	—	—	10	ns	V_{DD} = –25V, I_D = –1A, R_{GEN} = 25Ω
Rise Time	t_r	—	—	15		
Turn-on Delay Time	$t_{d(OFF)}$	—	—	20		
Fall Time	t_f	—	—	15		
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	–1.8	V	V_{GS} = 0V, I_{SD} = –500 mA (Note 1)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = –500 mA (Note 2)

Note 1: Unless otherwise stated, all DC parameters are 100% tested and at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

2: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
12-lead DFN	θ_{JA}	—	42	—	°C/W	Note 1

Note 1: 1 oz, 4-layer, 3” x 4” PCB

2.0 PIN DESCRIPTION

Table 2-1 shows the description of pins in TC8220.
Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	GN1	Gate of N-MOSFET 1
2	GP1	Gate of P-MOSFET 1
3	GN2	Gate of N-MOSFET 2
4	SN2	Source of N-MOSFET 2
5	GP2	Gate of P-MOSFET 2
6	SP2	Source of P-MOSFET 2
7	DP2	Drain of P-MOSFET 2
8	DN2	Drain of N-MOSFET 2
9	SP1	Source of P-MOSFET 1
10	DP1	Drain of P-MOSFET 1
11	DN1	Drain of N-MOSFET 1
12	SN1	Source of N-MOSFET 1
Thermal pad		Die attachment substrate, must be grounded externally. Thermal pad must be grounded.

3.0 FUNCTIONAL DESCRIPTION

Figure 3-1 and Figure 3-2 illustrate the switching waveforms and test circuits for TC8220.

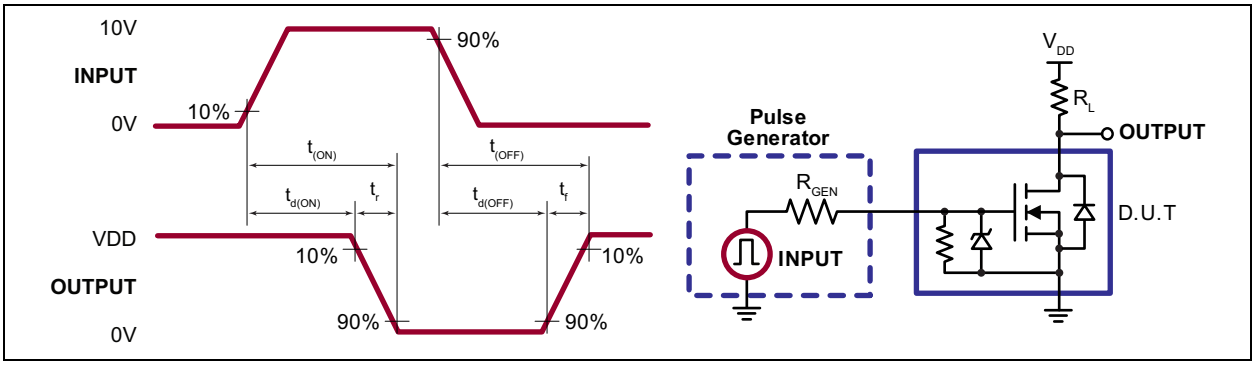


FIGURE 3-1: *N-channel Switching Waveforms and Test Circuit.*

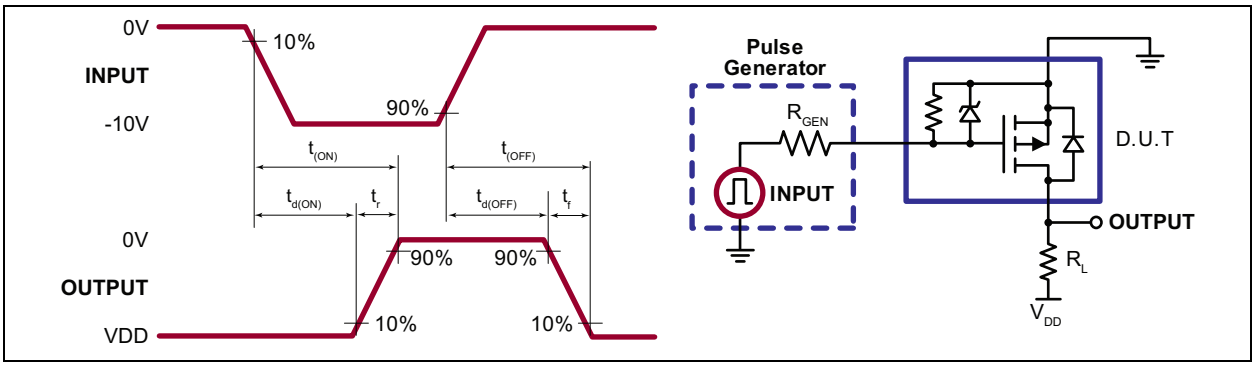


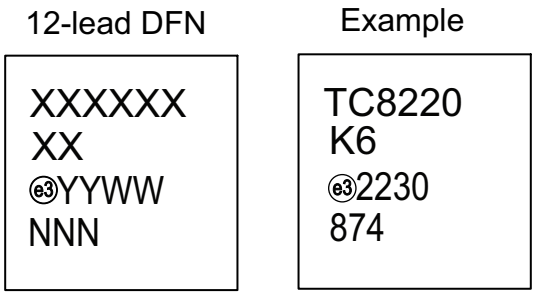
FIGURE 3-2: *P-channel Switching Waveforms and Test Circuit.*

TABLE 3-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)		$R_{DS(ON)}$ (Maximum) (Ω)	
N-Channel	**P-Channel**	**N-Channel**	**P-Channel**
200	–200	5.3	6.5

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

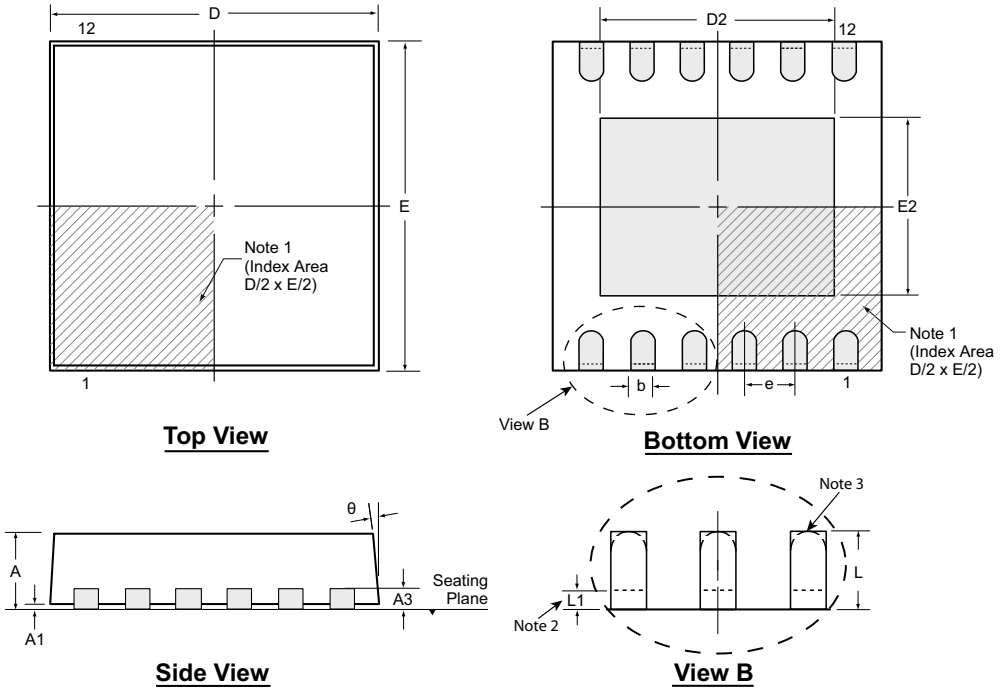


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

12-Lead DFN Package Outline (K6)

4.00x4.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	3.85	3.19	3.85	2.29	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02		0.25	4.00	3.34	4.00	2.44		0.40	-	-
	MAX	1.00	0.05		0.30	4.15	3.44	4.15	2.54		0.50	0.15	14°

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (August 2022)

- Converted Supertex Doc# DSFP-TC8220 to Microchip DS20005786A
- Changed the package marking format
- Changed the quantity of the 12-lead DFN K6 package from 3000/Reel to 3300/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	TC8220	=	Two-Pair N-Channel and P-Channel Enhancement-Mode MOSFET
Package:	K6	=	12-lead DFN
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for a K6 Package

Example:

a) TC8220K6-G:	Two-Pair N-Channel and P-Channel Enhancement-Mode MOSFET, 12-lead DFN, 3300/Reel

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