

B0546-SCH-01

RD1-4020 -- VEGA STDP4020 (DPRx to Dual-Link DVI) Reference Design

PCB# 400-530

### Revision History

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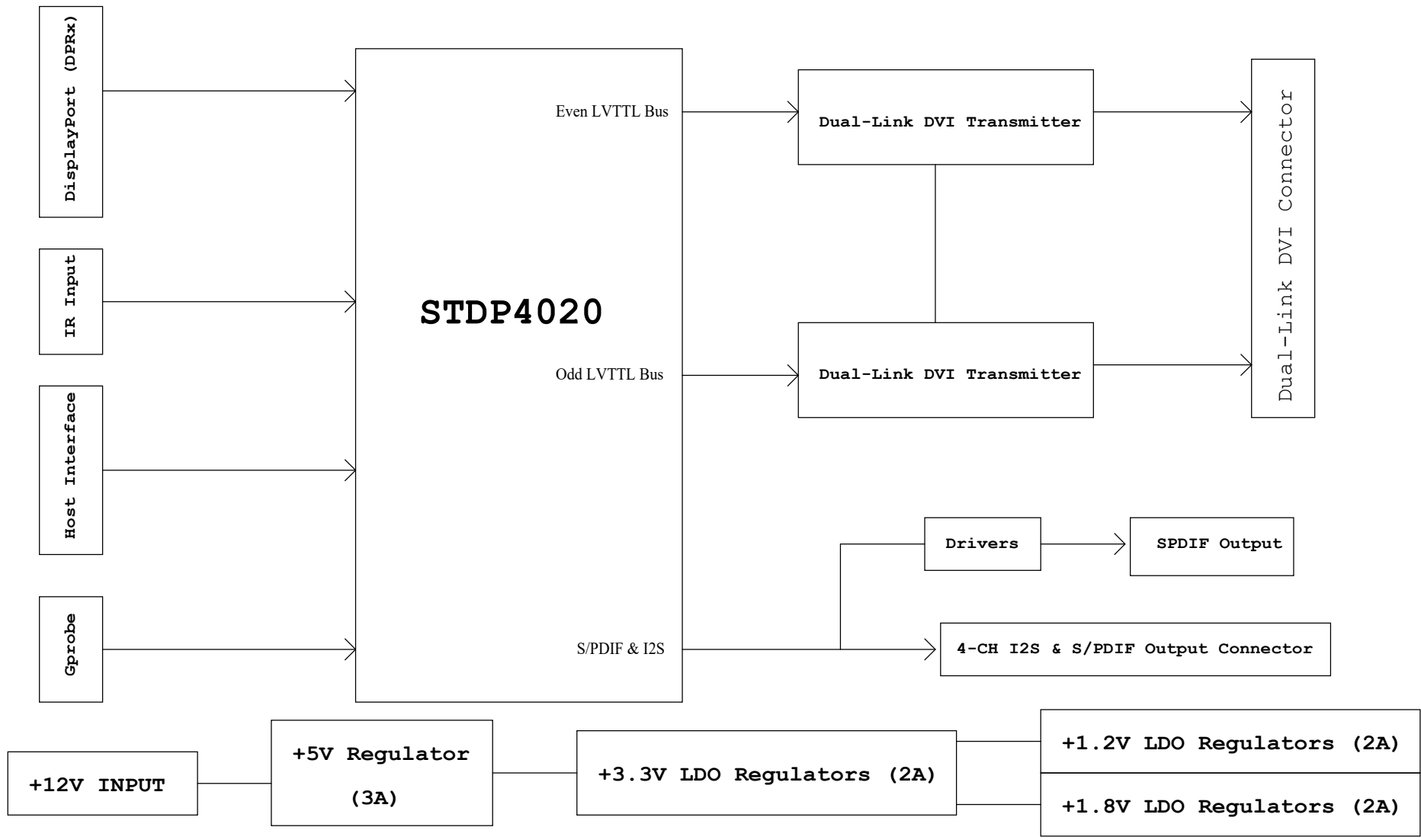
Date	Version	Comments
Sept. 12, 2009	Rev. A	Initial schematic.
Jan. 12, 2009	Rev. A1	DNP Q701, D701 and Related
June 8, 2010	Rev. B	Removed Q701, D701 and Related Added ASSR Enable/Disable BootStrap
July 12, 2011	Rev. C	Revised BootStaps default settings.
Sept 26, 2014	Rev. C	Changed Titleblock and logo to MegaChips.
March 13, 2020	Rev. 03a	Update to Kinetic format.

#### Layout Notes:

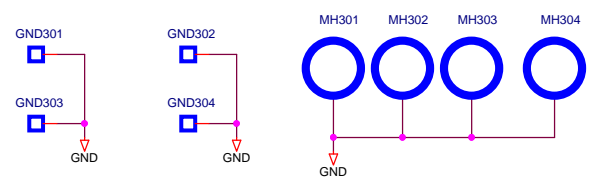
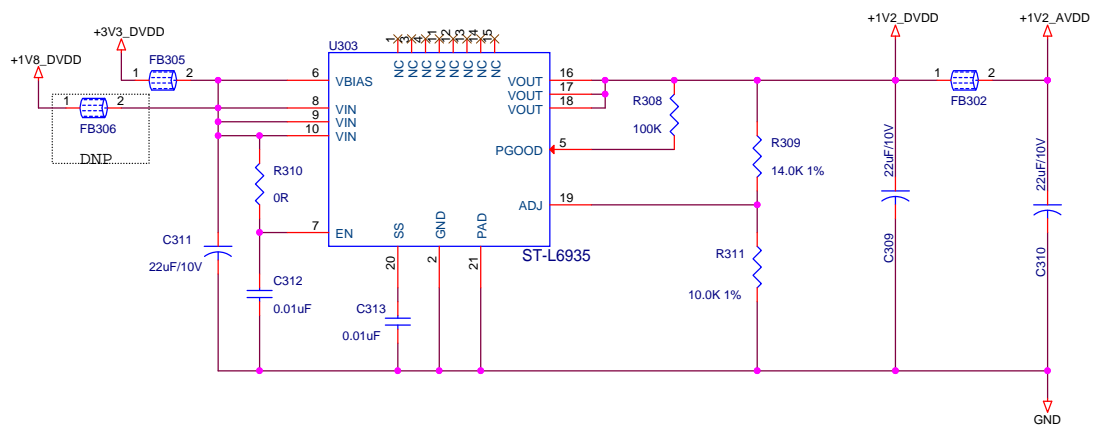
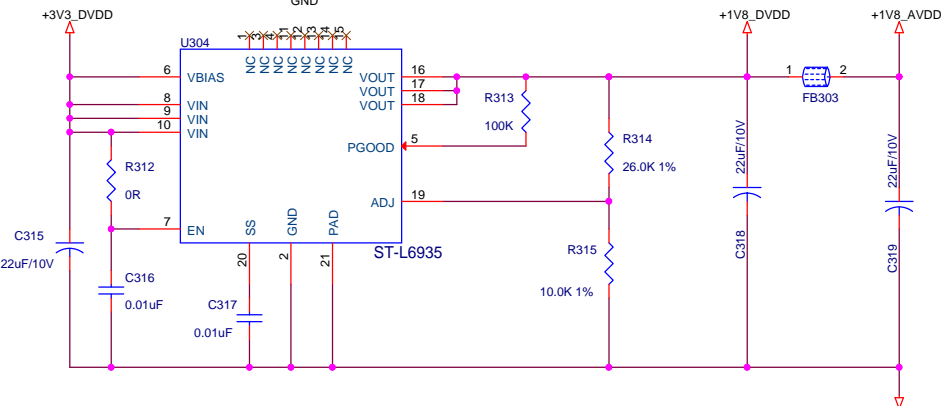
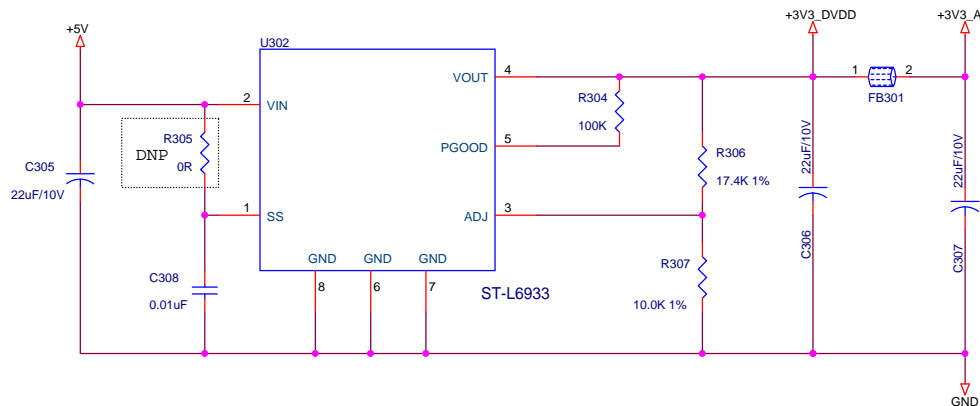
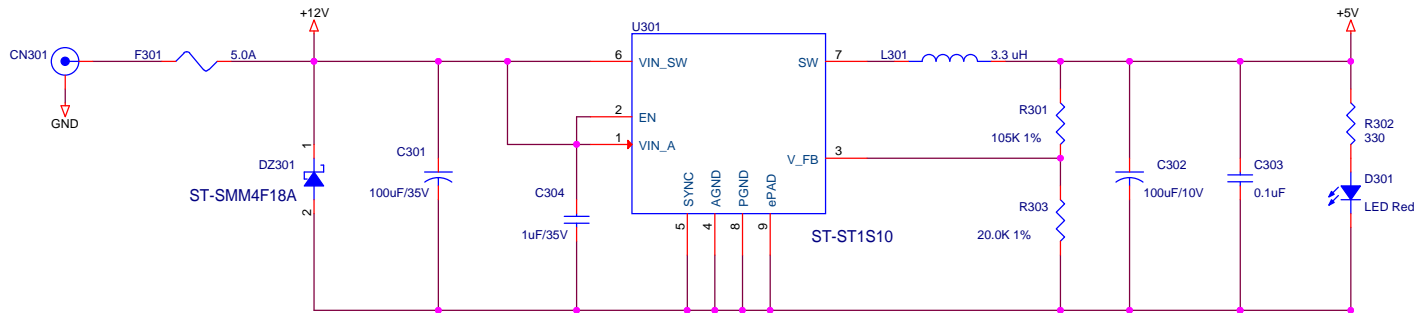
1. 50 ohms impedance on all LVTTTL traces
2. 100 ohms differential impedance on all DP & LVDS trace pairs
2. 4 Layers PCB, \*\*\* Top, GND, PWR, Bottom \*\*\* ,THK = 0.062 inches



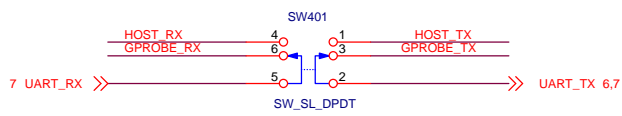
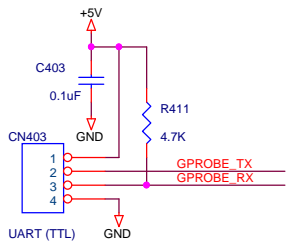
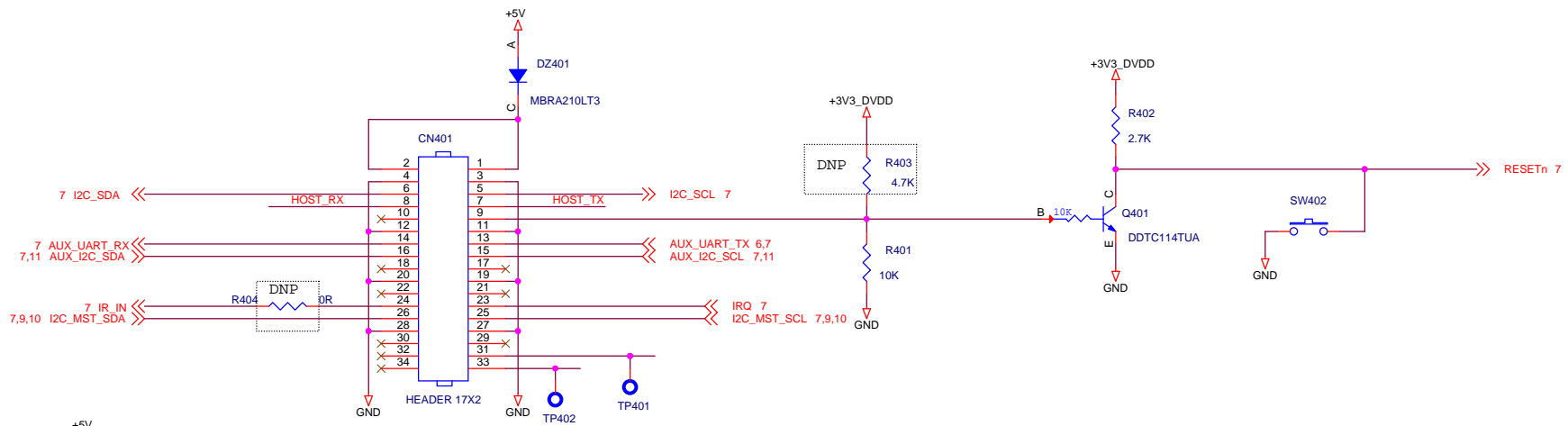
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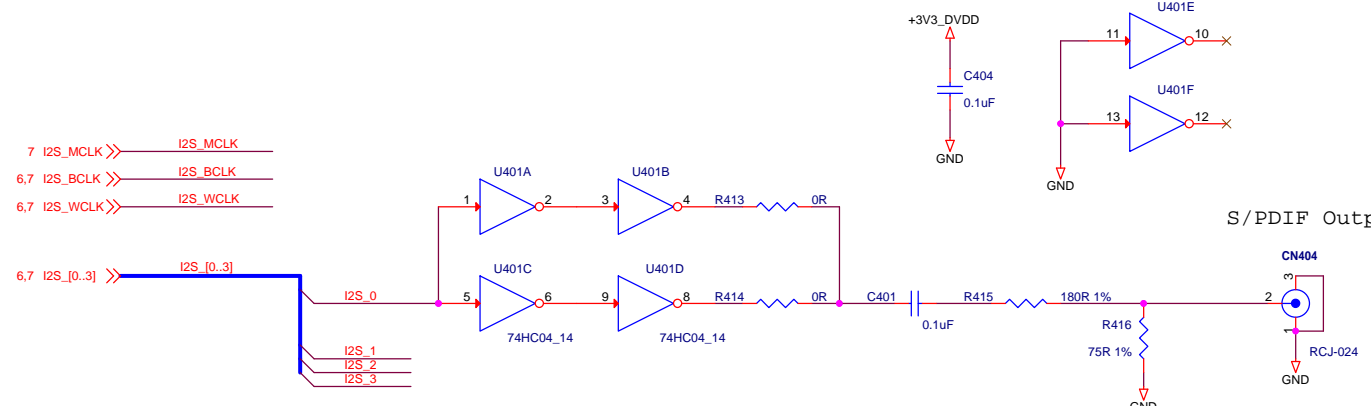
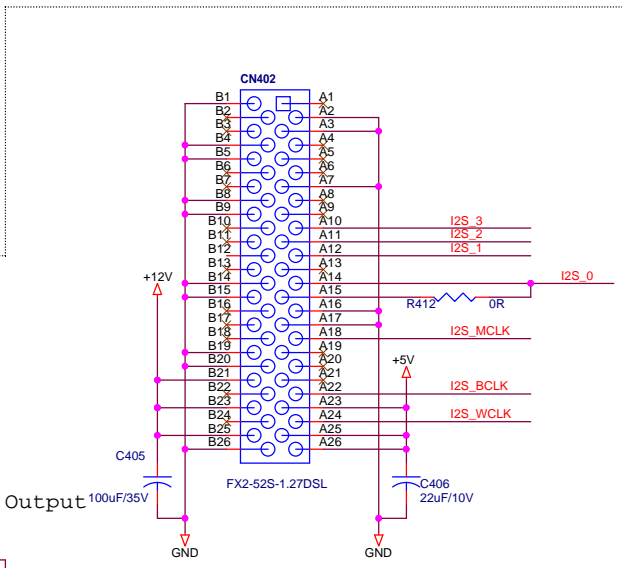
<b>kinetic technologies</b>		
Title		
<b>02. Overview</b>		
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<b>Title</b> 03. Power Supply, Fixed +5V, Adj. +3.3V & Adj. +1.2V		
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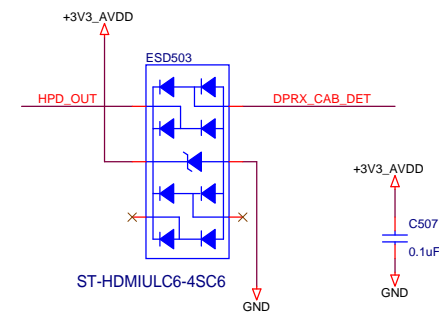
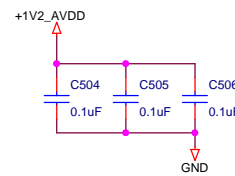
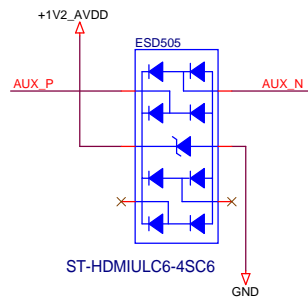
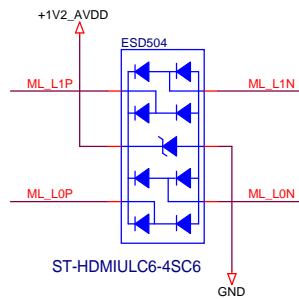
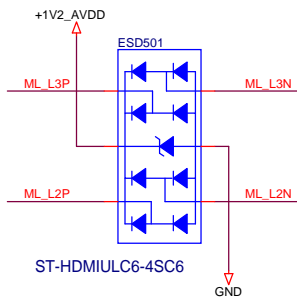
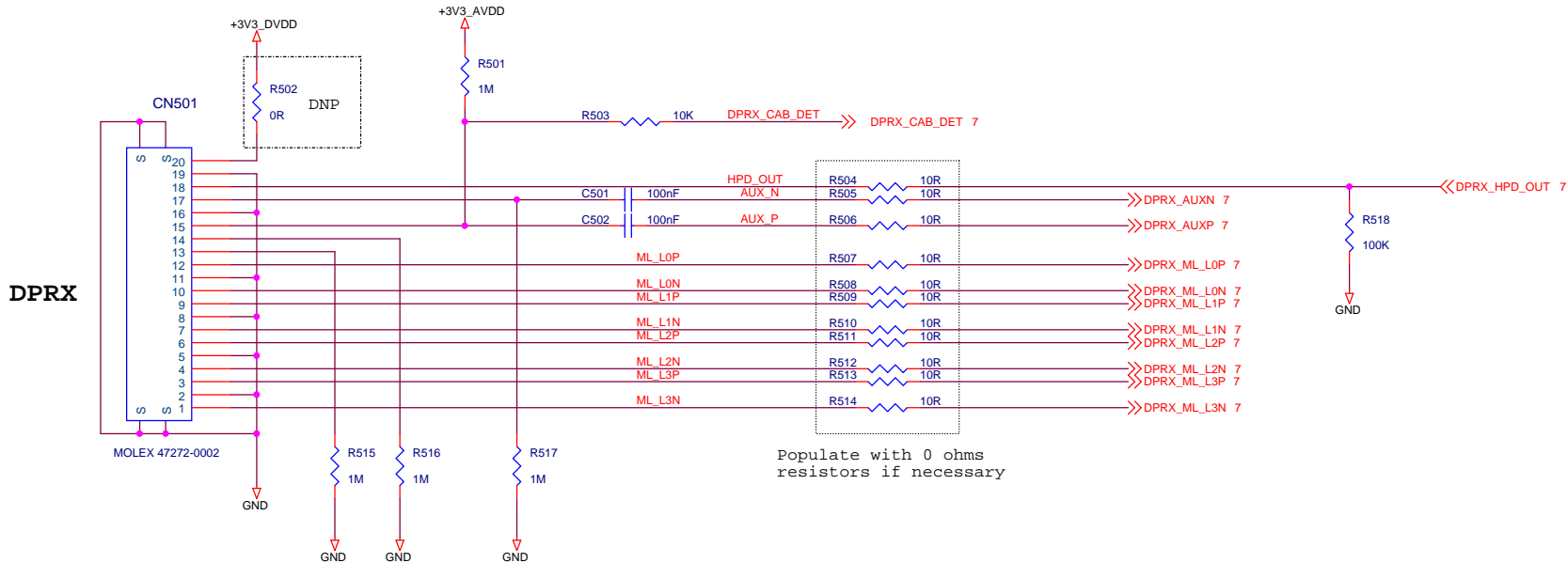


**Host Control Interface**



**Audio Output Section (8-CH I2S and S/PDIF)**

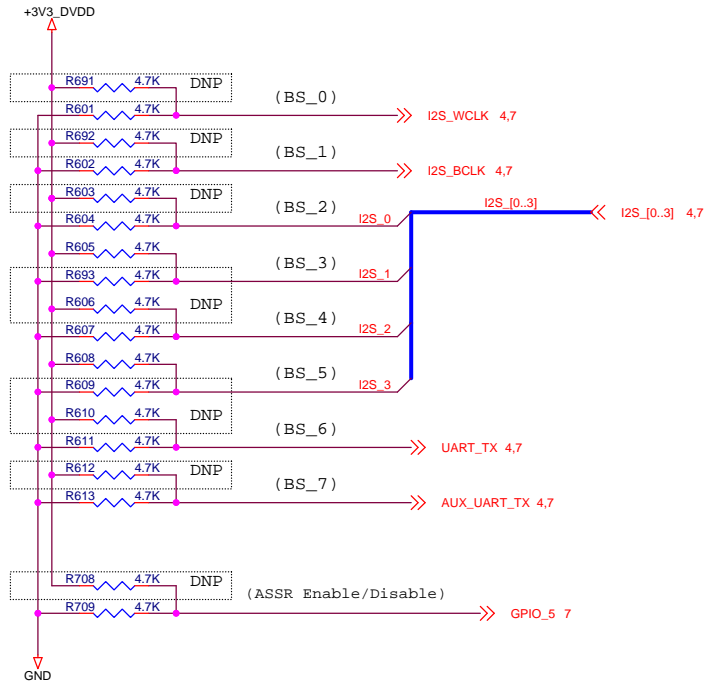
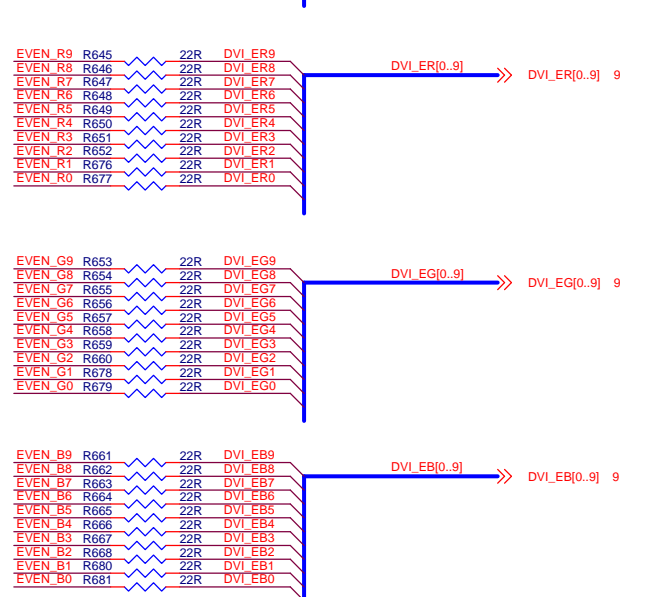
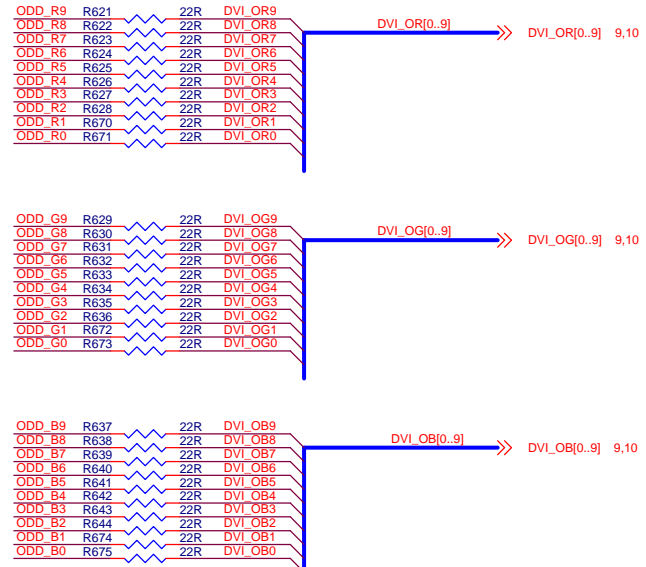
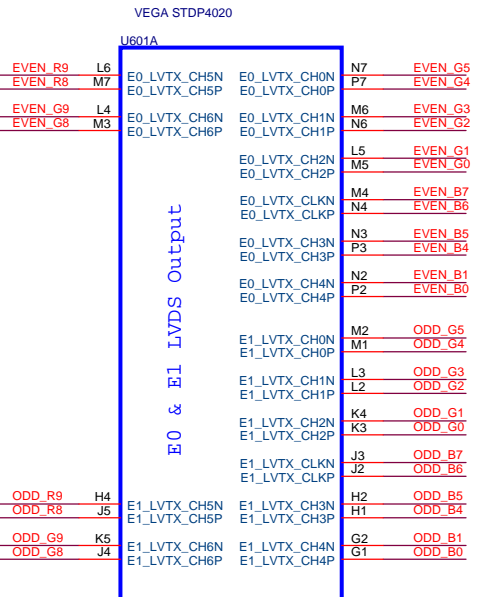
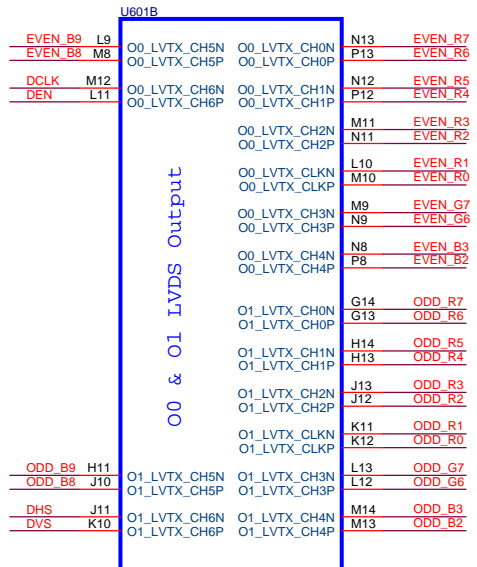
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ESD Protection Diodes



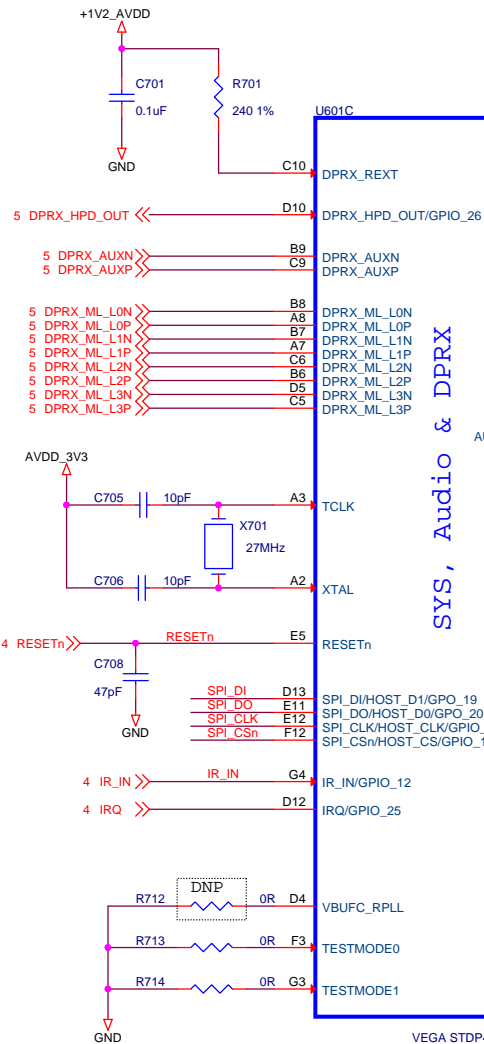
Title		
05. DPRx Interface		
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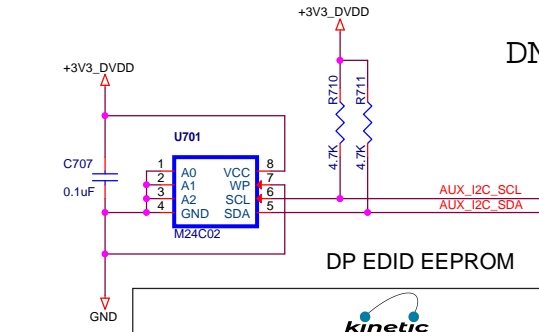
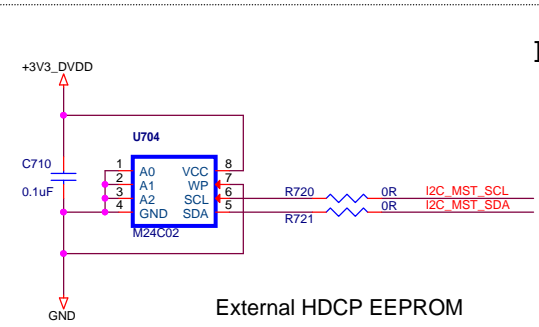
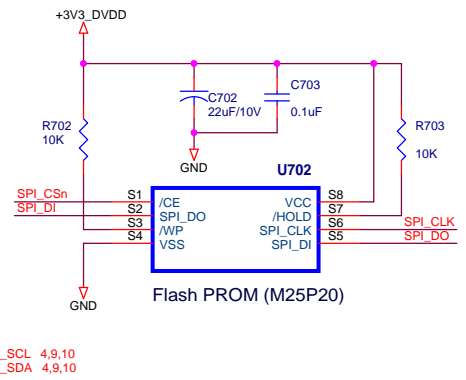
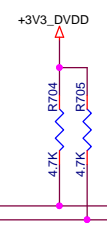
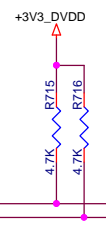
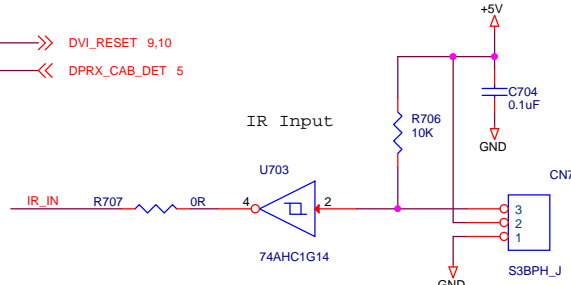
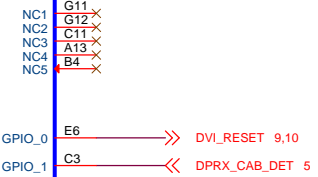
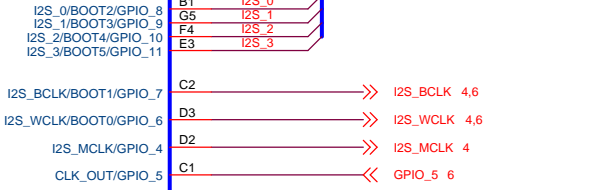
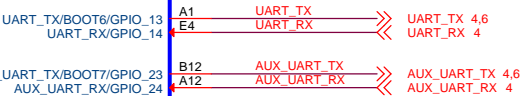
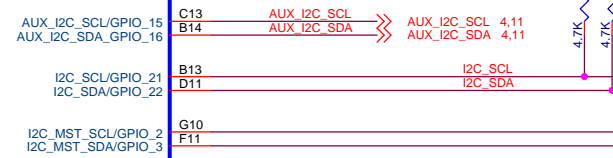
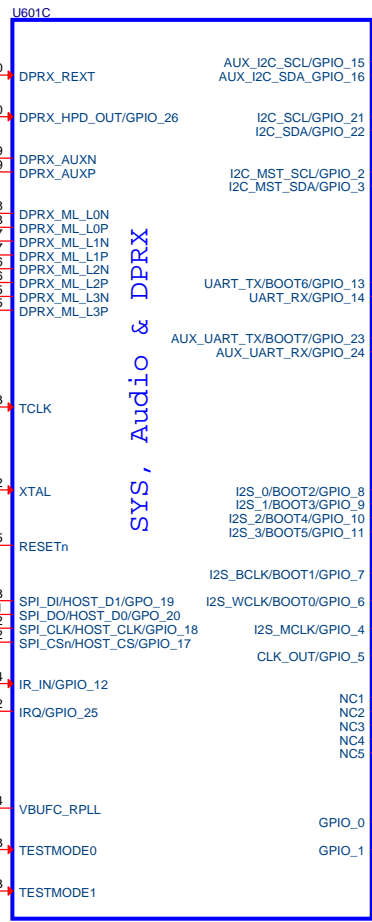
**kinetic technologies**

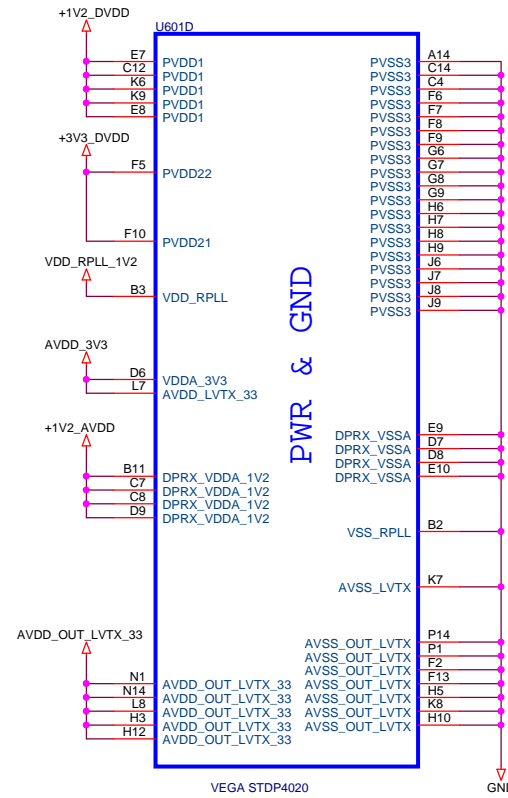
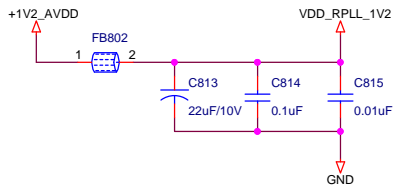
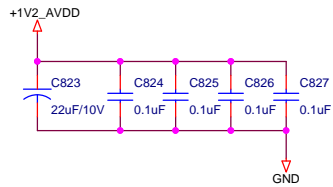
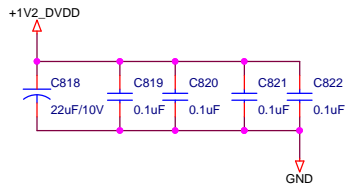
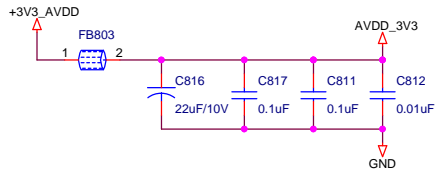
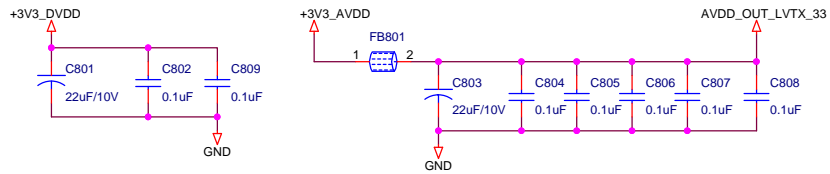
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SYS, Audio & DPRX

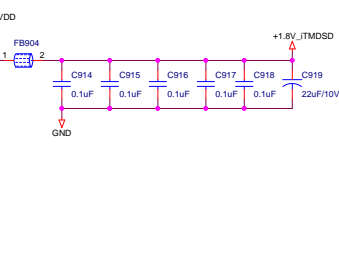
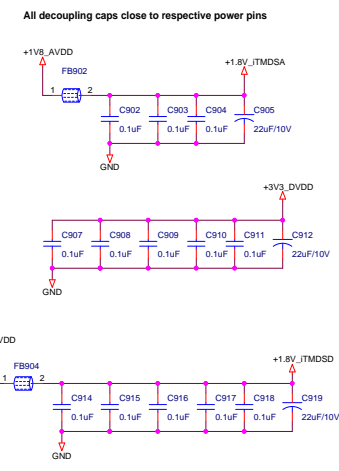
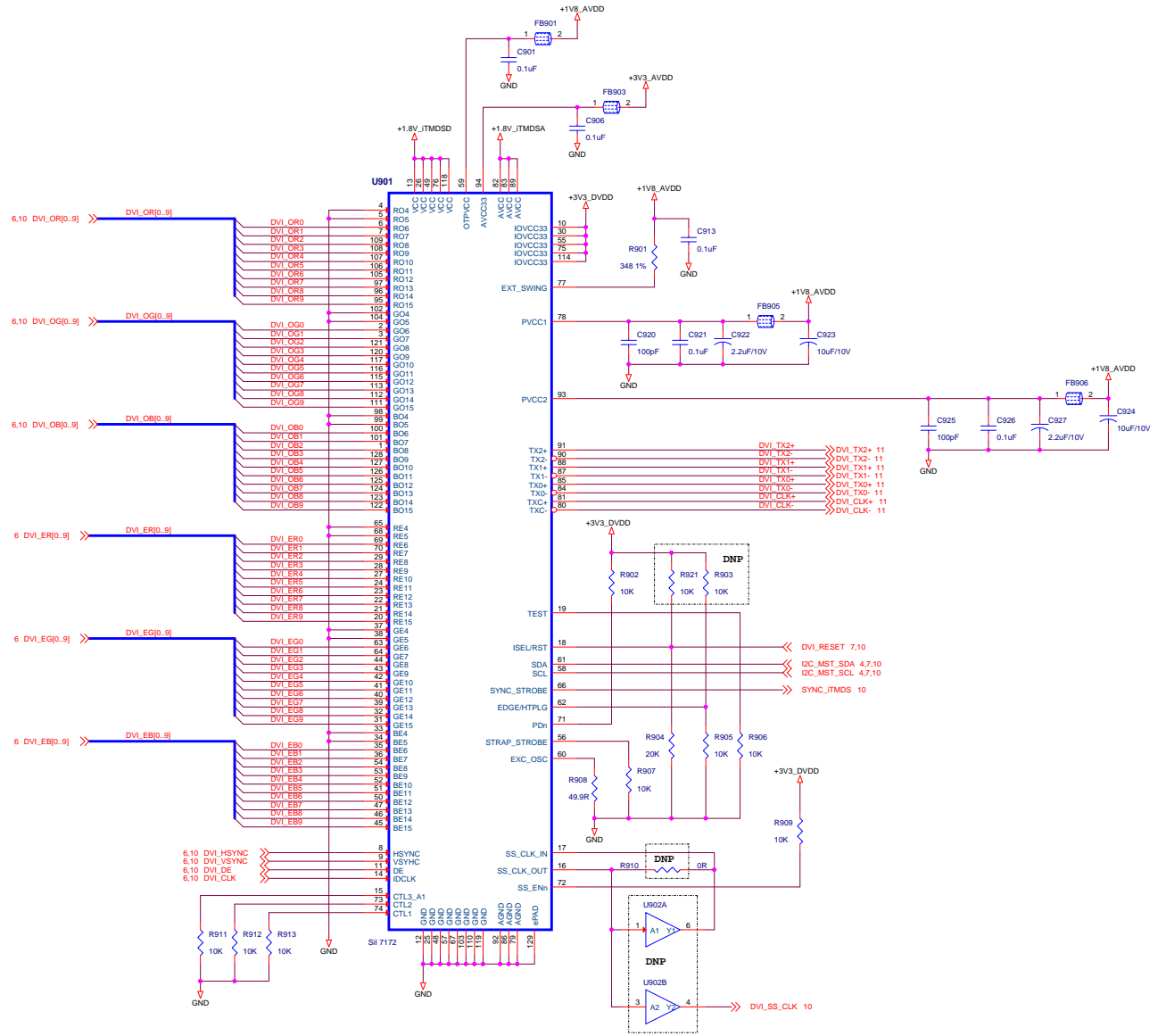




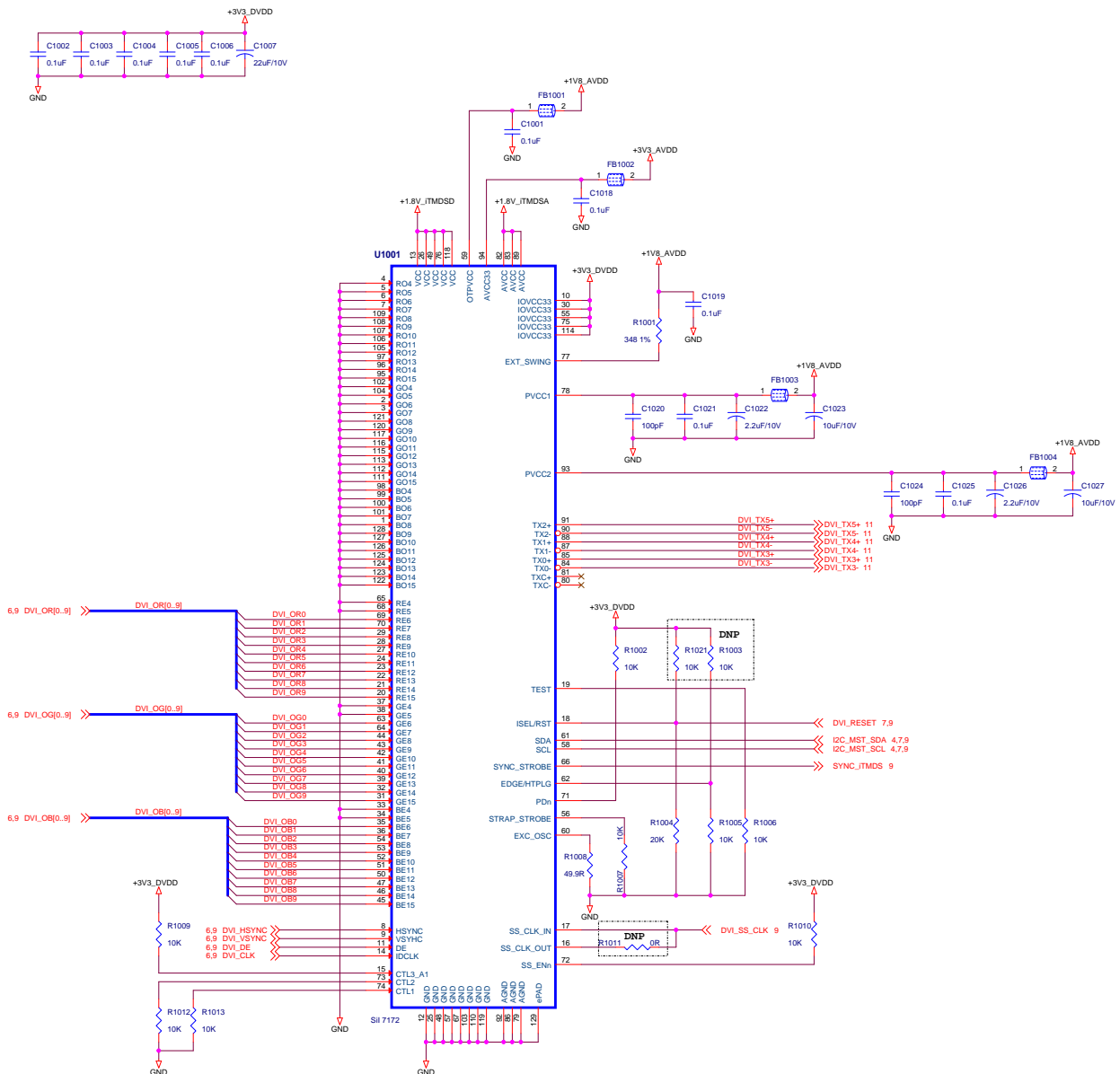
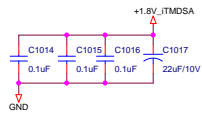
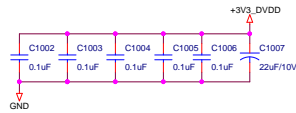
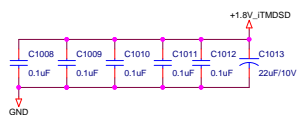
PWR & GND

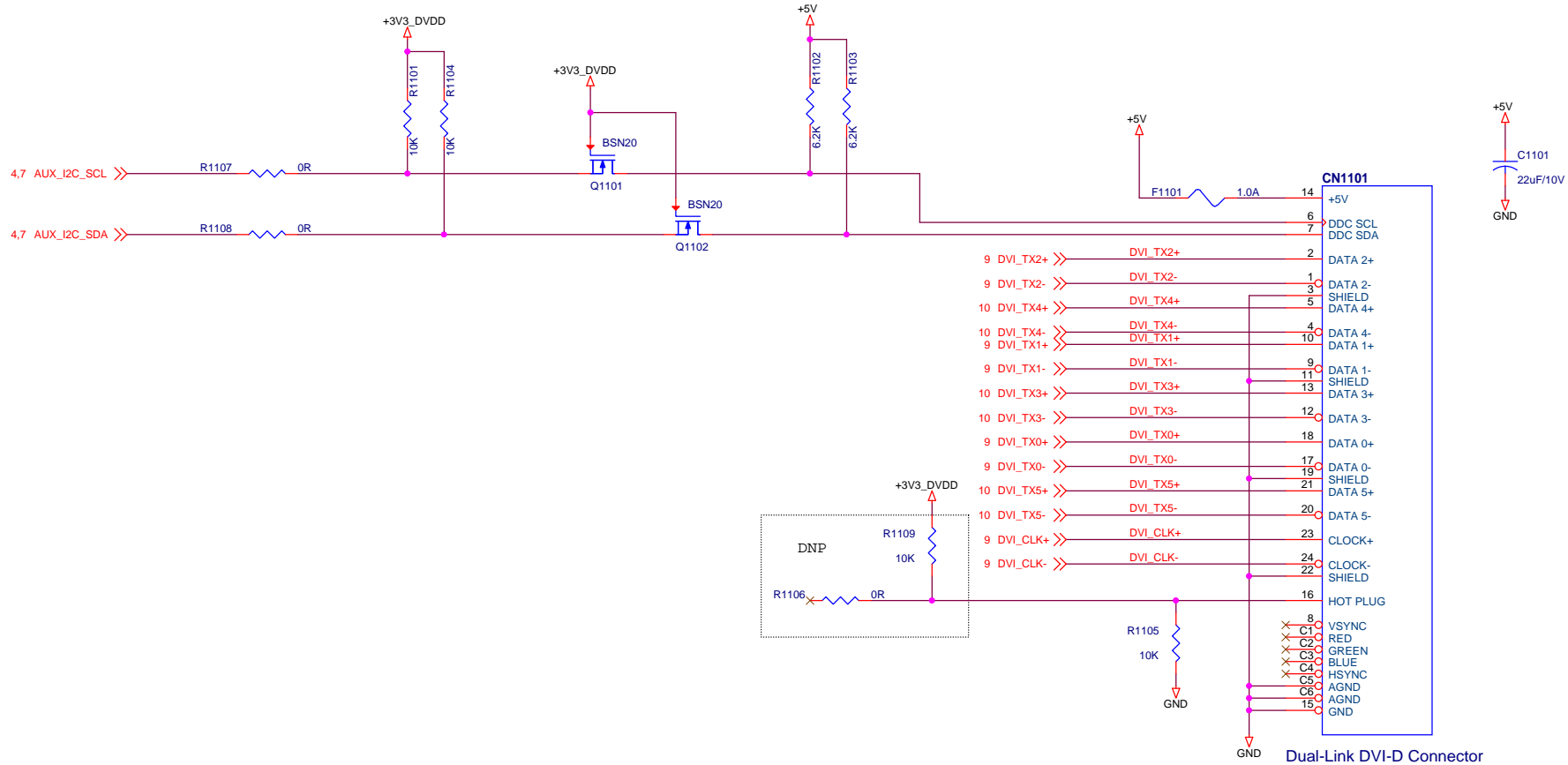
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All decoupling caps close to respective power pins





**Title**  
**11. Dual Link DVI Connector & I2C level Shifter**

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