Evaluating the ADMV8526 1.25 GHz to 2.60 GHz Digitally Tunable Band-Pass Filter

FEATURES

- Fully featured evaluation board for the ADMV8526
- On-board system demonstration platform (SDP-S) connector for the SPI
- Evaluation using on-board LDO regulators powered by the USB
- ACE software interface for SPI control

EQUIPMENT NEEDED

- Network analyzer
- Windows® PC
- USB cable
- EVAL-SDP-CS1Z (SDP-S) controller board

DOCUMENTS NEEDED

- ADMV8526 data sheet

SOFTWARE NEEDED

- ACE software

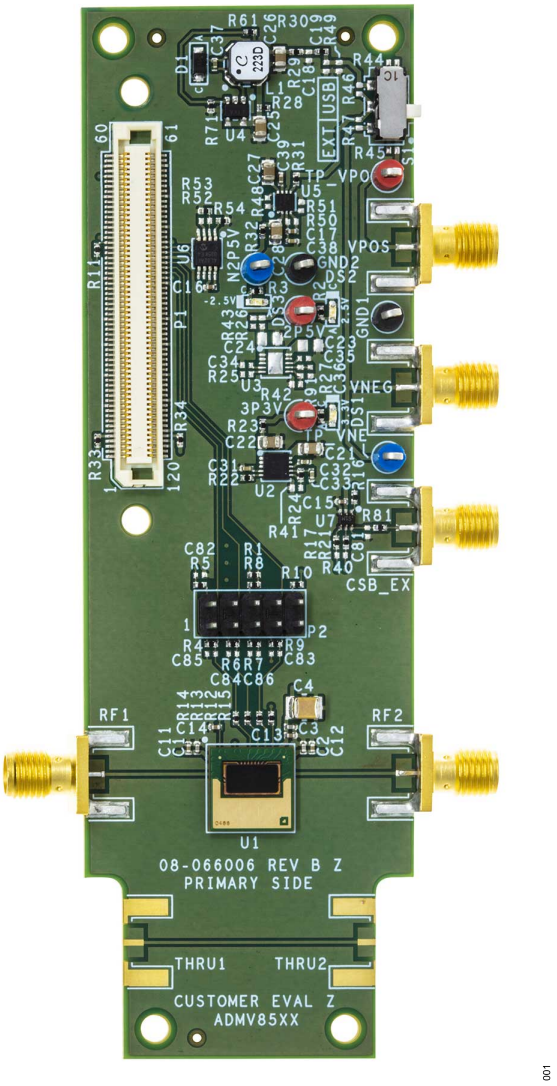
GENERAL DESCRIPTION

The ADMV8526-EVALZ is available for evaluating the ADMV8526 digitally tunable, band-pass filter (BPF). The ADMV8526-EVALZ incorporates the ADMV8526 chip, as well as a negative voltage generator, low dropout (LDO) regulators, and an interface to the EVAL-SDP-CS1Z (SDP-S) system demonstration platform (SDP) to allow simple and efficient evaluation. The negative voltage generator and LDO regulators allow the ADMV8526 to be powered by either the 5 V USB supply voltage from the PC via the SDP-S or by using two external power supplies.

The ADMV8526 is an IC that features a digitally selectable frequency of operation. The chip can be programmed using a 4-wire serial peripheral interface (SPI), and the SDP-S controller allows the user to interface with the SPI of the ADMV8526 through the Analog Devices, Inc., Analysis, Control Evaluation (ACE) software.

For full details on the ADMV8526, see the ADMV8526 data sheet, which must be consulted in conjunction with this user guide when using the ADMV8526-EVALZ.

EVALUATION BOARD PHOTOGRAPH



001

Figure 1. ADMV8526-EVALZ

TABLE OF CONTENTS

REVISION HISTORY

11/2021—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADMV8526-EVALZ has the ADMV8526 chip on board. The ADMV8526-EVALZ also includes a negative voltage generator and three LDO regulators to provide the necessary supply voltages for the chip. The regulators can be entirely powered by the 5 V USB supply voltage from the PC via the SDP-S.

To power the ADMV8526-EVALZ using the 5 V USB supply, slide the S1 switch to select USB (as shown in Figure 2) to power the on-board negative voltage generator and LDO regulators. Alternatively, the ADMV8526-EVALZ can be powered externally by sliding the S1 switch to select EXT and then connecting the power supplies to the VPOS and VNEG Subminiature Version A (SMA) ports or test points. The applicable voltage range for the positive input VPOS is between 3.5 V and 5.5 V, and the applicable voltage range for the negative input VNEG is between −5.5 V and −2.7 V.

Figure 2 shows an example lab bench setup for the ADMV8526-EVALZ. To observe the filter response from the ADMV8526-EVALZ, connect the RF1 and RF2 ports to a network analyzer (or similar instrument). Typically, RF1 and RF2 are connected to Port 1 and Port 2 on the network analyzer, as shown in Figure 2.

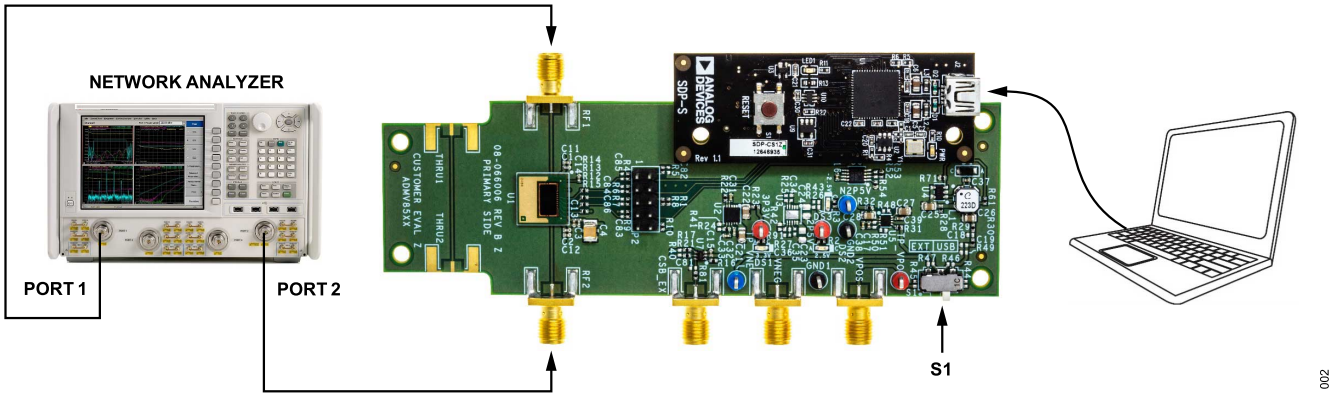


Figure 2. ADMV8526-EVALZ Lab Bench Setup

EVALUATION BOARD SOFTWARE

INSTALLING THE ACE SOFTWARE, ADMV8526 PLUG-INS, AND DRIVERS

The ADMV8526-EVALZ uses the Analog Devices Analysis|Control|Evaluation (ACE) software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

If the ACE software is already installed on the PC, ensure that the installed ACE software is the latest version, as listed on the ACE software page. If the installed software is not the latest version, take the following steps to install the updated ACE software:

1. Uninstall the current version of the ACE software on the PC.
2. Delete the ACE folders found in **C:\ProgramData\Analog Devices** and **C:\ProgramData (x86)\Analog Devices**.
3. Install the latest version of the ACE software. During installation, ensure that the **.Net 40 Client**, **SDP Drivers**, the **LRF Drivers** installations are checked off as well (see Figure 3).

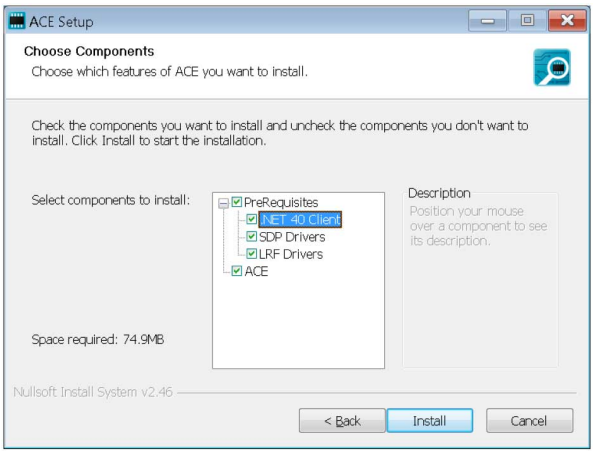


Figure 3. Required Driver Installations with the ACE Software

Once installation completes, the **ADMV8526 Board** plug-in appears in the **Attached Hardware** section of the **Start** tab when the ACE software is running (see Figure 4).

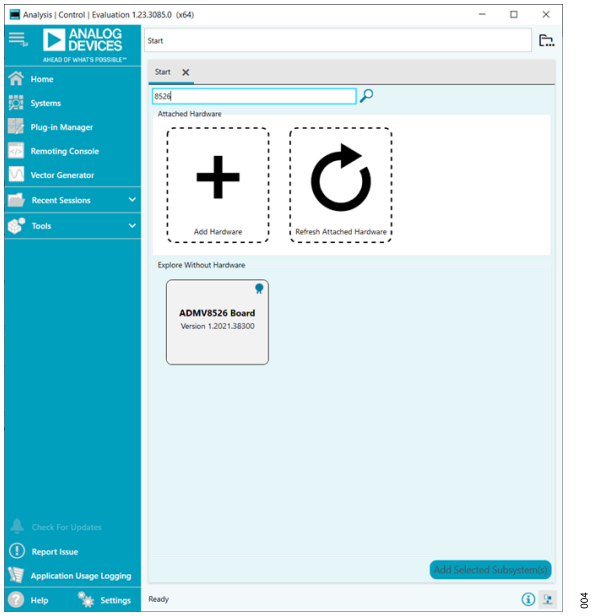


Figure 4. ADMV8526 Board Plug-In Window After Opening the ACE Software

EVALUATION BOARD SOFTWARE

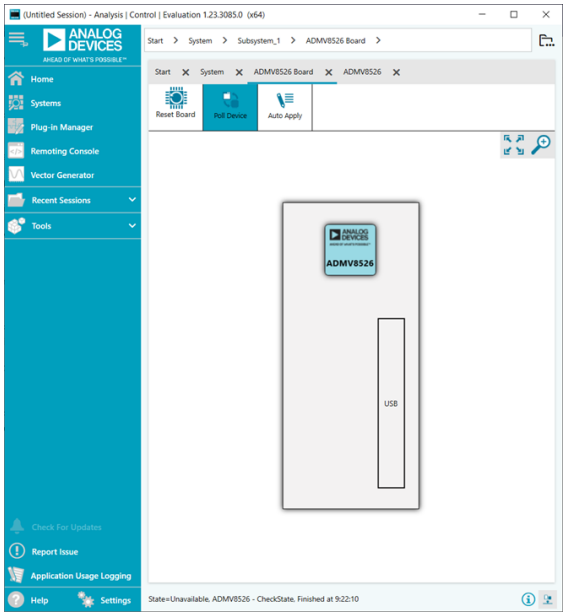
PLUG-IN OVERVIEW

When the ADMV8526-EVALZ is connected to the PC, the **ADMV8526 Board** appears in the **Attached Hardware** section of the **Start** tab. Double-click the **ADMV8526 Board** plug-in to open two tabs, which are the **ADMV8526 Board** plug-in view (see Figure 5) and the **ADMV8526** chip plug-in view (see Figure 6), respectively.

The **ADMV8526** chip plug-in view includes the following feature sections (see Table 1 for additional information on these sections):

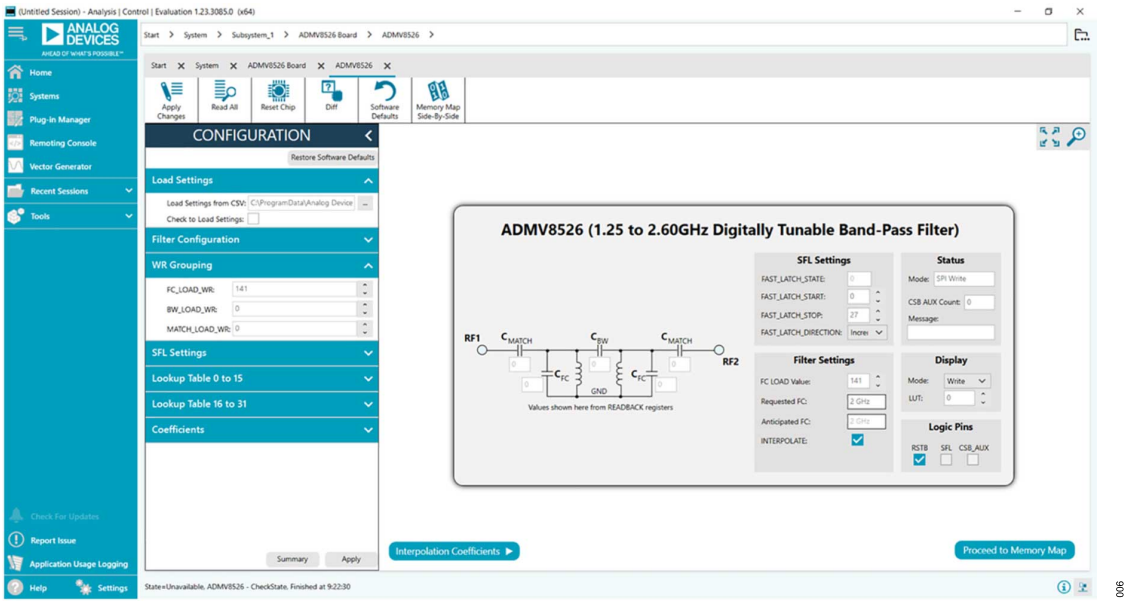
- The **CONFIGURATION** section (load from .csv)
- The **Logic Pins** section
- The **SFL Settings** section
- The chip **Status** section
- The **Display** controls section
- The **Filter Settings** section

The ACE software provides a simple tutorial for testing the ADMV8526. For a more customized and detailed implementation, refer to ADMV8526 data sheet for a full description of the functionality, registers, and corresponding settings.



005

Figure 5. ADMV8526 Board Plug-In View



006

Figure 6. ADMV8526 Chip Plug-In View

EVALUATION BOARD SOFTWARE

PLUG-IN DETAILS

The full screen ADMV8526 chip plug-in with labels is shown in Figure 7. The labels correspond to items listed in Table 1, which describes the functionality of each section. For additional detailed programming, refer to the ADMV8526 data sheet.

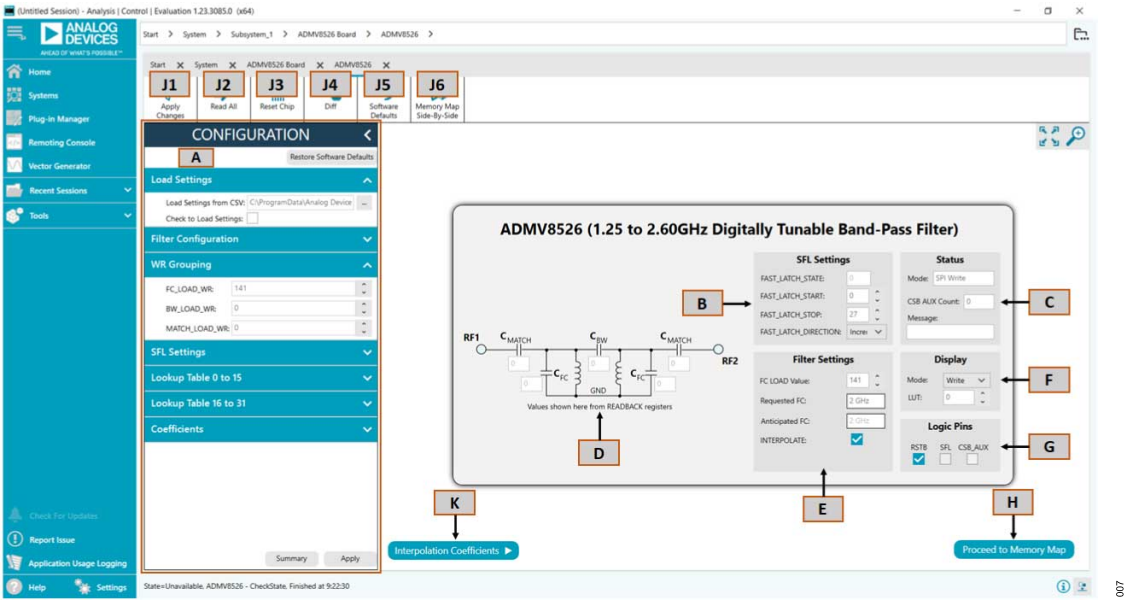


Figure 7. ADMV8526 Chip Plug-In with Labels

Table 1. ADMV8526 Chip Plug-In Label Functions (See Figure 7)

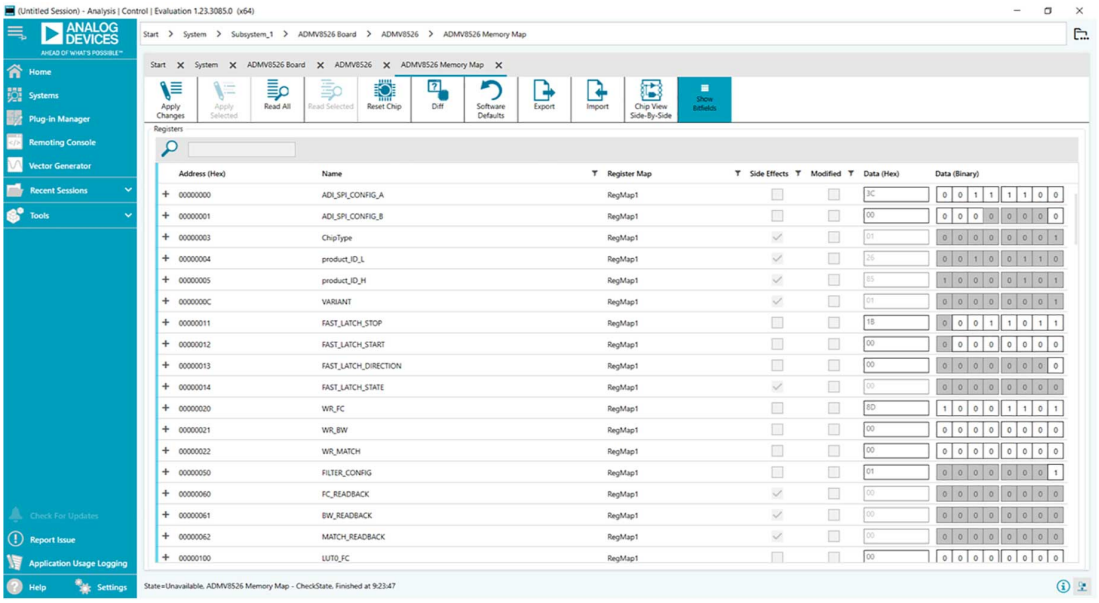
Label	Function
A	Use the **CONFIGURATION** section to initialize the ADMV8526-EVALZ. **Load Settings from CSV:** click the **...** button to select which .csv file to load into the **CONFIGURATION** section. **Check to Load Settings:** once a file is selected, select this check box to load the .csv file contents into the **CONFIGURATION** section. Note that a check mark does not appear when the check box is selected. **Filter Configuration:** select the configuration settings for enabling or disabling the interpolation function. **WR Grouping:** select the write (WR) grouping settings for SPI write mode. **SFL Settings:** select the SPI fast latch (SFL) settings that are used when the chip is placed into the SPI fast latch mode. **Lookup Table 0 to 15:** define the configuration for lookup table (LUT)0 to LUT15. **Lookup Table 16 to 31:** define the configuration for LUT16 to LUT31. **Coefficients:** define the interpolation coefficients. **Summary:** click this button to review the settings for the initial setup. **Apply**: click this button to apply the settings to the chip. Note that clicking **Apply Changes** (J1) does not update the changes in this section. In addition, at startup, the main diagram user controls cannot be updated until the **Apply** button is clicked at least once. **Restore Software Defaults:** click this button to zero out the **CONFIGURATION** section before loading a different .csv file.
B	Use the **SFL Settings** section to configure the SPI fast latch settings on the chip when in the SFL mode. Refer to the ADMV8526 data sheet for more information regarding the internal state machine and SFL mode functionality. This section includes the following: **FAST_LATCH_STATE:** this value is the next state of the internal state machine pointer (read only). **FAST_LATCH_START:** this value determines the start location within the internal state machine. **FAST_LATCH_STOP:** this value determines the stop location within the internal state machine. **FAST_LATCH_DIRECTION:** this bit determines the direction that the internal state machine advances for each rising edge of the $\overline{CS}$ pin when in SFL mode.
C	The **Status** section includes the following: **Mode:** when the SFL pin is low, the mode is **SPI Write**. When the SFL pin is high, the mode is **SPI Fast Latch**, and the chip uses the LUT. **CSB_AUX Count:** when in SFL mode, this field displays the number of times the SDP-S logic pin, CSB_AUX, was toggled. **Message:** upon entering SFL mode, the **Message** field displays **Waiting for CSB**. Once the CSB_AUX pin is toggled, the **Message** field displays the current LUT number followed by the next LUT number.

EVALUATION BOARD SOFTWARE

Table 1. ADMV8526 Chip Plug-In Label Functions (See Figure 7)

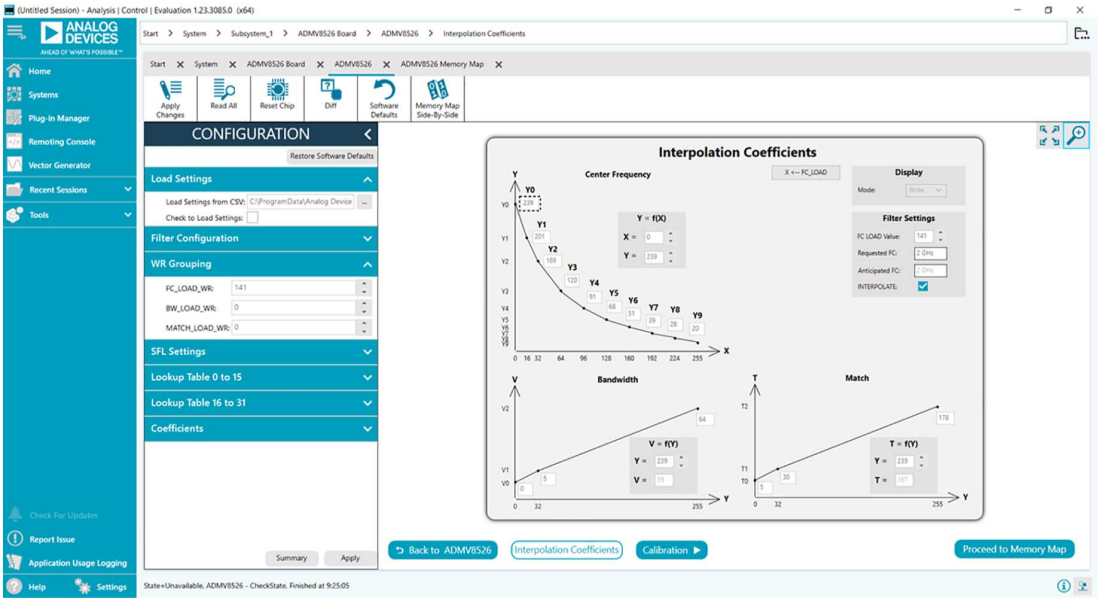
Label	Function
D	The displayed block diagram section shows the capacitor codes for the filter. While in **SPI Write** mode, any changes to the WR registers automatically triggers a read operation of the **READBACK** registers, so that this section always reflects the actual hardware.
E	The **Filter Settings** section shows several controls for configuring the filter. Depending upon if **INTERPOLATE** is enabled, various controls can be visible. When **INTERPOLATE** is enabled (as shown Figure 7), the following controls are visible: **FC_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired center frequency value. Note that this is a unitless quantity, where a 0 corresponds to the lowest center frequency, and 255 corresponds to the highest center frequency. **Requested FC:** enter in a requested center frequency in this text box. The value entered is used to compute the closest **FC_LOAD Value** for that frequency of operation. **Anticipated FC:** this text box is an estimation of the operating center frequency based upon the **FC_LOAD Value**. **INTERPOLATE:** this check box enables the interpolation functionality on the chip. When **INTERPOLATE** is disabled (not shown in Figure 7), the following controls are visible: **FC_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired center frequency capacitor code. **BW_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired bandwidth capacitor code. **MATCH_LOAD Value:** this numeric up and down box (0 to 255) is used to set the desired input and output match capacitor code. **INTERPOLATE:** this check box enables the interpolation functionality on the chip. **READBACK Values to Filter Settings:** this button is available when interpolation is disabled. Click this button to populate the read back values from the hardware into the FC_LOAD, BW_LOAD, and MATCH_LOAD values.
F	The **Display** section determines the actively selected SPI write or LUT number. This section includes the following: **Mode:** use the drop-down menu to select either write or LUT display mode. When the display mode is set to write, then the **Filter Settings** section updates the WR registers. **LUT:** when the **Mode** is set to **LUT**, scroll up and down to set the LUT number (0 to 31) that is currently being configured and displayed in the **Filter Settings** section. Changing to the LUT number automatically changes the **Mode** to **LUT**.
G	Use the **Logic Pins** section to toggle the SDP-S logic pins, which are connected to the logic pins on the ADMV8526 chip. This section includes the following: **RSTB:** clear the check box to bring the ADMV8526 $\overline{\text{RST}}$ pin low, which holds the chip in reset. Select the check box again to bring the chip out of reset. **SFL:** select the check box to bring the ADMV8526 SFL pin high, which places the chip in SFL mode. This action also toggles the on-board ADG749BKSZ switch connected to the ADMV8526 $\overline{\text{CS}}$ pin (see Figure 12). While in SFL mode, the ADMV8526 $\overline{\text{CS}}$ pin is connected to the SDP-S logic pin, CSB_AUX, and normal SPI transactions are disallowed. **CSB_AUX:** this pin is only available in SFL mode. Selecting the check box brings the CSB_AUX pin high, which advances the internal state machine pointer to the next LUT. If an external waveform generator is connected to the CSB_EXT port on the ADMV8526-EVALZ, the CSB_AUX pin has no effect, and the CSB_EXT port takes precedence.
H	Click **Proceed to Memory Map** to open the **ADMV8526 Memory Map** (see Figure 8)
J1	All changes, except those made within the **CONFIGURATION** section, do not take effect until clicking **Apply Changes.** If **Auto Apply** is highlighted in the **ADMV8526 Board** tab (see Figure 5), the **Apply Changes** feature continuously runs every few seconds, and users do not have to click the **Apply Changes** to apply or read back the block diagram settings.
J2	To read back all of the SPI registers of the chip, click **Read All**.
J3	Click **Reset Chip** to reset the chip.
J4	Click **Diff** to show registers that are different on the chip.
J5	Click **Software Defaults** to restore the software defaults to the chip, and then click **Apply Changes**. The software defaults for the ADMV8526 registers are zero, except for Register 0x011, which is set to 0x7F, and the interpolation coefficients in Register 0x300 to Register 0x30F.
J6	Click **Memory Map Side-By-Side** to enable the side by side memory map view.
K	Click **Interpolation Coefficients** to open the subdiagram for displaying and editing the interpolation coefficients (see Figure 9). The interpolation coefficients can be changed to calibrate the center frequency and/or change the desired operating bandwidth of the filter. Once the **Interpolation Coefficients** subdiagram is visible, an additional button, **Calibration**, is available. Click **Calibration** to open the additional subdiagram (see Figure 10) for performing the recommended calibration sequence. Refer to the ADMV8526 data sheet theory of operations section for guidance on editing the interpolation coefficients.

EVALUATION BOARD SOFTWARE



008

Figure 8. ADMV8526 Memory Map in the ACE Software



009

Figure 9. Interpolation Coefficients Subdiagram in the ACE Software

EVALUATION BOARD SOFTWARE

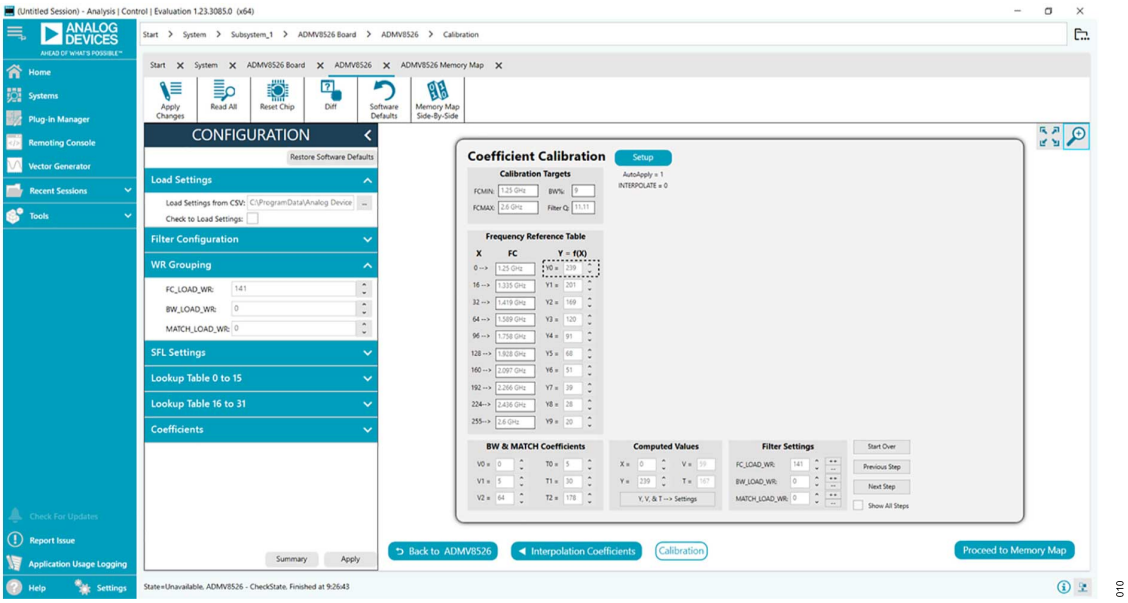


Figure 10. Coefficient Calibration Subdiagram in the ACE Software

PERFORMING EVALUATION

ADMV8526-EVALZ QUICK START

To set up the ADMV8526-EVALZ, take the following steps:

1. Connect the RF1 and RF2 ports to a network analyzer (or a similar instrument). Typically, RF1 and RF2 are connected to Port 1 and Port 2 on the network analyzer, as shown in Figure 2.
2. Connect the SDP-S to the 120-pin connector on the ADMV8526-EVALZ. Do not connect the SDP-S to the PC until after completing Step 3 or Step 4.
3. On the ADMV8526-EVALZ, slide the S1 switch to select USB (as shown in Figure 2) to power the ADMV8526-EVALZ from the 5 V USB supply voltage from the PC via the SDP-S.
4. Alternatively to Step 3, slide the S1 switch to select EXT and connect the power supplies to the VPOS and VNEG ports. The applicable voltage range for VPOS is between +3.5 V and +5.5 V and for VNEG is between −5.5 V and −2.7 V. The external supply current limits must be set to 20 mA. Expected supply current drawn for VPOS is 12 mA to 14 mA and for VNEG is 2 mA to 3 mA. The ADMV8526 chip current drawn per supply pin is typically 10s of microamps or less. Most of the current drawn from the ADMV8526-EVALZ comes from the LDO regulators and the status indicator light emitting diodes (LEDs), DS1 to DS3.
5. Connect a USB cable between the PC and the SDP-S.
6. Open the ACE software. The **ADMV8526 Board** appears in the **Attached Hardware** section of the **Start** tab. Double-click on the **ADMV8526 Board** plug-in to open two tabs, one is the **ADMV8526 Board** plug-in view, and one is the ADMV8526 chip plug-in view.
7. Use the **CONFIGURATION** section (see Figure 11) in the ACE software to initialize the chip. By default, the **ADMV8526_Coefficients_Bandwidth_Nominal.csv** file is loaded into this section. Click **Apply** to send the default settings to the chip and to allow the main diagram user controls to become editable.

NETWORK ANALYZER SETTINGS

When evaluating the ADMV8526-EVALZ, a good starting point for configuring the network analyzer is as follows:

- Start frequency = 0.01 GHz
- Start frequency = 4.01 GHz
- Number of points = 4001
- Step size = 1 MHz
- Power level = –10 dBm
- Measure types = S-parameters (S21, S11, and S22)
- Format = log magnitude (S21), smith charts (S11 and S22)
- Calibration = full 2-port

CSV FILES

By default, the **ADMV8526_Coefficients_Bandwidth_Nominal.csv** file is loaded into the **CONFIGURATION** section. This file contains interpolation coefficients that correspond to approximately 9% bandwidth. There are two additional .csv files provided that contain interpolation coefficients for approximately 7% and 11% bandwidth, respectively. To load a different .csv file in the **CONFIGURATION** section, take the following steps:

1. If the **Modify** button is visible, click to allow changes.
2. Click **Restore Software Defaults** to zero out the **CONFIGURATION** section.
3. Click the **…** button next to **Load Settings from CSV** to select which .csv file to load (see Figure 11).
4. Select the **Check to Load Settings** check box to load the .csv file contents into the **CONFIGURATION** section. Note that a check mark does not appear when the check box is selected.
5. Click **Apply** to send out the settings to the hardware.

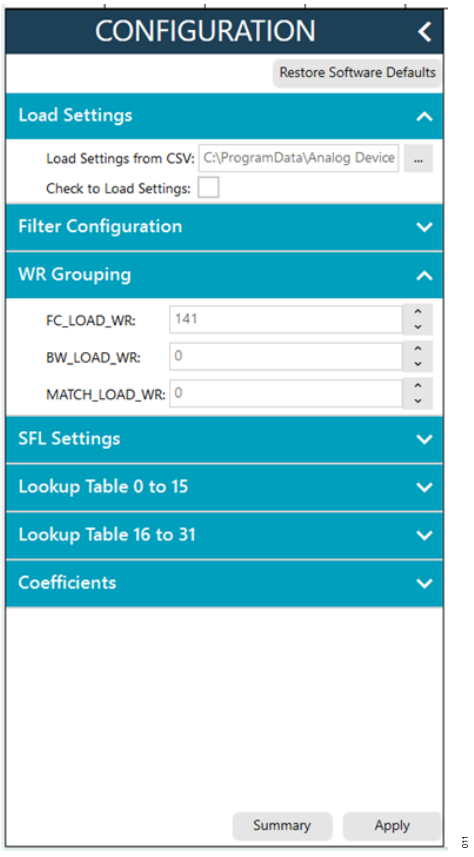


Figure 11. ADMV8526 CONFIGURATION Section

PERFORMING EVALUATION

AUTOMATIC CHIP RESET

If a reset of the ADMV8526 chip is required on the ADMV8526-EVALZ, click **Reset Chip** (see Figure 7, Label J3, and Table 1 for additional information). This automated sequence performs the following actions:

- Toggles all SDP-S general-purpose input and output (GPIO) logic pins to a low state, which brings the $\overline{\text{RST}}$ pin of the ADMV8526 low to initiate a hard reset of the ADMV8526.
- Toggles the $\overline{\text{RST}}$ pin high to bring the ADMV8526 chip back to the normal operating state.
- Programs Register 0x000 to 0x81, which also resets the ADMV8526. This step covers legacy boards that did not have the $\overline{\text{RST}}$ pin connected.
- Programs Register 0x000 to 0x3C to enable the SDO pin on the ADMV8526 and to allow SPI streaming with Endian register ascending order.
- Reads back the register settings of the ADMV8526.

MANUAL CHIP RESET

For manual reset operations, the following outlines two ways to perform a reset:

- The $\overline{\text{RST}}$ pin can also be pulled low from within the ACE software by unchecking the **RSTB** check box in the lower right corner of Figure 7 (see Label G). When using this option, be sure to click the check box again to return the $\overline{\text{RST}}$ pin high.
- Register 0x000 can be programmed to 0x81 to initiate a reset of the ADMV8526.

Regardless of the manual reset option used, it is recommended to perform the following after the device resets:

- Programs Register 0x000 to 0x3C to enable the SDO pin on the ADMV8526 and to allow SPI streaming with Endian register ascending order.
- Read back all registers on the ADMV8526.

LOSS OF BOARD COMMUNICATION

When the ADMV8526 is turned off and then on, or if the USB cable is disconnected and connected while the ACE software is running, communication with the ADMV8526 may be lost. To regain communication, take the following steps:

1. Click the **System** tab.
2. Click the USB symbol in the **SDP-S Controller** subsystem.
3. Click **Acquire**.

If this action does not work, restart the ACE software to reinitiate communication with the ADMV8526-EVALZ.

REGULATOR BYPASS

The ADMV8526-EVALZ has a negative voltage generator and three LDO regulators on board that allow the user to operate the device using the 5 V USB supply voltage from the PC via the SDP-S. By default, the provisional 2.5 V LDO regulator, U3, is not installed because the ADMV8526 has a built-in LDO regulator for that supply voltage. The other two on-board LDO regulators, U2 and U5, provide the necessary supply voltages of +3.3 V and −2.5 V, respectively. If desired, these two LDO regulators can be bypassed by removing the 0 Ω resistors (R23 and R32) from the ADMV8526-EVALZ and then by applying each voltage independently by using the corresponding test points. Bypassing the on-board regulators is useful for measuring the ADMV8526 supply current, but it must be noted that each supply pin is also connected to status indicator LEDs, DS1 to DS3, and each LED draws approximately 2 mA of current. Remove the R2, R3, and R91 resistors to disable these status indicators. See Figure 12 and Figure 13 for more details.

PLUG-IN SPI REGISTER CONTROLLER

The ADMV8526 plug-in utilizes an SPI register controller to communicate with the ADMV8526. When using the ADMV8526 in a system, it is recommended to follow a similar methodology for implementing SPI communication. The following is a summary of the SPI register controller:

1. Determine if Register 0x000 is not set to 0x3C.
2. If Step 1 is true, set Register 0x000 to 0x3C to enable the SDO pin on the ADMV8526 and to allow SPI streaming with Endian register ascending order.
3. Determine if the values have changed for any of the WR registers (Register 0x020 to Register 0x022).
4. If Step 3 is true, write to Register 0x020 through Register 0x022 by pointing to Register 0x020 and streaming out 3 bytes of data. The transaction is 40 bits in total (R/W bit + 15 address bits + 24 data bits).
5. If Step 4 has occurred, write dummy data to Address 0x0A. Note that Address 0x0A does not exist in the ADMV8526, and the written dummy data is ignored. This step is microcontroller architecture dependent and can be ignored in most cases. It is necessary for the SDP-S to clear the SPI bus and reconfigure for a standard 24-bit SPI transaction.
6. Determine if the values have changed for any of the LUT registers (Register 0x100 to Register 0x15F).
7. If Step 6 is true, write to Register 0x100 to Register 0x15F by performing the following:
    a. Pointing to Register 0x100 and streaming out 48 bytes of data.
    b. Pointing to Register 0x130 and streaming out 48 bytes of data.
8. If Step 7 has occurred, repeat Step 5.
9. Write out any remaining registers that may have changed.

EVALUATION BOARD SCHEMATICS AND ARTWORK

ADMV8526-EVALZ

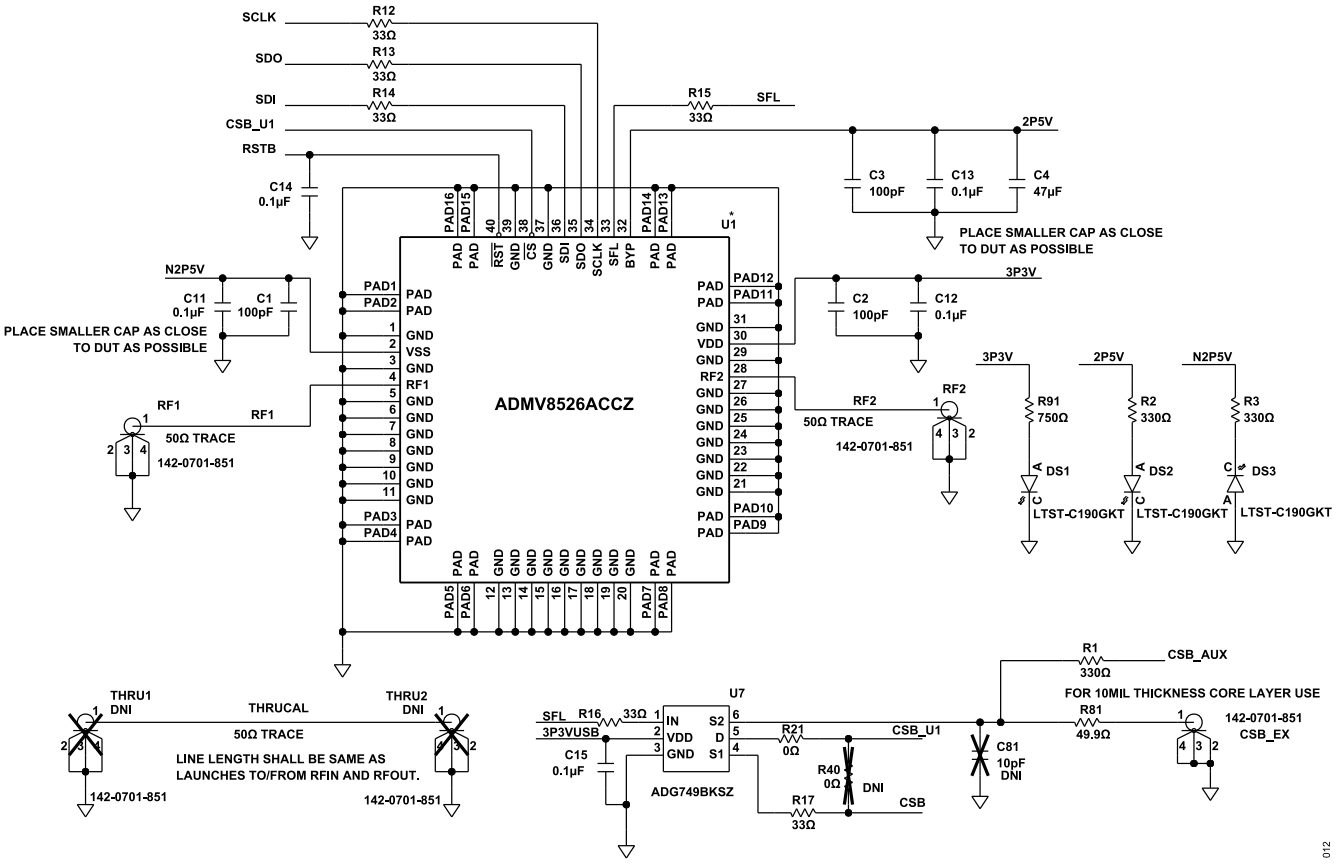


Figure 12. ADMV8526-EVALZ Schematic, Page 1

EVALUATION BOARD SCHEMATICS AND ARTWORK

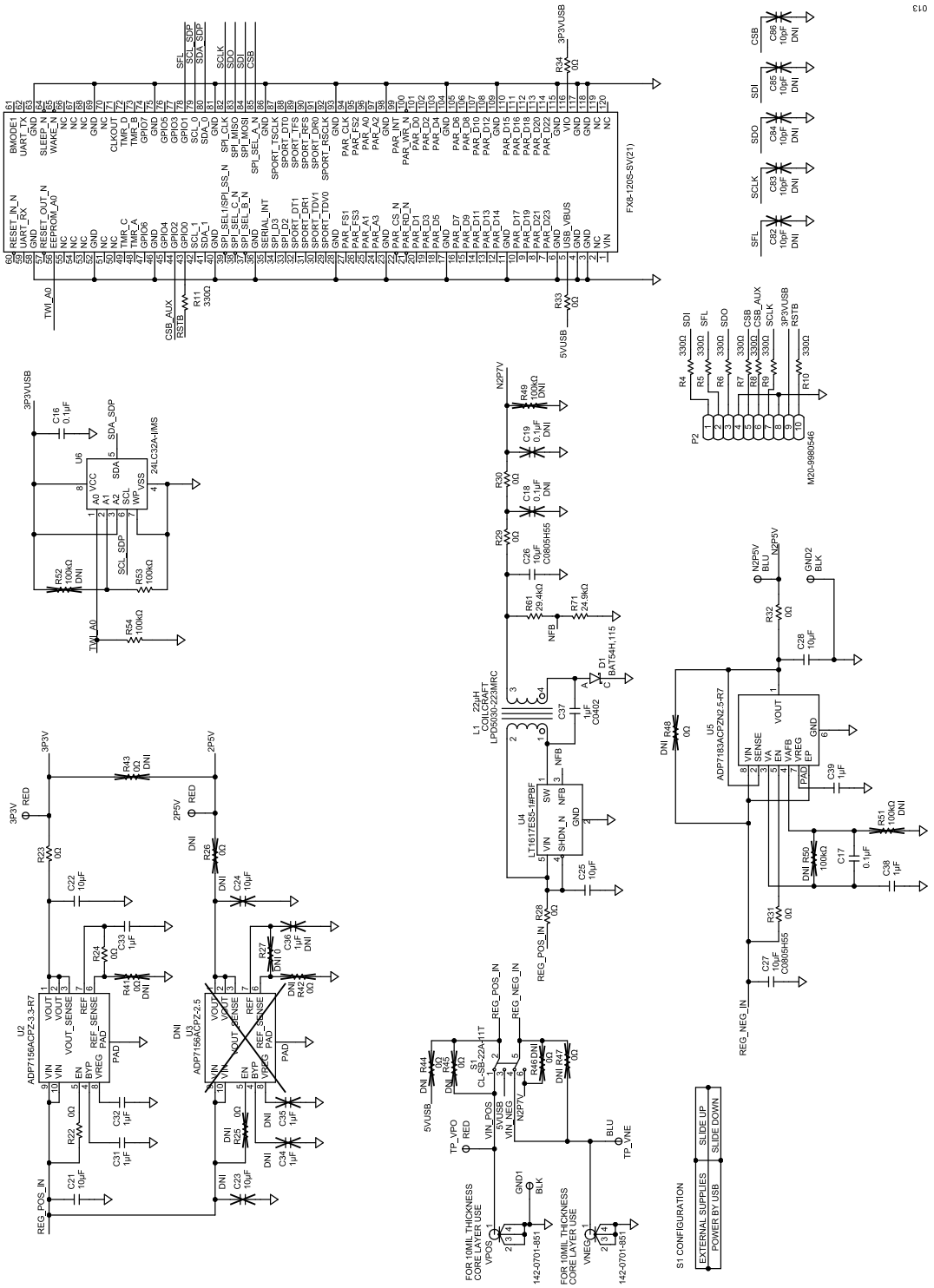


Figure 13. ADMV8526-EVALZ Schematic, Page 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

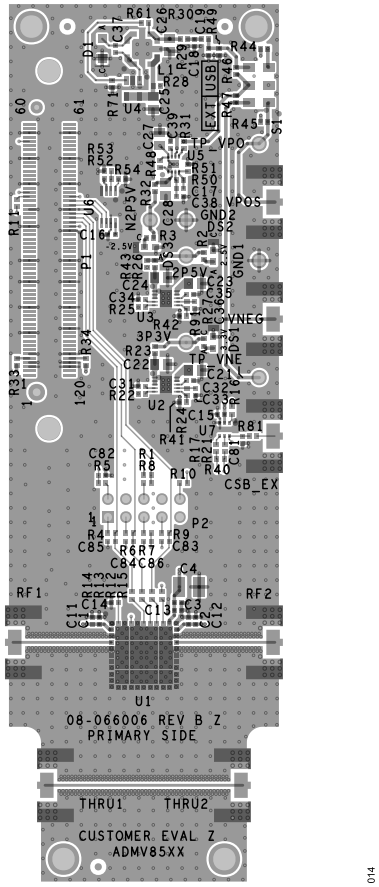


Figure 14. ADMV8526-EVALZ Layer 1

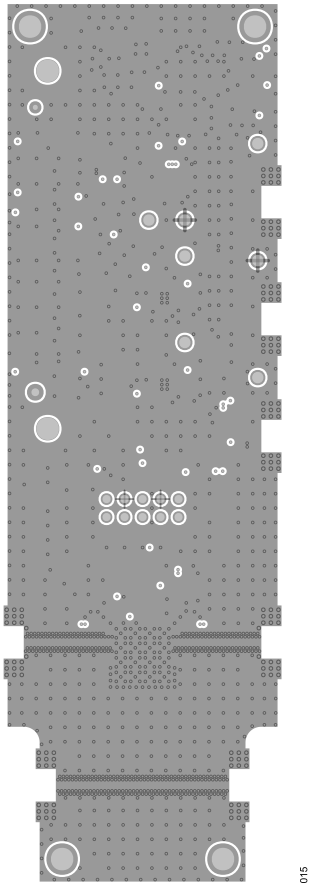


Figure 15. ADMV8526-EVALZ Layer 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

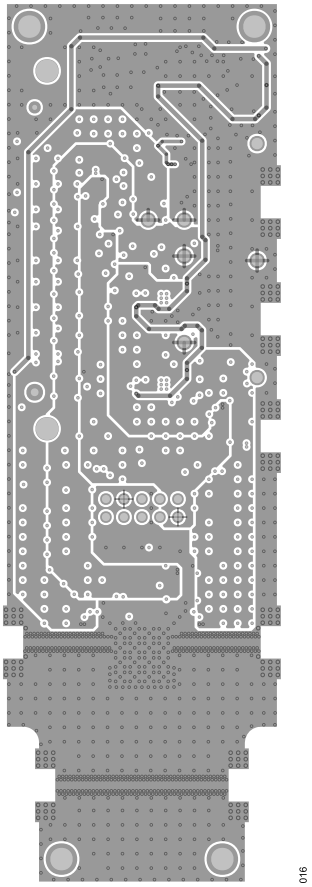


Figure 16. ADMV8526-EVALZ Layer 3

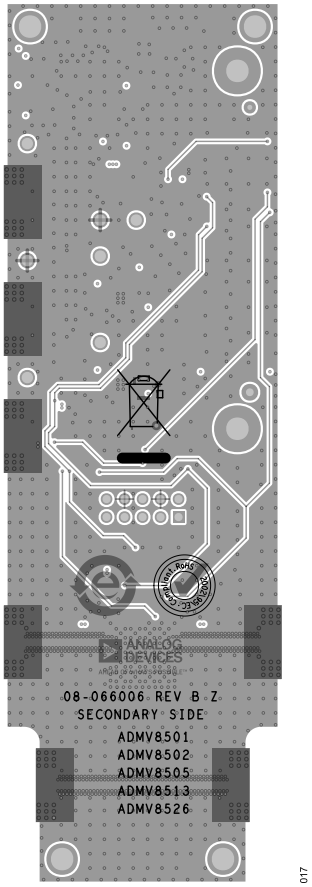


Figure 17. ADMV8526-EVALZ Layer 4

ORDERING INFORMATION

BILL OF MATERIALS

Table 2. ADMV8526-EVALZ

Quantity	Reference Designator	Description	Manufacturer	Part Number
3	2P5V, 3P3V, TP_VPOS	Test points, red	Components Corporation	TP-104-01-02
2	GND1, GND2	Test points, black	Components Corporation	TP-104-01-00
2	N2P5V, TP_VNEG	Test points, blue	Components Corporation	TP-104-01-06
5	CSB_EXT, RF1, RF2, VNEG, VPOS	Connectors, edge launch, SMA	Cinch Connectivity	142-0701-851
3	C1 to C3	Capacitors, 100 pF, 50 V, 5%, 0402	Johanson Dielectrics	500R07N101JV4T
7	C11 to C17	Capacitors, 0.1 µF, 16 V, 5%, 0402	Kemet	C0402C104J4RACTU
6	C21, C22, C25 to C28	Capacitors, 10 µF, 16 V, 10%, 0805	Samsung	CL21B106KOQNNNE
6	C31 to C33, C37 to C39	Capacitors, 1 µF, 6.3 V, 10%, 0402	Murata	GRM155R70J105KA12D
1	C4	Capacitor, 47 µF, 10 V, 10%, 1210	Murata	GRM32ER71A476KE15L
1	D1	Diode, BAT54H, 30V, SOD123F	NXP Semiconductor	BAT54H,115
3	DS1 to DS3	LED, LTST-C190GKT, Green, 0603	Lite-On Technology	LTST-C190GKT
1	L1	Coupled Inductor, 22uH, 20%	Coilcraft	LPD5030-223MRC
1	P1	Connector, vertical, surface-mount technology (SMT), 120-pin	Hirose Electric Co.	FX8-120S-SV(21)
1	P2	Connector, vertical, header, 10-pin	Harwin Inc.	M20-9980546
11	R1 to R11	Resistors, 330 Ω, 1/10 W, 5%, 0402	Panasonic	ERJ-2GEJ331X
6	R12 to R17	Resistors, 33 Ω, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF33R0X
11	R21 to R24,R28 to R34	Resistors, 0 Ω, 1/16 W, 0402	Stackpole	RMCF0402ZT0R00
2	R53, R54	Resistors, 100 kΩ, 1/16 W, 5%, 0402	Yageo	RC0402JR-07100KL
1	R61	Resistor, 29.4 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF2942X
1	R71	Resistor, 24.9 kΩ, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF2492X
1	R81	Resistor, 49.9 Ω, 1/10 W, 1%, 0402	Panasonic	ERJ-2RKF49R9X
1	R91	Resistor, 750 Ω, 1/16 W, 5%, 0402	Panasonic	ERJ-2GEJ751X
1	S1	Switch, mechanical, slide, DPDT, 0.2 A	Nidec Copal Electronics	CL-SB-22A-11T
1	U1	IC, 1.25 GHz to 2.60 GHz, digitally tunable band-pass filter	Analog Devices	ADMV8526ACCZ
1	U2	IC, LDO regulator, 3.3 V	Analog Devices	ADP7156ACPZ-3.3-R7
1	U4	IC, inverting dc-to-dc converter	Analog Devices	LT1617ES5-1#PBF
1	U5	IC, LDO regulator, –2.5 V	Analog Devices	ADP7183ACPZN2.5-R7
1	U6	IC, 24LC32A, EEPROM, I^2C	Microchip Technology	24LC32A-I/MS
1	U7	IC, CMOS SPDT switch	Analog Devices	ADG749BKSZ
2	C18, C19	Capacitors, 0.1 µF, 16 V, 5%, 0402, do not install (DNI)	Kemet	C0402C104J4RACTU
2	C23, C24	Capacitors, 10 µF, 16 V, 10%, 0805, DNI	Samsung	CL21B106KOQNNNE
3	C34 to C36	Capacitors, 1 µF, 6.3 V, 10%, 0402, DNI	Murata	GRM155R70J105KA12D
6	C81 to C86	Capacitor, 10 pF, 50 V, 5%, 0402, DNI	Yageo	CC0402JRNPO9BN100
12	R25 to R27,R40 to R48	Resistors, 0 Ω, 1/16 W, 0402, DNI	Stackpole	RMCF0402ZT0R00
4	R49 to R52	Resistors, 100 kΩ, 1/16 W, 5%, 0402, DNI	Yageo	RC0402JR-07100KL
2	THRU1, THRU2	Connectors, edge launch, SMA, DNI	Cinch Connectivity	142-0701-851
1	U3	IC, LDO regulator, 2.5 V, DNI	Analog Devices	ADP7156ACPZ-2.5-R7

ORDERING INFORMATION

NOTES

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.