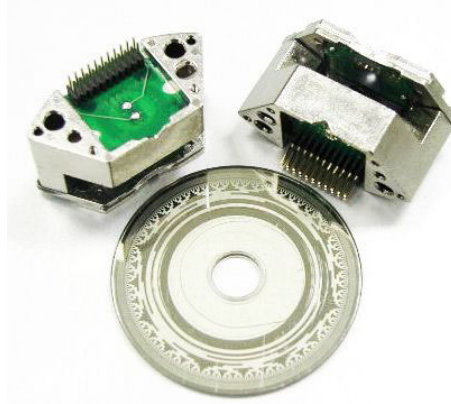


AEAS-7000

Ultra-precision 16 bit Gray Code Absolute Encoder Module



Data Sheet



Description

The encoder IC consists of 13 signal photo diode channels and 1 monitor photo diode channel and is used for the optical reading of rotary carriers (i.e., discs). The photodiodes are accompanied with precision amplifiers plus additional circuitry.

The monitor channel is used to drive a constant current source for the highly collimated IR illumination system.

Functional Description

Background

The 13 signal channels are set up as:

1. Two precision defining signals (A0, A09), which are two 90° electrical shifted sine, cosine signals. These signals are conditioned to be compensated for offset and gain errors. After conditioning they are on chip interpolated
2. 11 analog (A1-A11) channels which are directly digitized by precision comparators with hysteresis tracking. The digitized signals are called D1-D11.

An internal correction and synchronization module allows the composition of a true 16 bit Gray code by merging the data bits of (1) and (2) by still keeping the code monotonic.

There is a Gray code correction feature for this encoder. This Gray code correction can be disabled/enabled by the pin KORR.

The gain and offset conditioning value of the sine and cosine signals are preloaded on-chip by factory. This will compensate for mechanical sensor misalignment error.

Features

- Minimum mechanical alignment during installation
- Two Sine/Cosine true differential outputs with 1024 periods for unit alignment
- Integrated highly collimated illumination system
- 11 digital tracks plus 2 sin/cos tracks generate precise 16 bit Gray code
- Ultra fast, 1 μ s cycle for serial data output word equals 16 MHz
- On-chip interpolation and code correction
- MSB can be inverted for changing the counting direction
- Internally built-in monitor track for tracking the light level of the LED.
- Watch dog with alarm output
- -25°C to +85°C operating temperature

Applications

- Rotary application up to 16 bit/360° absolute position
- Linear positioning system
- Cost effective solution for direct integration into OEM systems

Signal-Channels A1-A11

The photocurrent of the photo diodes is fed into a trans-impedance amplifier. The analog output of the amplifier has a voltage swing of (dark/light) about 1.3 V. Every output is transformed by precision comparators into digital signals (D1-D11). The threshold is at $V_{DD}/2$ (=Analog-reference), regulated by the monitor channel.

Monitor Channel with LED Control at Pins LEDR and LERR

The analog output signal of the monitor channel is regulated by the LED current. An internal bipolar transistor sets this level to $V_{DD}/2$ (control voltage at pin LEDR). Thus the signal swing of each output is symmetrical to $V_{DD}/2$ (=Analog-reference)

The error bit at pin LERR is triggered if the V_e of the internal bipolar transistor is larger than $V_{DD}/2$.

Signals Channels A0, A09 with Signal Conditioning and Calibration

These two channels give out a sine and cosine wave, which are 90 degree phase shifted. These signals have amplitudes which are almost constant due to the LED current monitoring. Due to amplifier mismatch and mechanical misalignment, the signals have gain and offset errors. These errors are eliminated by an adaptive signal conditioning circuitry. The conditioning values are on-chip preprogrammed by factory. The analog output signals of A0 and A09 are supplied as true-differential voltage with a peak to peak value of 2.0 V at the pins A09P, A09N, A0P, A0N.

Interpolator for Channels A0,A09

The interpolator generates the digital signals D0,D09 and D-1 to D-4. The interpolated signals D-1 to D-4 extend the 12 bit Gray code of the signals D11....D0 to form a 16 bit Gray code.

D0 and D09 are digitized from A0 and A09. The channels A0-A11 and A09 have very high dynamic bandwidth, which allows a real time monotone 12 bit Gray code at 12000 RPM.

The interpolated 16 bit Gray code can be used up to 1000 RPM only. At more than 1000 RPM, only the 12 bit Gray code from the MSB side can be used.

LSB Gray Code Correction (Pin KORR)

This function block synchronizes the switching points for the 11 bit Gray code of the digital signals D1 to D11 with D0 and D09 (digitized signal of A0 and A09).

This Gray code correction only works for the 12 bit MSB(4096 steps per revolution).

The correction is not for the 4 excess interpolated bits of the 16 bit Gray code.

Gray code correction can be switched on or off by putting the pin KORR =1(on) or =0(off).

MSBINV and DOUT Pins

The serial interface consists of a shift register. The most significant bit, MSB (D11) will always be sent first to DOUT. The MSB can be inverted (change code direction) by using pin MSBINV.

DIN and NSL Pins

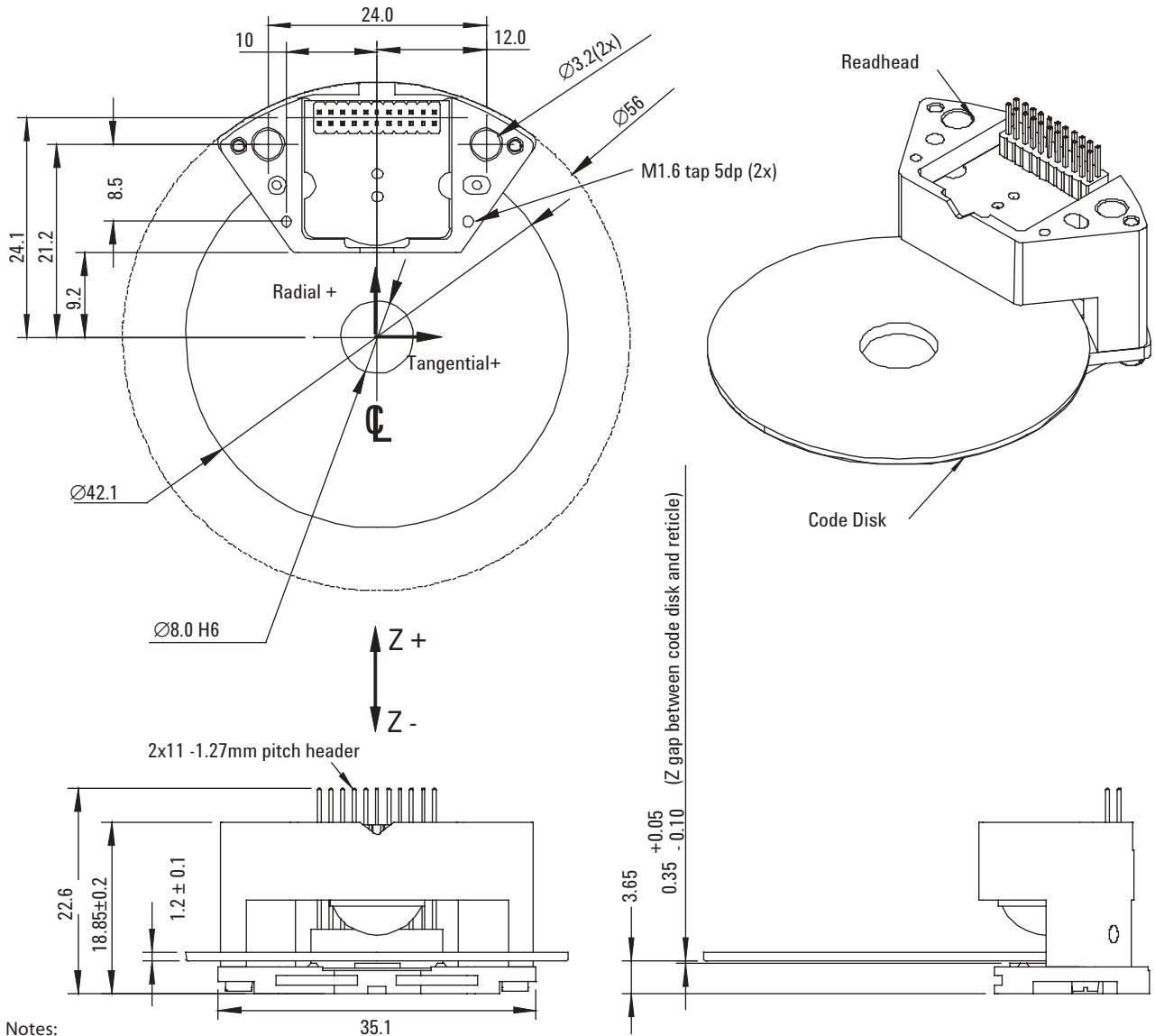
The serial input DIN allows the configuration as ring register for multiple transmissions or for cascading 2 or more encoders. DIN is the input of the shift register that shifts the data to DOUT.

The NSL pin controls the shift register, to switch it between load (1) or shift (0) mode. Under load mode, DOUT will give the logic of the MSB, i.e., D11.

Under shift mode (0), coupled with the SCL, the register will be clocked, and gives out the serial word output bit by bit. As the clock frequency can be up to 16 MHz, the transmission of the full 16 bit word can be done within 1 μ s.

Valid data of DOUT should be read when the SCL clock is low. Please refer to timing diagram (Figure 3).

Package Dimensions



Notes:

1. 3rd Angle Projection
2. Dimensions are in millimeters
3. Unless otherwise specified, the tolerances are: XX. – ± 0.3 ; XX.X – ± 0.1 ; XX.XX – ± 0.03
4. Codewheel and readhead mounting tolerances for radial, tangential and Z gap are:
 - Radial : $\pm 50 \mu\text{m}$
 - Tangential : $\pm 40 \mu\text{m}$
 - Z Gap : $\pm 50 \mu\text{m}$

Figure 1. Package Dimensions

Device Selection Guide ¹

Part Number	Resolution	Operating Temperature (°C)	Output	Output Code	DC Supply Voltage (V)
AEAS-7000-1GSD0	13 bit	-25 to 85	Serial	Gray Code	+4.5 to +5.5
AEAS-7000-1GSG0	16 bit	-25 to 85	Serial	Gray Code	+4.5 to +5.5

Notes:

1. For other options of absolute encoder module, please refer to factory.

Absolute Maximum Ratings ^{1, 2}

Parameter	Symbol	Limits	Units
DC Supply Voltage	VD	-0.3 to + 6.0	V
Input Voltage	V _{in}	-0.3 to +VD +0.3	V
Output Voltage	V _{out}	-0.3 to +VD +0.3	V
Relative Air Humidity (non-condensing)	RH	85	%
Operating Temperature	T _A	- 25 to +85	°C
Storage Temperature	T _S	- 35 to +85	°C

Notes:

- Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Condition

Parameter	Symbol	Values			Units	Notes
		Min.	Typ.	Max.		
DC Supply Voltage	VD	+ 4.5	+ 5.0	+5.5	V	1
Operating Temperature	T _A	- 25	25	+85	°C	
Input High Level	V _{IH}	0.7*VD		VD	V	
Input Low Level	V _{LI}	0		0.3*VD	V	

Notes:

- Voltage ripple of supply voltage, V_{ripple}, should be within 100mVpp or less for improved accuracy.

Electrical Characteristics

Electrical Characteristics over Recommended Operating Range, typical at TA=25 °C and VD = 5V

Parameter	Symbol	Condition	Values			Units
			Min	Typical	Max	
Total Operating Current	I _{total}			25		mA
Digital Input-Pull Down Current	I _{pd}		-20		-5	μA
Digital Input-Pull Up Current	I _{pu}		30		160	μA
Digital Output-H-Level	V _{OH}	I _{OH} = 2 mA	VD -0.5 V		VD	V
Digital Output-L-Level	V _{OL}	I _{OL} = - 2 mA	0		0.5	V
SCL Clock Frequency	f _{SCL}				16	MHz
Duty Cycle SCL Clock	T _{LH}	T _{LH} = H/(L+H)	0.4		0.6	
Accuracy within one revolution ^{1, 2, 3}		f _{SCL} = 5MHz RPM =80 V _{ripple} <50mVpp			±2 bit	
Signal frequency of A0, A09	f _{A0} , f _{A09}				250	kHz

Notes:

- LSB accuracy will also depend on mechanical precision of the shaft, bearings, hub etc.
Final accuracy of the encoder module is dependent on the precision of the total assembly.
- Accuracy would be influenced by installation control and the bearing and shaft type being used.
- Other test conditions to determine accuracy are briefly listed as follows:
 - At nominal radial, tangential and gap position
 - On dual preloaded bearing with absolute assembly total runout of not exceeding 0.01 mm TIR
 - Both VDD & VDDA RC filters placed not more than 20mm from header pins

Pin Description

No.	Pin Name	Description	Function	Notes1
1	NC		Do not use. Internally connected to cathode of LED	
2	KORR	Digital-input	1 = Gray Code Correction Active	CMOS, internal pu
3	PROBE_ON	Digital-Input	Do not use	CMOS, internal pd
4	PCL	Digital Input Positive edge	Do not use	CMOS, internal pu
5	STCAL	Digital Input Positive edge Negative edge	Do not use unnecessarily	CMOS, internal pd
6	MSBINV	Digital-Input	1 = Most Significant Bit, MSB, inverted	CMOS, internal pd
7	DIN	Digital Input	Shift Register Input. Use for cascading only.	CMOS, internal pd
8	NSL	Digital-Input	Shift-register Shift (=0) / Load(=1) Control	CMOS, internal pu
9	SCL	Digital-Input Positive Edge	Shift-register Clock	CMOS, internal pu
10	DOUT	Digital Output	Shift-Register Data Out (MSB first)	CMOSS, 2mA
11	DO	Digital Output	DO signal	CMOS, 2mA
12	DPROBE	Digital Output	D09 signal	CMOS, 2mA
13	VDD	Supply Voltage	+5V Supply Digital	
14	GND	Ground for supply voltage	GND for 5V supply analog/digital	
15	A09P	Analog Output	A09 positive(+True diff.)	CMOS, analog out
16	GND	Ground for supply voltage	GND for 5V supply analog/digital	
17	A0P	Analog Output	A0 positive(+True diff.)	CMOS, analog out
18	A09N	Analog Output	A09 negative(-True diff.)	CMOS, analog out
19	VDDA	Supply Voltage	+5V Supply Analog	
20	A0N	Analog Output	A0 negative (- True dif)	CMOS, analog out
21	LERR	Digital Output	IR-LED Current Limit Signal	CMOS, 2mA
22	LEDR	Analog Output	Do not use	CMOS, analog out

Notes:

1. Internal pu/pd = internal pull-up (typ. 50 μ A)/ pull-down (typ. 10 μ A) CMOS-transistor-Rs

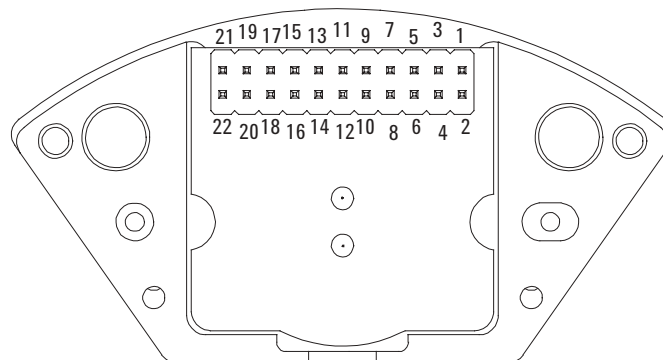


Figure 2. Pinout Configuration

ESD WARNING: HANDLING PRECAUTIONS SHOULD BE TAKEN TO AVOID STATIC DISCHARGE.

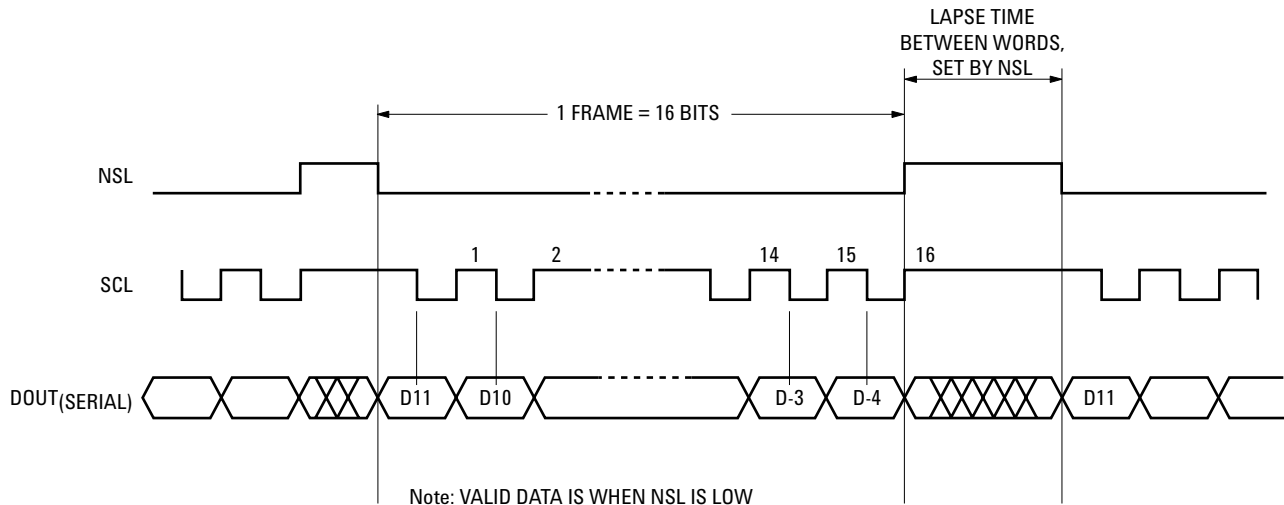


Figure 3. Timing Diagram

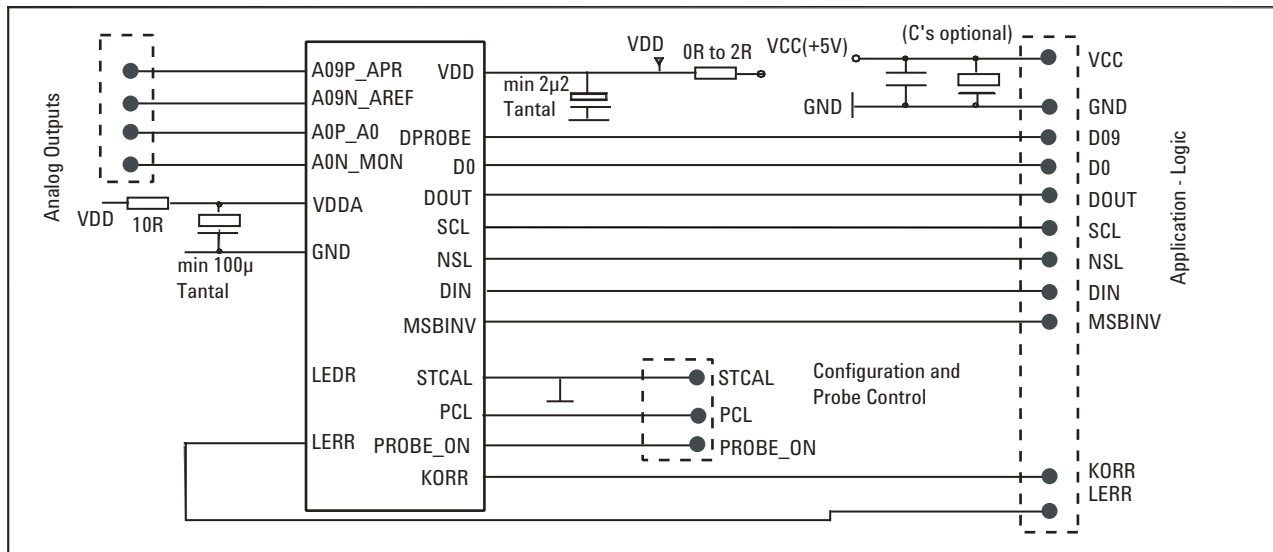


Figure 4. Schematic for using AEAS-7000

Using the AEAS-7000

IMPORTANT NOTE:

The RC-filter combination, especially on VDDA, is used to filter spikes and transients and is strongly recommended. It is advised that the tantalum caps be put as close to the VDD and VDDA pins as possible.

It is recommended to ground the PROBE_ON pin during normal operation.

Leave PCL unconnected.

A09N and A0N are the negative cosine and sine waves, the negative versions of A09P and A0P.

D0 is used to check the D0 signal. D0 is the digitized signal of A0. DPROBE is used to check D09, the digitized signal of A09. Recommended to be used for testing purpose only.

KORR is for Gray Code correction for 12 bits - resolution only.

MSBINV is for user to change between counting up and counting down for a given rotating direction. MSB(D11) will always be sent out to DOUT first.

LEDR, do not connect to this pin.

LERR will be high when the light output perceived by the photo diode array is low, and the LED current is under overdrive mode. This is an indicator when light intensity is at a critical stage affecting the performance of the encoder.

It is caused by contamination of the codewheel or LED degradation.

Operation

1. After powering up the unit using $V_D = +5\text{ V}$ and connecting GND to ground, trigger input pins NSL and SCL using the timing diagram (Figure 3). NSL is a control pin for the internal shift register. NSL=1 is load mode while NSL=0 is shift mode for the shift register. When NSL=0 and combined with clock pulses, the serial Gray code will be shifted out to DOUT bit by bit per every clock pulse. Valid data of DOUT should be sampled at the falling edges of the clock pulses.
2. The 16 bit serial Gray code can be tapped out from the pin DOUT, most significant bit (D11) first. The rate of the 16 bit Gray code serial transfer rate is dependent on the SCL clock frequency. The faster the clock, the faster the transfer rate. The maximum clock rate the AEAS-7000 can take is 16 MHz, which means the entire 16 bit Gray code can be serially transferred out in $1\ \mu\text{s}$.
3. Whenever NSL is high, the DOUT will have the logic of the MSB (D11). After NSL goes low, the number of bits being transferred out will depend on the number of clock pulses given to SCL. The default is 16 bit clock pulses for the 16 bit Gray code. If for other application where another number other than 16 is needed, just supply the corresponding number of clock pulses to the SCL, e.g., 12 bit, 13 bit, 14 bit or 15 bit, and the corresponding length of Gray code words with the corresponding resolution can be obtained.

Plug & Play Hub-Shaft design

Figure 5 details the hub-shaft design of which the dimensions must be strictly followed for the plug & play feature of the AEAS-7000 to work. In order to secure the code disk to the hub, an adhesive should be utilised. It is recommended to use DELO-DUOPOX, 1895 from DELO or its equivalence. Stainless steel is recommended as the hub-shaft material.

A more detailed instruction for AEAS-7000 installation consideration can be found in AEAS-7000 application note.

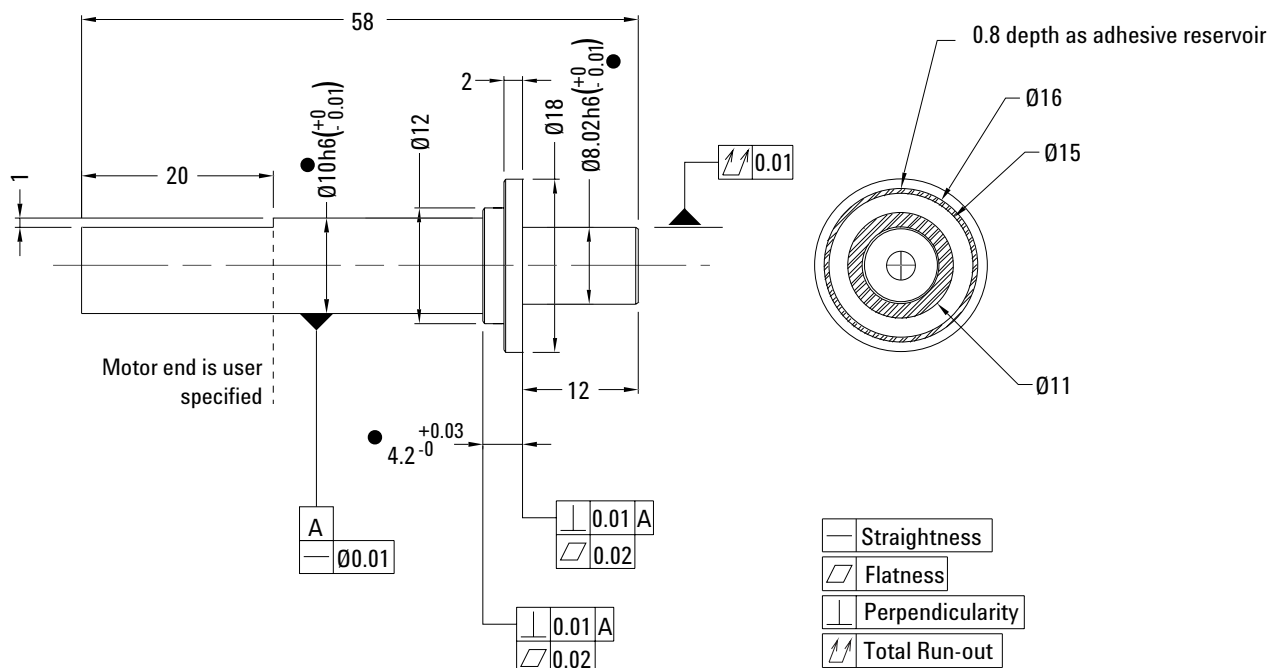


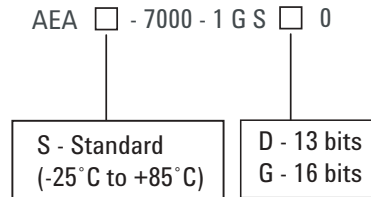
Figure 5. Design reference for code disk hub-shaft

Ordering Information

AEAS-7000-1GSD0	Single-turn, -25 to +85°C, detached encoder set, 5V, serial, 13 bit
AEAS-7000-1GSG0	Single-turn, -25 to +85°C, detached encoder set, 5V, serial, 16 bit
HEDS-8933	Mechanical Alignment Tool for AEAS-7000

Note:

For alignment process, please refer to Avago Technologies website (www.avagotech.com) for application note or contact factory.



Legend

1 = 5V

G = Gray code

S = serial output mode

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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