

Product Summary

V _{BR_MIN}	I _{PP_MAX}	C _{T_Typ}
5V	10.5A	0.3pF

Description

The DIODES D3V3Z1BD2CSP is an extremely low capacitance of 0.3 pF ESD protection device designed specifically to protect high-speed differential lines. These devices can also be used for EOS protection due to their high peak pulse current capability (10.5A, $t_P = 8/20\mu s$). It has excellent ESD protection features, highlighted by low peak ESD clamping voltage and high ESD withstand voltage (+/-20kV contacts per IEC 61000-4-2). The small package DSN 0.60 x 0.30 x 0.30 gives designers the flexibility to protect a single line in applications.

Applications

- USB3.0, USB3.1 and USB3.2 Gen 2 x 2
- USB Type-C®
- HDMI™ 1.4, HDMI™ 2.0 and HDMI™ 2.1
- Thunderbolt 2, thunderbolt 3
- 10G ethernet
- WiFi-6 AnT

Features

- Provide Transient Protection for The Protected Line to IEC 61000-4-2 (ESD) Air $\pm 20kV$, Contact $\pm 20V$ IEC 61000-4-5 (surge) 10.5A (8/20 μs)
- Bidirectional ESD Protection of One Line
- Extremely Low Capacitance Cd = 0.3pF
- Extremely Low Clamping Voltage to Protect Sensitive I/Os
- Low Reverse Leakage Current: 50nA max at $V_R = 3.3V$
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative. <https://www.diodes.com/quality/product-definitions/>**

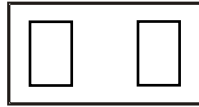
Mechanical Data

- Package: X2-DSN0603-2
- Package Material: Chip Scale Package
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: NiAu Bump. Solderable per MIL-STD-202, Method 208 ^(e4)
- Weight: 0.0002 grams (Approximate)

X2-DSN0603-2



Top View



Bottom View



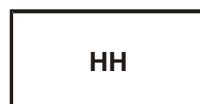
Device Schematic

Ordering Information (Note 4)

Part Number	Package	Marking Code	Reel Size (Inches)	Tape Width (mm)	Packing	
					Qty.	Carrier
D3V3Z1BD2CSP-7	X2-DSN0603-2	HH	7	8	10,000	Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See http://www.diodes.com/quality/lead_free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



HH = Product Type Marking Code

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit	Condition
Peak Pulse Power Dissipation	PPP	55	W	8/20μs, per Figure 3
Peak Pulse Current	I _{PP}	10.5	A	8/20μs, per Figure 3
ESD Protection – Air Discharge	V _{ESD_AIR}	±20	kV	IEC61000-4-2 Standard
ESD Protection – Contact Discharge	V _{ESD_CONTACT}	±20	kV	IEC61000-4-2 Standard

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Package Power Dissipation (Note 5)	P _D	250	mW
Thermal Resistance, Junction to Ambient (Note 5)	R _{θJA}	500	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ.	Max	Unit	Test Conditions
Reverse Standoff Voltage	V _{RWM}	—	—	3.3	V	—
Channel Leakage Current (Note 6)	I _{RM}	—	—	50	nA	V _{RWM} = 3.3V
Clamping Voltage	V _{CL}	—	5.3	—	V	I _{PP} = 10.5A, t _P = 8/20μs
		—	5	—		I _{PP} = 16A, TLP, t _P = 100ns
Breakdown Voltage	V _{BR}	5	—	9	V	I _R = 1mA
Differential Resistance	R _{DYN}	—	0.14	—	Ω	TLP = 4A to 16A, t _P = 100ns
Channel Input Capacitance	C _T	—	0.3	0.34	pF	V _R = 0V, f = 1MHz

- Notes:
5. Device mounted on FR-4 PCB pad layout (2oz copper) as shown on Diodes Incorporated's suggested pad layout, which can be found on our website at <http://www.diodes.com/package-outlines.html>.
 6. Short duration pulse test used to minimize self-heating effect.

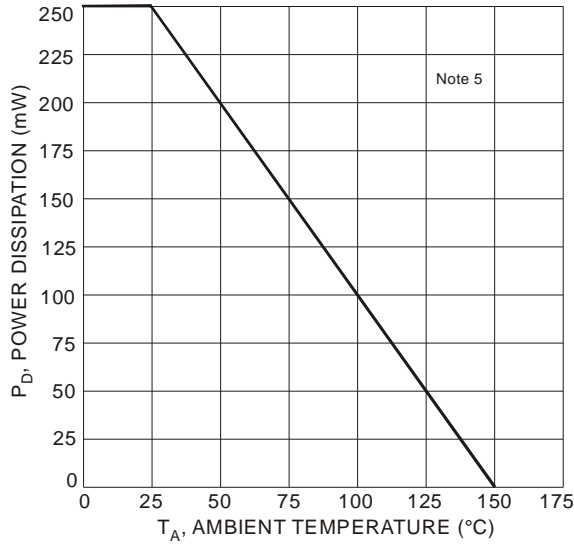


Figure 1 Power Derating Curve

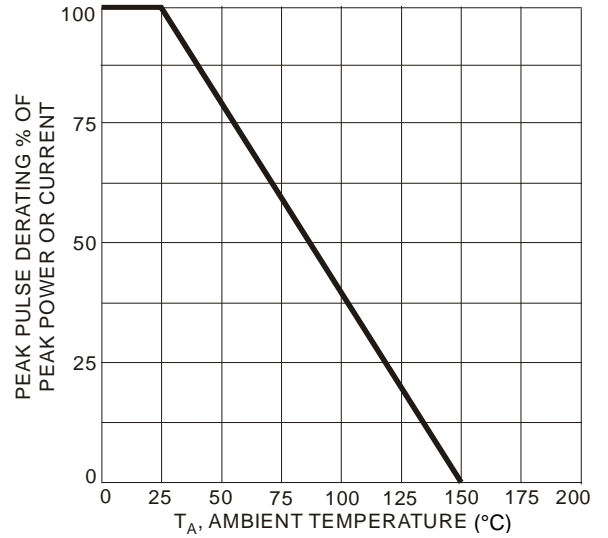


Figure 2 Pulse Derating Curve

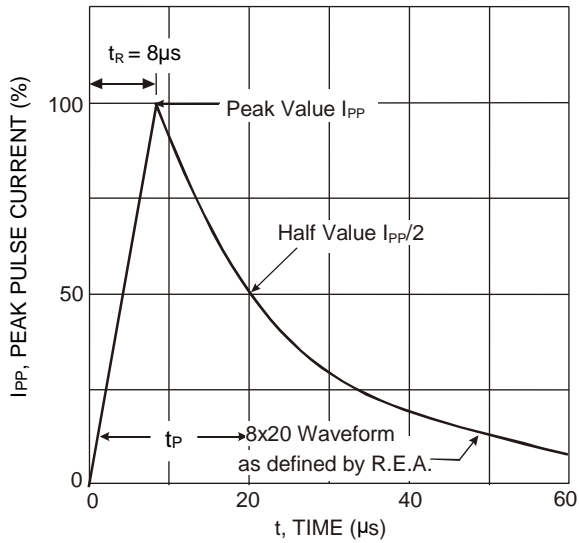


Figure 3 Pulse Waveform

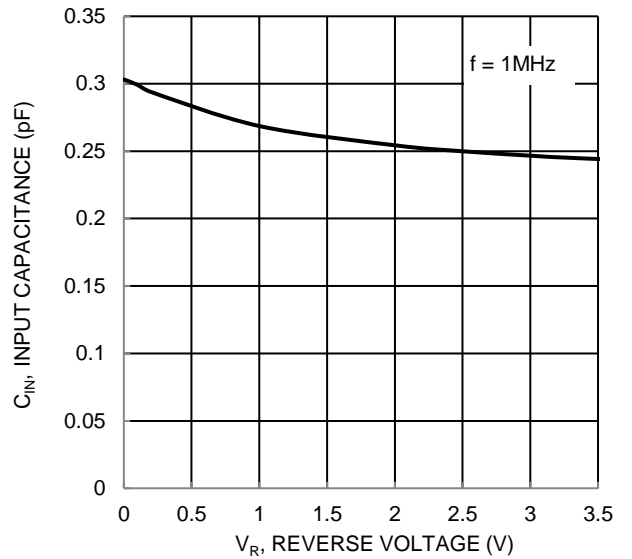


Figure 4 Typical Junction Capacitance

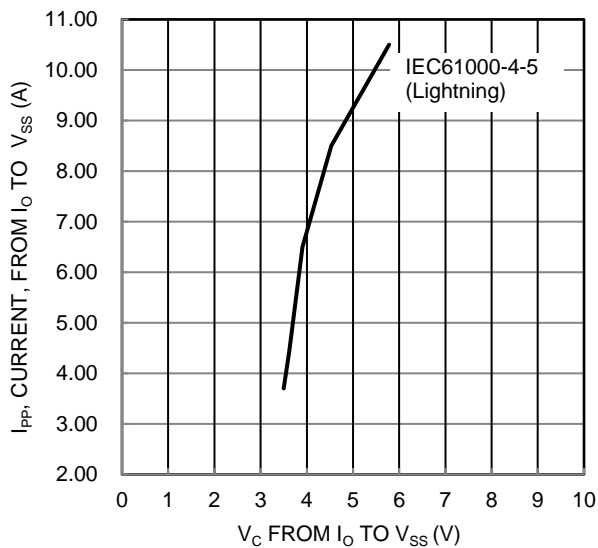


Figure 5 Clamping Voltage Characteristic

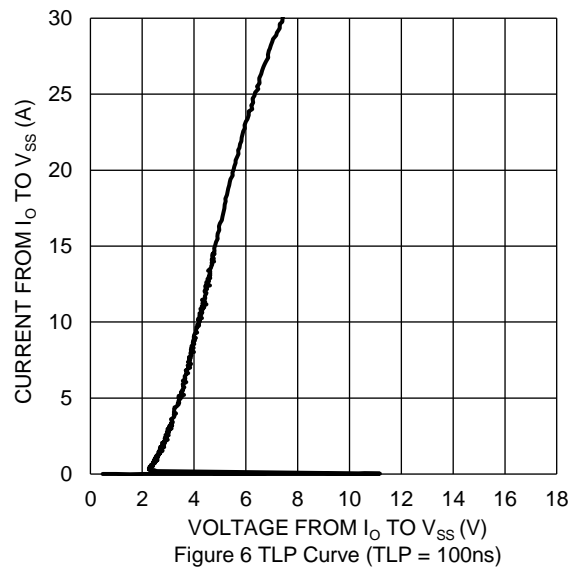
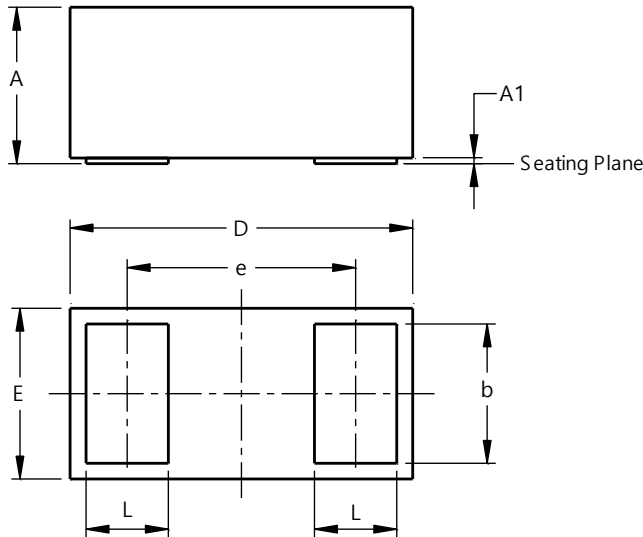


Figure 6 TLP Curve (TLP = 100ns)

Package Outline Dimensions (Note 7)

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DSN0603-2



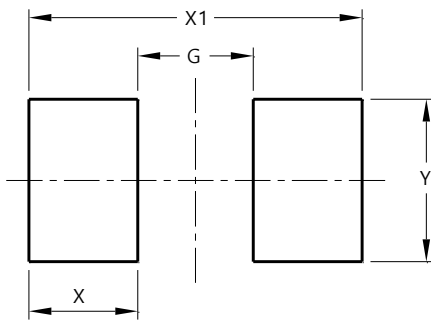
X2-DSN0603-2			
Dim	Min	Max	Typ
A	0.280	0.320	0.300
A1	0.00	0.020	0.010
b	0.220	0.260	0.240
D	0.575	0.625	0.600
E	0.275	0.325	0.300
e	-	-	0.400
L	0.120	0.160	0.140
All Dimensions in mm			

Note 7: Device side walls are electrically active bare silicon. Avoid contact of solder or flux on the side walls during the PCB assembly process.

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DSN0603-2



Dimensions	Value (in mm)
G	0.206
X	0.194
Y	0.291
X1	0.594

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