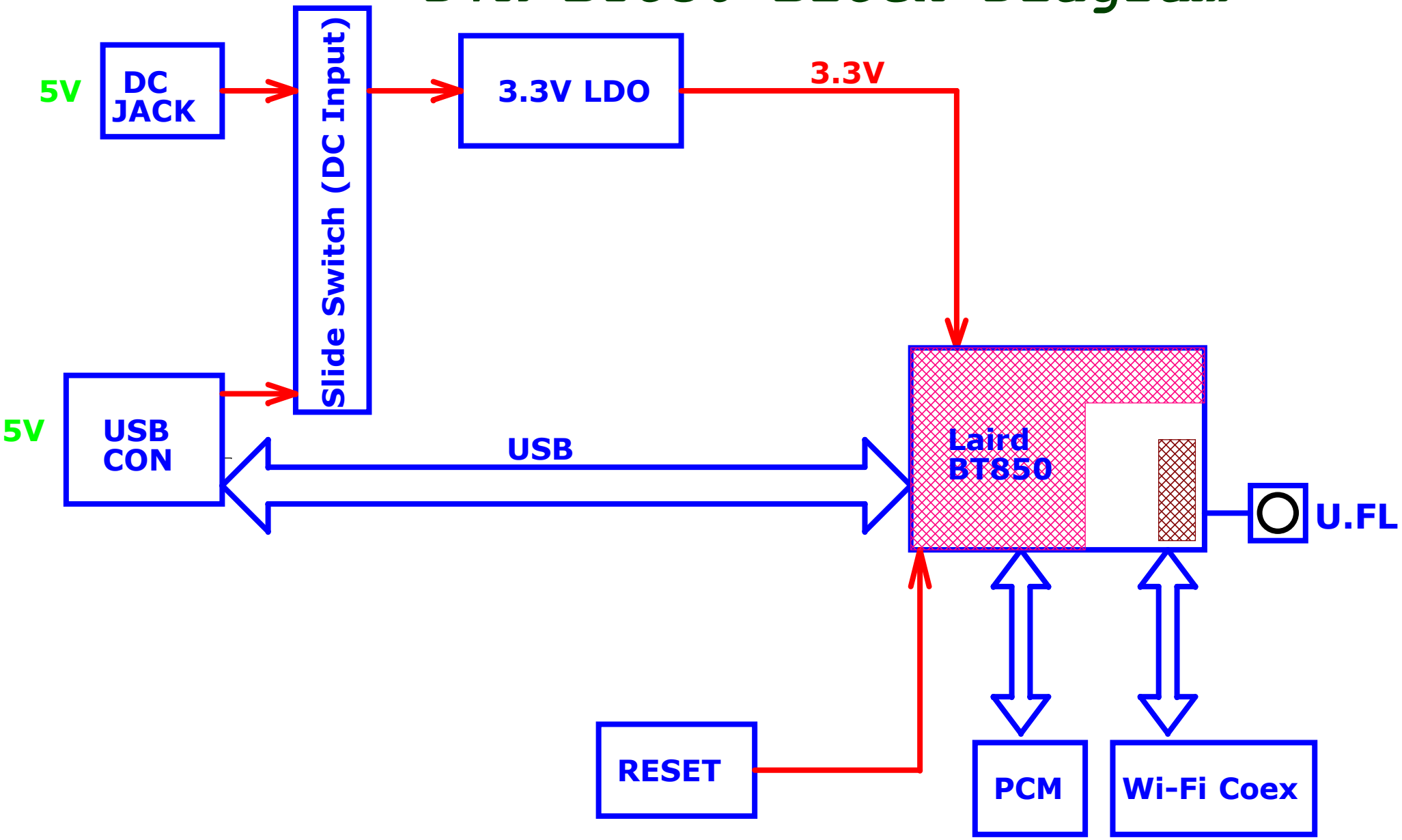
DVK-BT850 Block Diagram



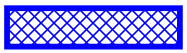
Laird Technologies CS			
Project Name : DVK-BT850	Schematic Name : BLOCK DIAGRAM		Drawing By : Jacky Kuo
Date : Wednesday, August 23, 2017	Sheet : 1 of 3		Revision : 1.0

DATE	REVISION NUMBER	INITIALS	Initial Release
5/16/2017	A0	Jacky Kuo	Initial draft
7/12/2017	B0	Jacky Kuo	1. Change R1 and R2 package to 0402 size 2. Change C3 - 6.8pF to 1.2nH 3. Added LED4 with wired to GPIO_5
2017/08/23	1.0	Jacky Kuo	MP release

PCB design specification

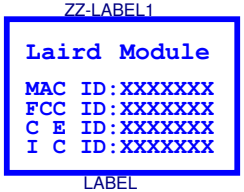
1. Substrate: FR4 ROHS compliant, High TG 140 degree.
2. Solder mask, color=GREEN, Silkscreen color=WHITE
3. Surface finish to be Immersion Nickel/Gold (ENIG) with 1-2 u"
4. Start with 1 oz. copper on all layers.

ZZ-PCB1



PCB

ZZ-LABEL1



LABEL

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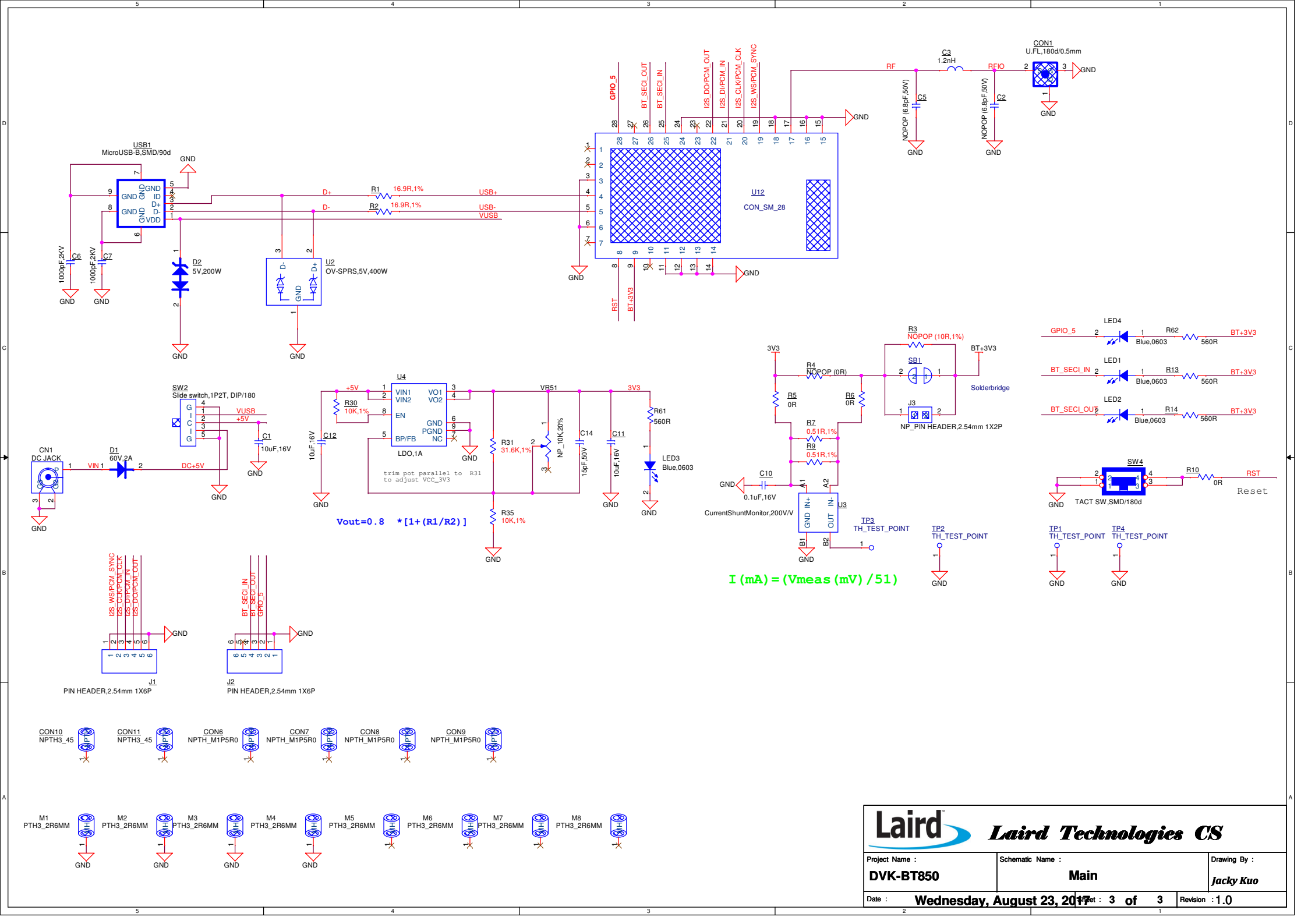
Project Name :	Schematic Name :	Drawing By :
CYW20704 USB DVK	HISTORY	Jacky Kuo
Date : Wednesday, August 23, 2017	Sheet : 2 of 3	Revision : 1.0



Laird

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Project Name :	Schematic Name :	Drawing By :
DVK-BT850	Main	Jacky Kuo

Date :	Sheet :	Revision :
Wednesday, August 23, 2017	3 of 3	1.0