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**Vishay Siliconix** 

AUTOMOTIVE

RoHS

COMPLIANT HALOGEN

FREE

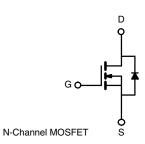
# Automotive N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	100				
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.0095				
I <sub>D</sub> (A)	120				
Configuration	Single				
Package	TO-263				



### FEATURES

- TrenchFET® power MOSFET
- · Package with low thermal resistance
- AEC-Q101 qualified <sup>d</sup>
- 100 %  $\rm R_g$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \degree C$ , unless otherwise noted)							
PARAMETER		SYMBOL	LIMIT	UNIT			
Drain-Source Voltage		V <sub>DS</sub>	100	V			
Gate-Source Voltage		V <sub>GS</sub>	± 20	v			
Continuous Drain Current	$T_{C} = 25 \ ^{\circ}C \ ^{a}$	Ŀ	120				
Continuous Drain Current	T <sub>C</sub> = 125 °C	I <sub>D</sub>	73				
Continuous Source Current (Diode Conduct	tion) <sup>a</sup>	I <sub>S</sub>	120	А			
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	480				
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	73				
Single Pulse Avalanche Energy	L = 0.1 mm	E <sub>AS</sub>	266	mJ			
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	D	375	W			
Maximum Fower Dissipation ~	T <sub>C</sub> = 125 °C	P <sub>D</sub>	125	٧V			
Operating Junction and Storage Temperatu	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C				

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	LIMIT	UNIT			
Junction-to-Ambient	t PCB Mount <sup>c</sup>		40	°C/W			
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.4	0/10			

### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT		
Static		•					•	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub>	= 0, I <sub>D</sub> = 250 μA	100	-	-	v	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5	3.0	3.5	v	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, $V_{GS} = \pm 20$ V	-	-	± 100	nA	
		$V_{GS} = 0 V$	V <sub>DS</sub> = 100 V	-	-	1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = 100 \text{ V}, \text{ T}_{\text{J}} = 125 ^{\circ}\text{C}$	-	-	50	μA	
		$V_{GS} = 0 V$	$V_{DS}$ = 100 V, T <sub>J</sub> = 175 °C	-	-	150		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	120	-	-	Α	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A	-	0.0079	0.0095		
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	$I_D = 30 \text{ A}, T_J = 125 ^\circ\text{C}$	-	-	0.0190	Ω	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	0.0250		1	
Forward Transconductance b	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	99	-	S	
Dynamic <sup>b</sup>								
Input Capacitance	C <sub>iss</sub>			-	6915	8645		
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = 25 V$ , f = 1 MHz	-	635	795	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	280	350		
Total Gate Charge <sup>c</sup>	Qg			-	120	180		
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 50 \text{ V}, I_{D} = 85 \text{ A}$	-	30	-	nC	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	28.5	-		
Gate Resistance	Rg	f = 1 MHz		0.25	0.7	2.3	Ω	
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	$V_{DD} = 50 \text{ V}, \text{ R}_{\text{L}} = 0.6 \Omega$ $\text{I}_{\text{D}} \cong 85 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 2.5 \Omega$		-	21	32	- ns	
Rise Time <sup>c</sup>	t <sub>r</sub>			-	24	36		
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	52	78		
Fall Time <sup>c</sup>	t <sub>f</sub>			-	16	24		
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	480	Α	
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 85 A, V <sub>GS</sub> = 0		-	0.9	1.5	V	

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

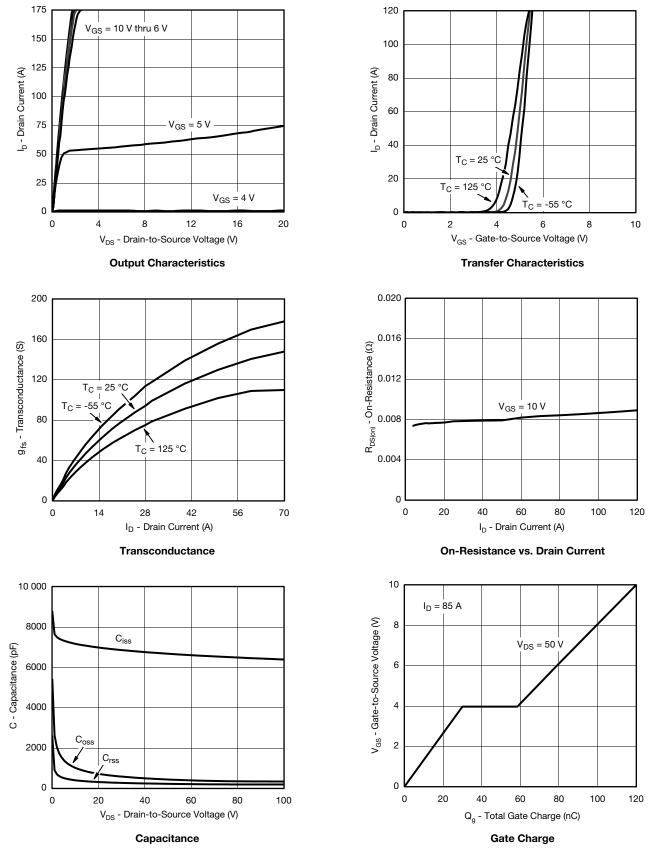
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**ISHAY** 

SQM120N10-09

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## **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



S15-1875-Rev. C, 10-Aug-15

3

Document Number: 71515

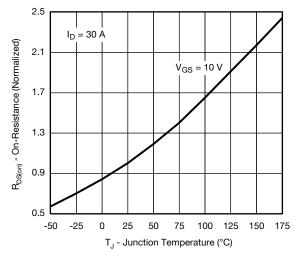
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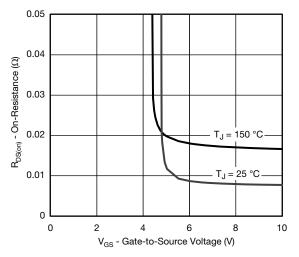
SQM120N10-09



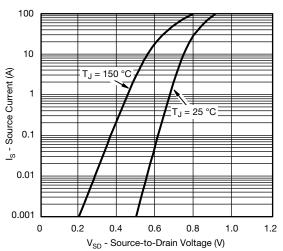
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



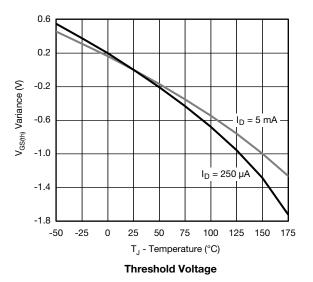
**On-Resistance vs. Junction Temperature** 

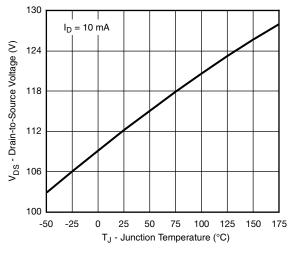


**On-Resistance vs. Gate-to-Source Voltage** 



Source Drain Diode Forward Voltage





Drain Source Breakdown vs. Junction Temperature 4

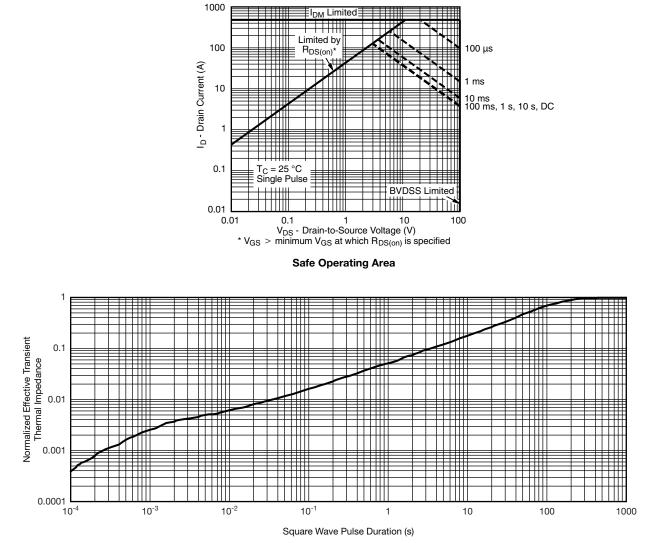
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### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

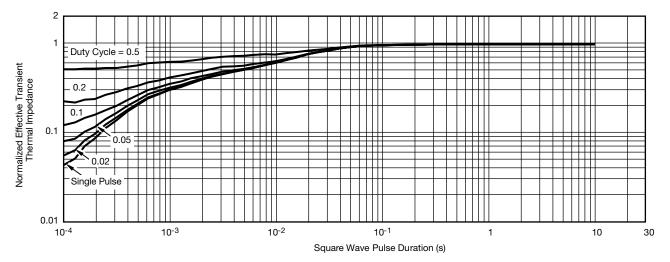


Normalized Thermal Transient Impedance, Junction-to-Ambient



## Vishay Siliconix

**THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

### Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction to Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction to Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?71515">www.vishay.com/ppg?71515</a>.



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REVISION HISTORY <sup>a</sup>					
REVISION	DATE	DESCRIPTION OF CHANGE			
С	04-Aug-15	Revised R <sub>g</sub> minimum limit			

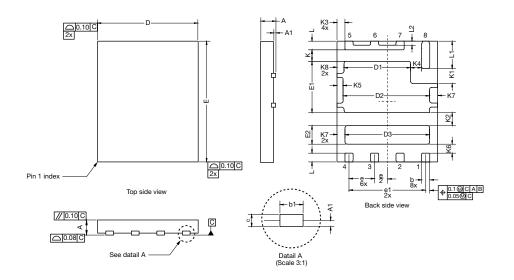
Note

a. As of April 2014



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PowerPAIR<sup>®</sup> 6 x 5 F Case Outline



DIMENSION	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.028	0.030	0.031	
A1	0.00	-	0.10	0.000	-	0.004	
b	0.35	0.41	0.46	0.014	0.016	0.018	
b1		0.38 ref.			0.015 ref.		
С	0.15	0.20	0.25	0.006	0.008	0.010	
D	4.90	5.00	5.10	0.193	0.197	0.201	
D1	3.26	3.31	3.36	0.128	0.130	0.132	
D2	4.20	4.30	4.40	0.165	0.169	0.173	
D3	4.15	4.20	4.25	0.163	0.165	0.167	
E	5.90	6.00	6.10	0.232	0.236	0.240	
E1	2.50	2.55	2.60	0.098	0.100	0.102	
E2	0.87	0.92	0.97	0.034	0.036	0.038	
е	1.27 BSC			0.050 BSC			
e1		3.81 BSC		0.150 BSC			
К	0.52	0.57	0.62	0.020	0.022	0.024	
K1	0.69	0.74	0.79	0.027	0.029	0.031	
K2	0.60	0.65	0.70	0.024	0.026	0.028	
K3	0.39 BSC			0.015 BSC			
K4	0.50	0.55	0.60	0.020	0.022	0.024	
K5	0.25	0.30	0.35	0.010	0.012	0.014	
K6	0.40	0.45	0.50	0.016	0.018	0.020	
K7	0.35	0.40	0.45	0.014	0.016	0.018	
K8	0.30	0.35	0.40	0.012	0.014	0.016	
L	0.33	0.43	0.53	0.013	0.017	0.021	
L1	1.31	1.36	1.41	0.052	0.054	0.056	
L2		0.20 ref.		0.008 ref.			

#### Note

• Millimeters will govern

Revision: 25-Feb-2020



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TO-263 (D<sup>2</sup>PAK): 3-LEAD









DETAIL A (ROTATED 90°)



		INC	HES	MILLIN	IETERS	
DIM.		MIN.	MAX.	MIN.	MAX.	
	А	0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
	D3	0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
E2		0.355	0.375	9.017	9.525	
E3		0.072	0.078	1.829	1.981	
	е	0.100	BSC	2.54 BSC		
	К	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
L2		L2 0.040		1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4		0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

### Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB.
  - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

Revison: 30-Sep-13



## **RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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