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U_FPGA-MGT
FPGA-MGT.SchDoc

U_PWR1
PWR1.SchDoc

U_Clock
Clock.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_PWR2
PWR2.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

A

A

B

B

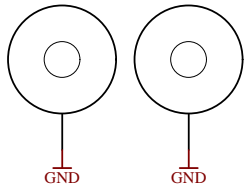
C

C

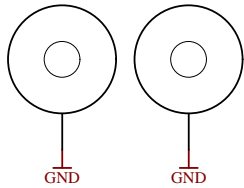
D

D

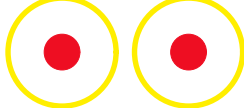
Mount.Hole 3.2mm Mount.Hole 3.2mm



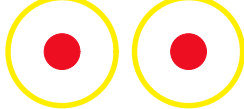
Mount.Hole 3.2mm Mount.Hole 3.2mm



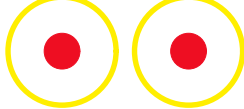
FIDU-DOT - small FIDU-DOT - small



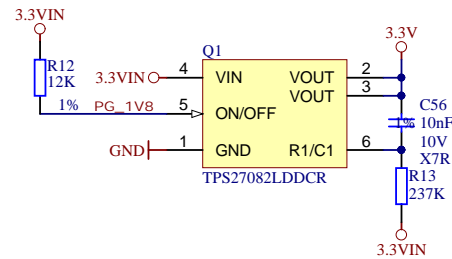
PM1 PM2
FIDU-DOT - small FIDU-DOT - small



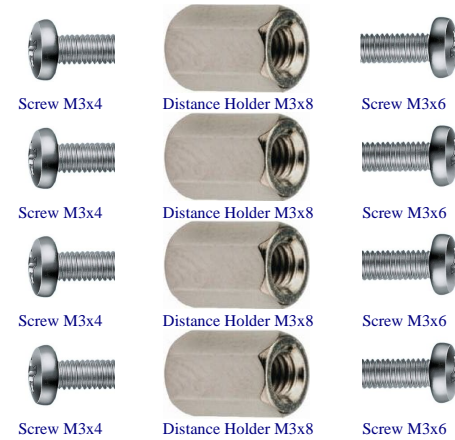
PM3 PM4
FIDU-DOT - small FIDU-DOT - small




PM5 PM6



Top of Board



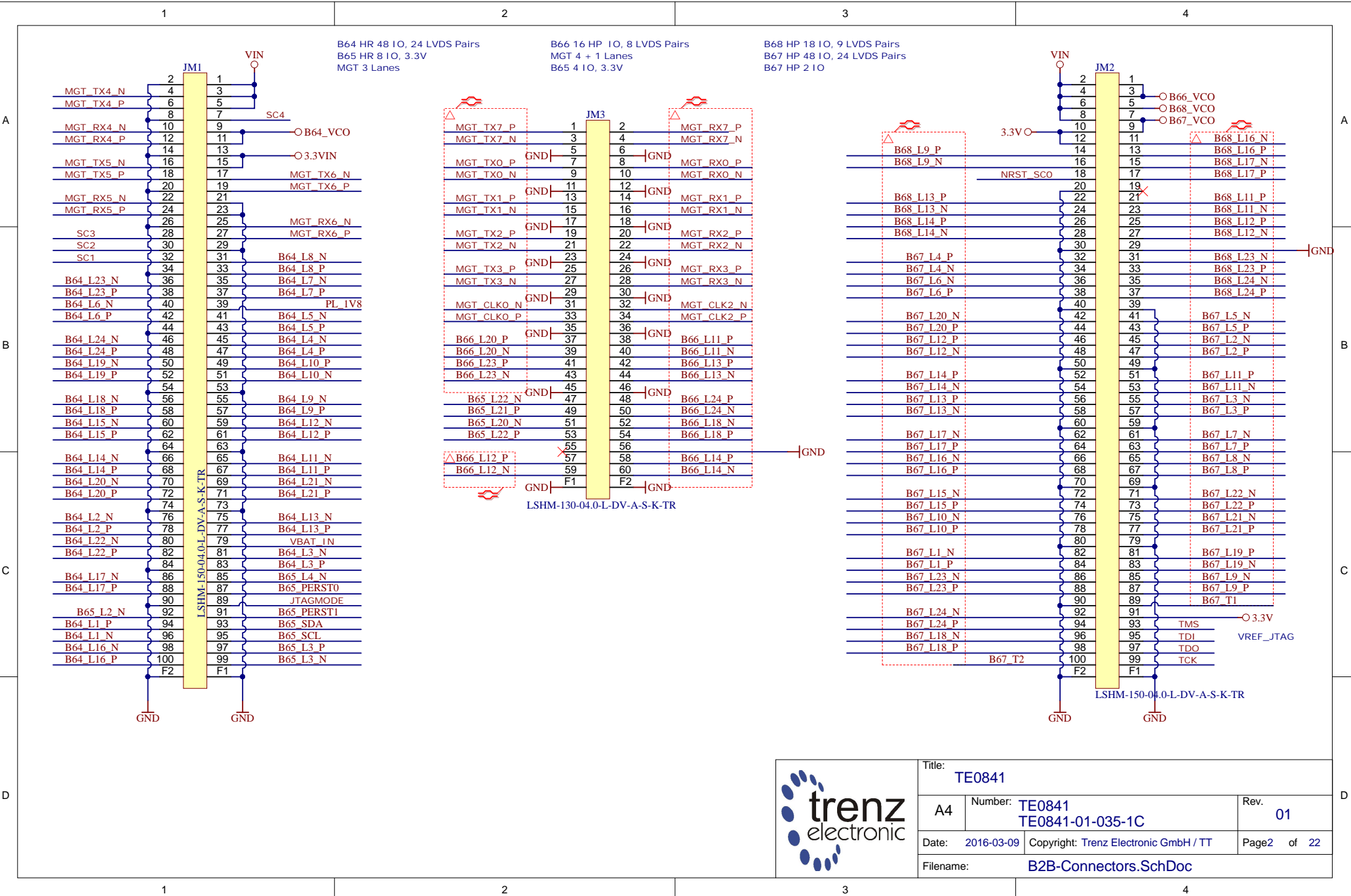
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		A4	Number: TE0841 TE0841-01-035-1C
Date: 2016-03-09		Copyright: Trenz Electronic GmbH / TT	
Filename: TE0841.SchDoc		Page1 of 22	

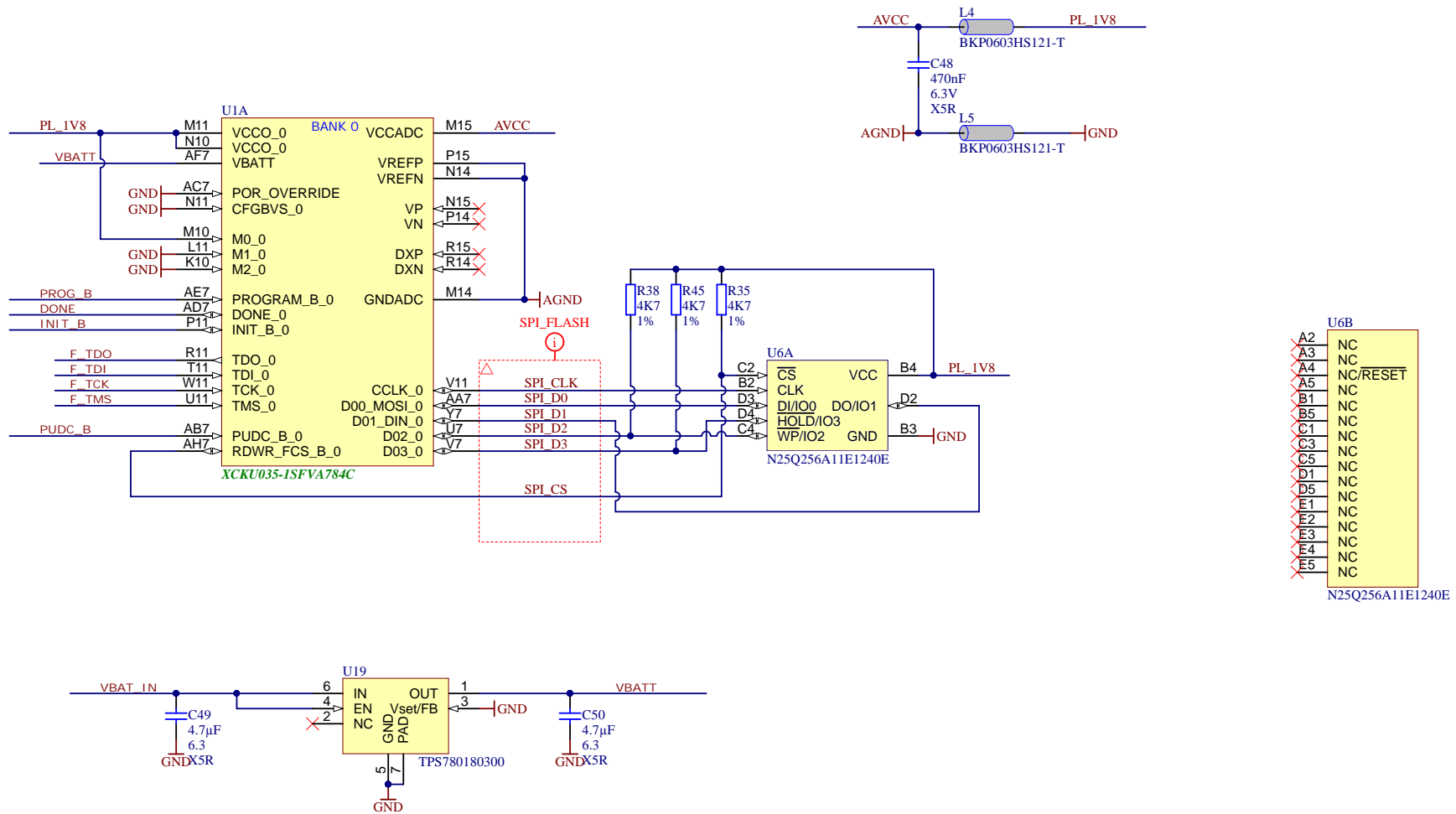
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		A4	Number: TE0841 TE0841-01-035-1C
Date: 2016-03-09		Copyright: Trenz Electronic GmbH / TT	
Filename: FPGA-MISC.SchDoc		Page3 of 22	

1 2 3 4

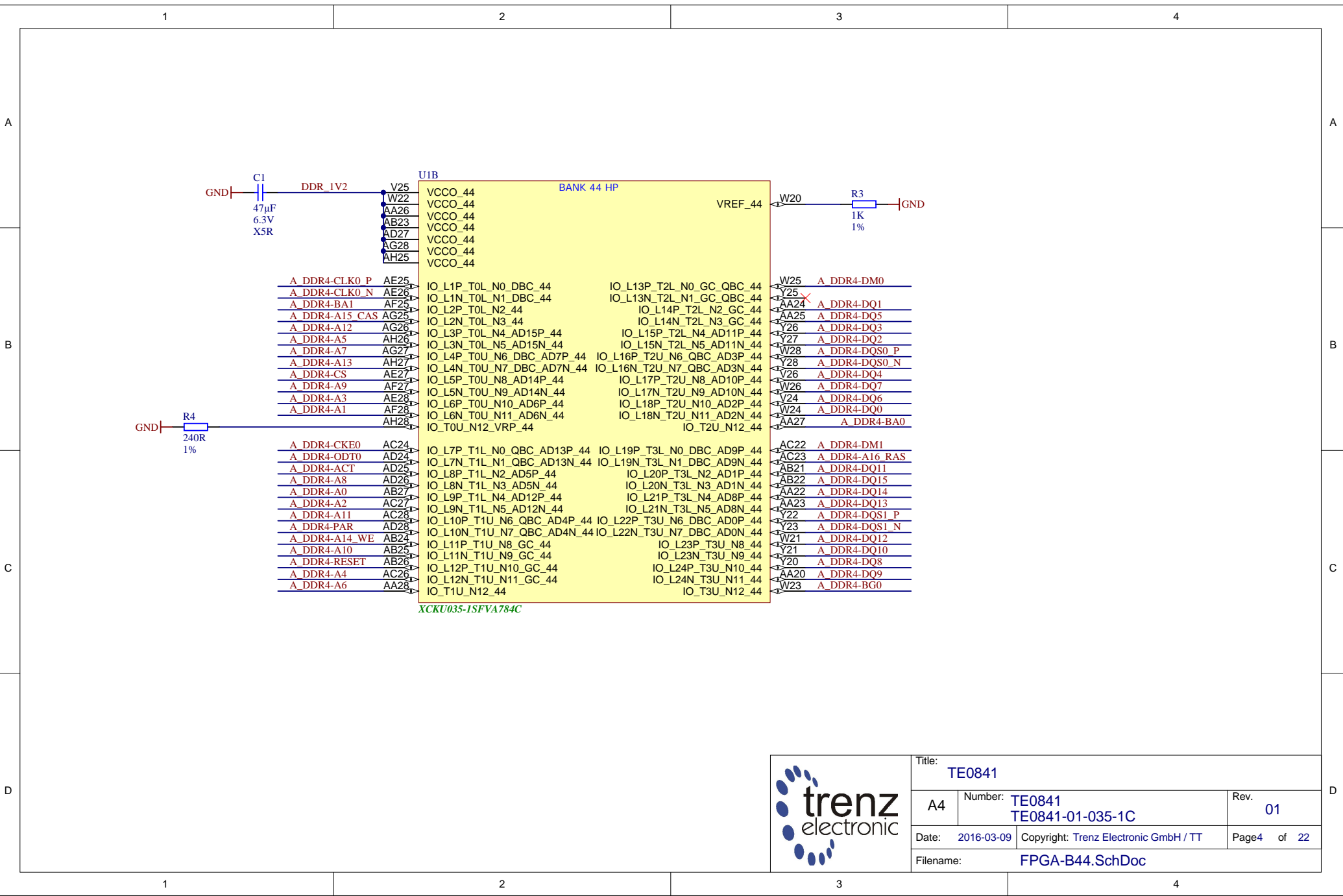
A

B

C

D

1 2 3 4



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page4 of 22
Filename: FPGA-B44.SchDoc		

1

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A

A

B

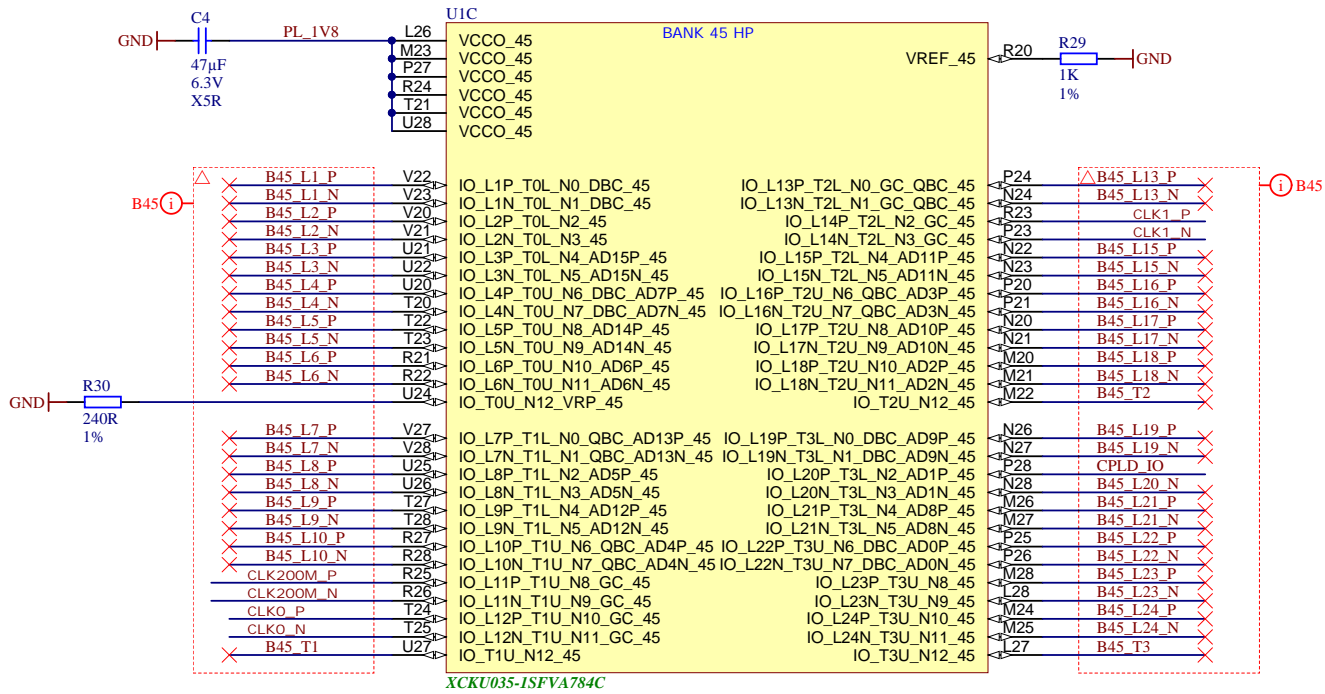
B

C

C

D

D



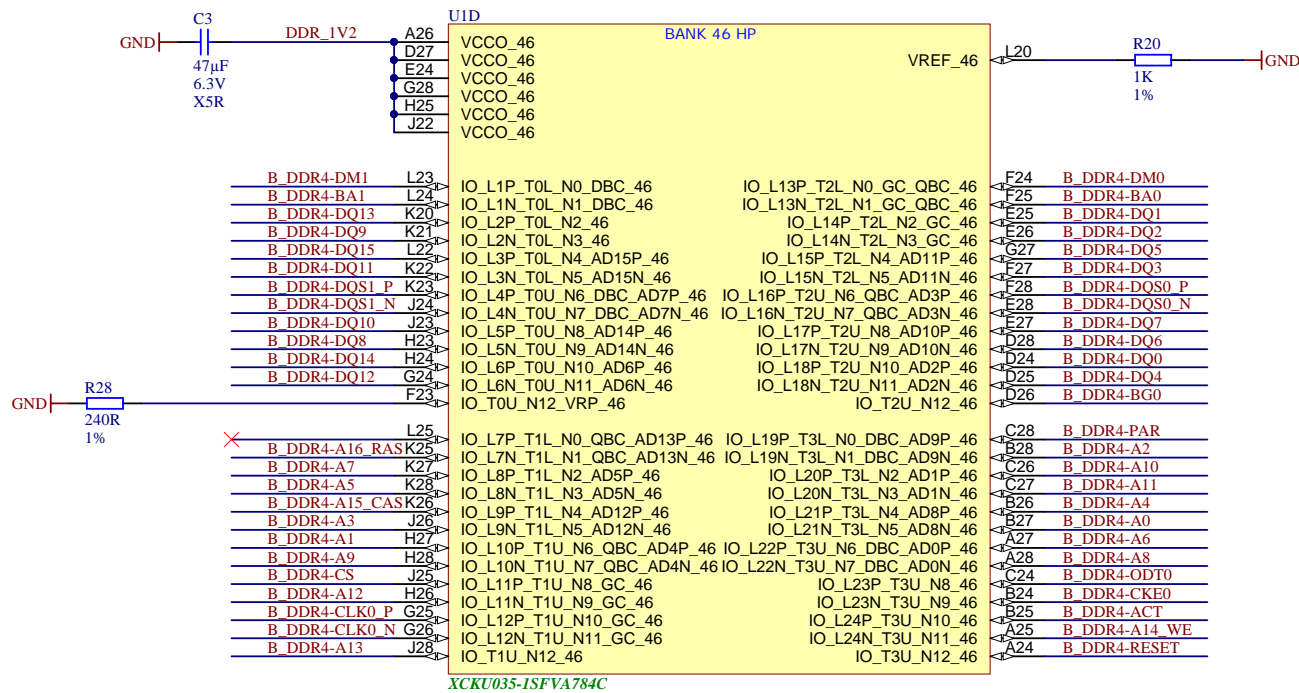
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Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page5 of 22
Filename: FPGA-B45.SchDoc		

1

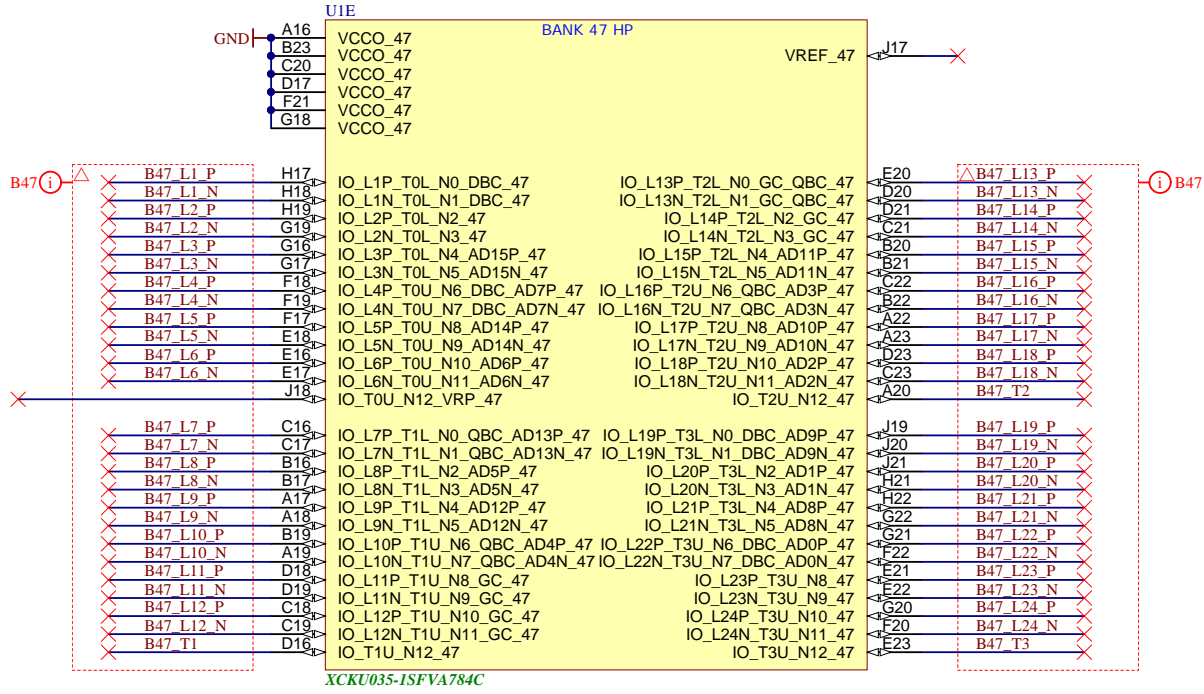
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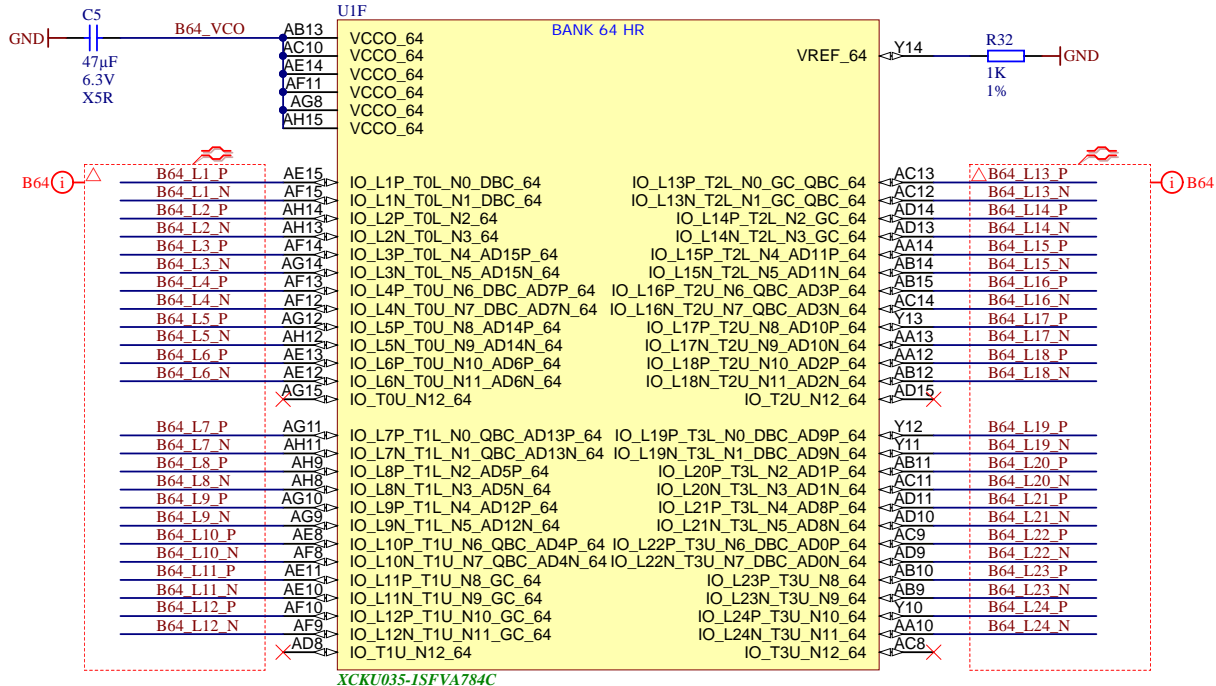
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Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page6 of 22
Filename: FPGA-B46.SchDoc		




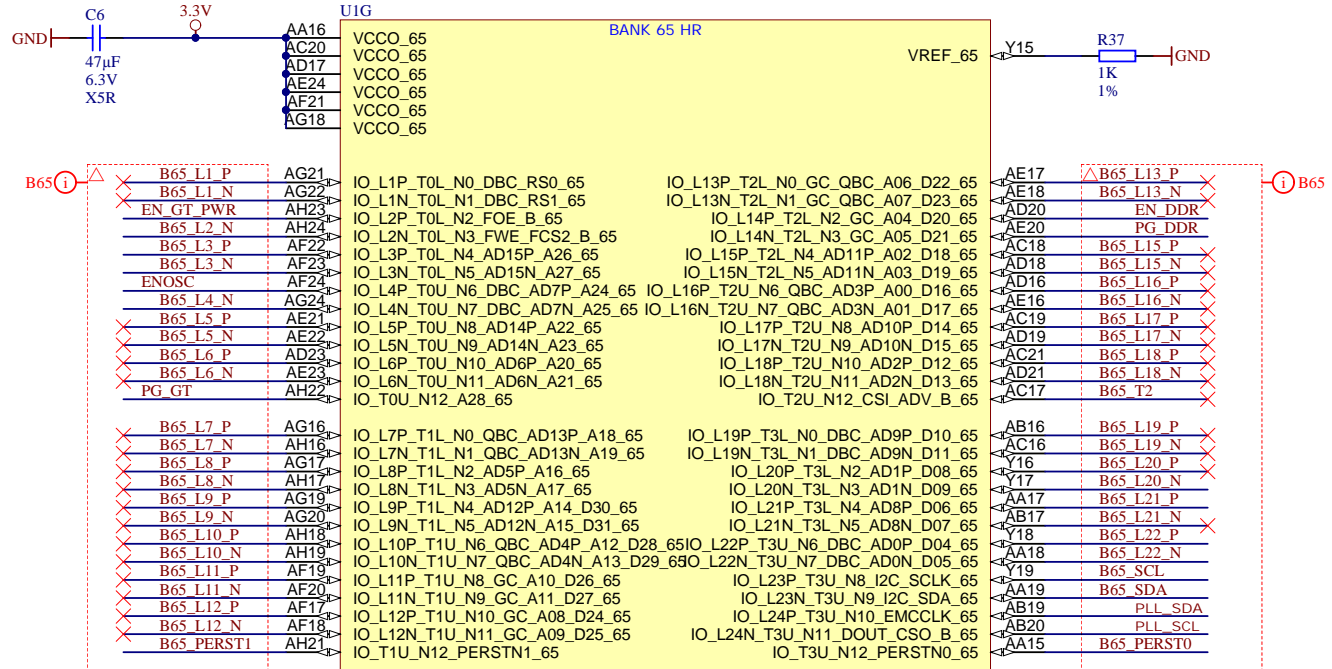
XCKU035-ISFVA784C



Title: TE0841		
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Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 7 of 22
Filename: FPGA-B47.SchDoc		



	Title: TE0841		
	A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page8 of 22
	Filename: FPGA-B64.SchDoc		



XCKU035-ISFVA784C



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page9 of 22
Filename: FPGA-B65.SchDoc		

A

A

B

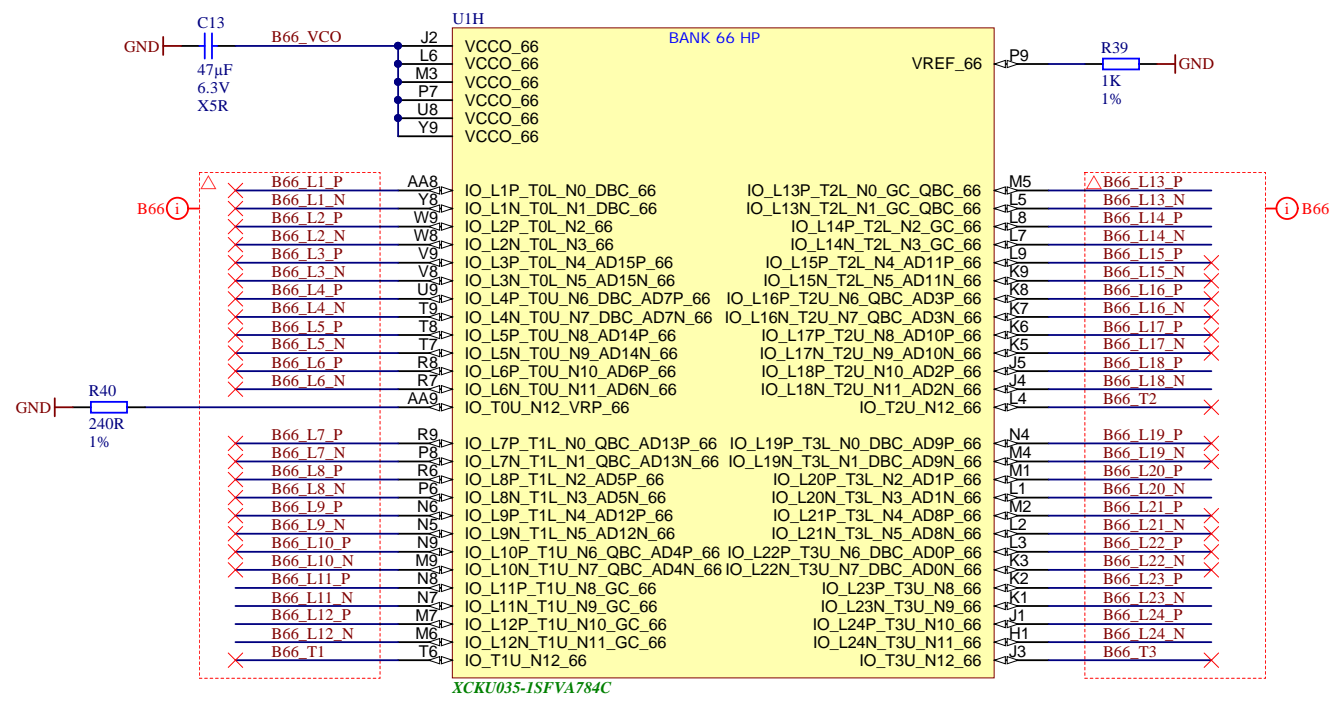
B

C

C

D

D



	Title: TE0841		
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	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 10 of 22
	Filename: FPGA-B66.SchDoc		

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A

A

B

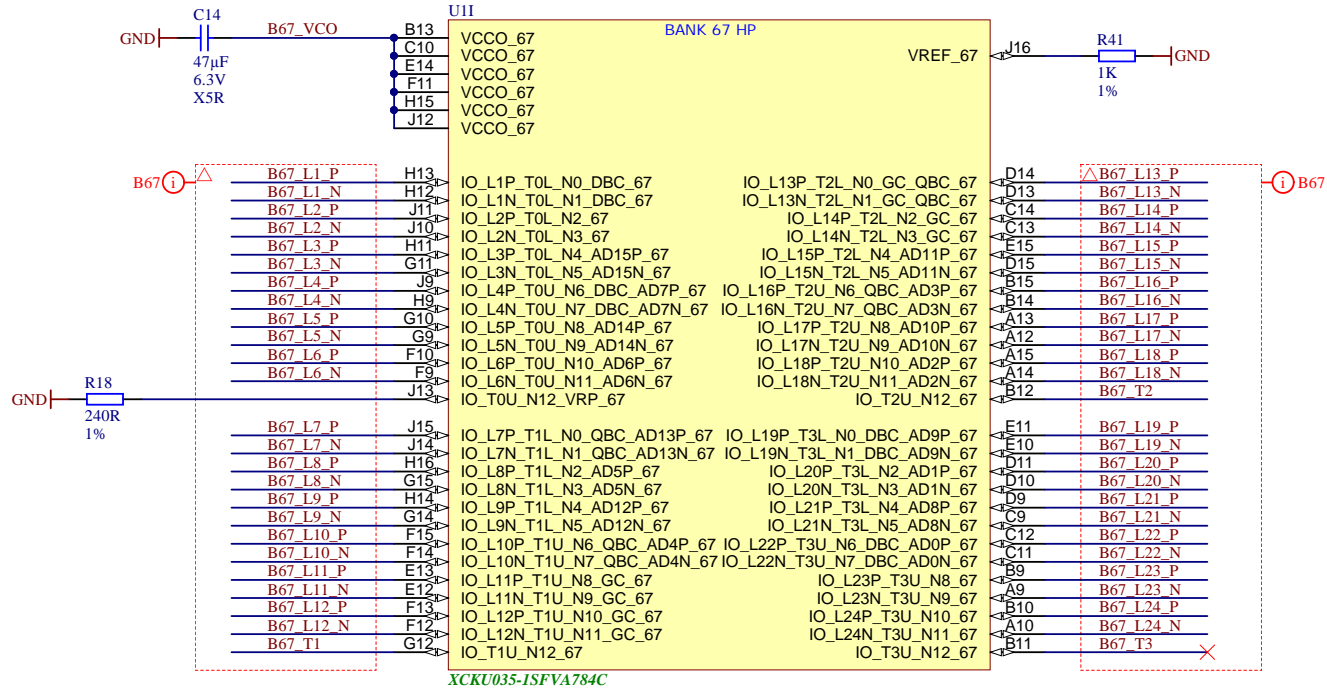
B

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C

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D



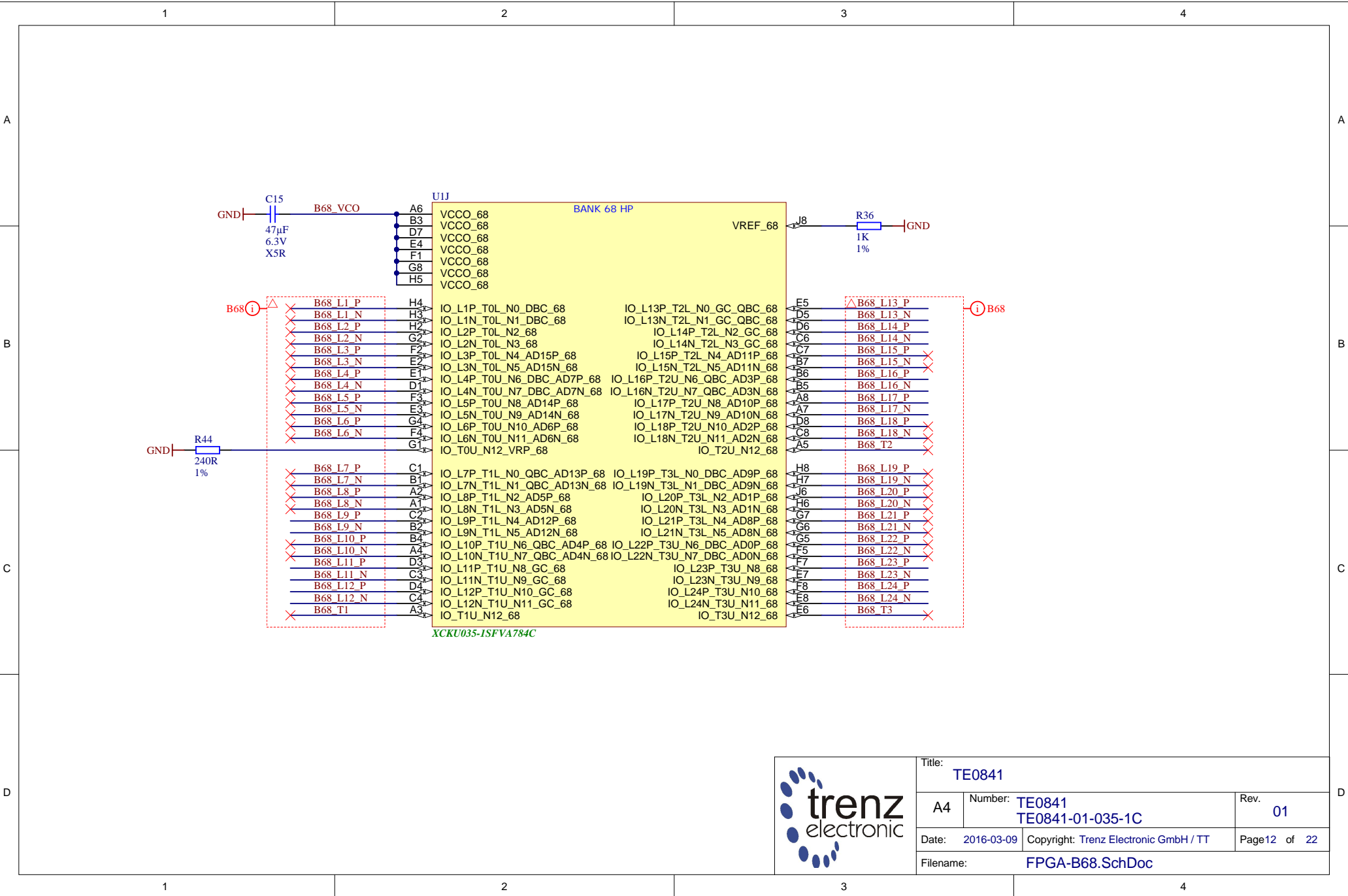
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Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 11 of 22
Filename: FPGA-B67.SchDoc		

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Title: TE0841		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 12 of 22
Filename: FPGA-B68.SchDoc		

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A

A

B

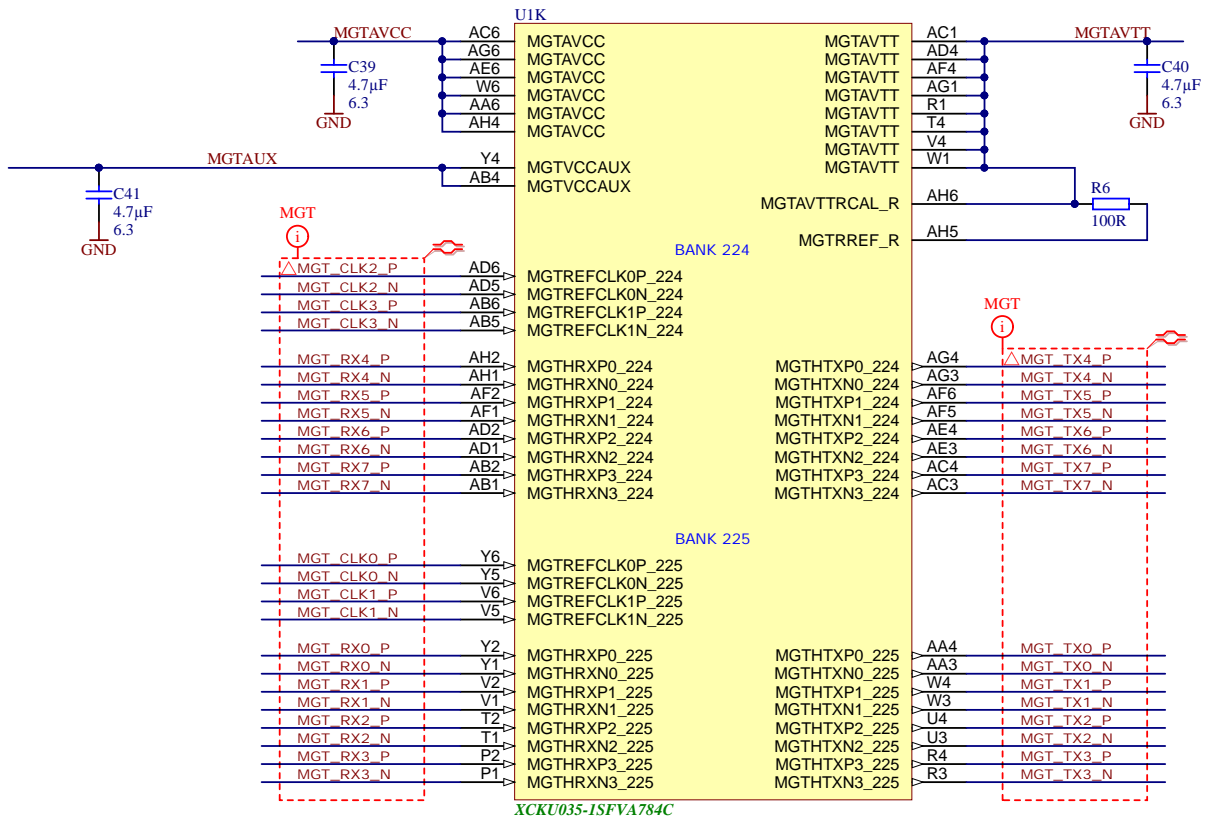
B

C

C

D

D



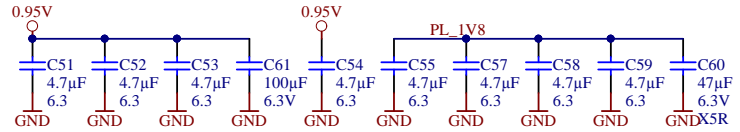
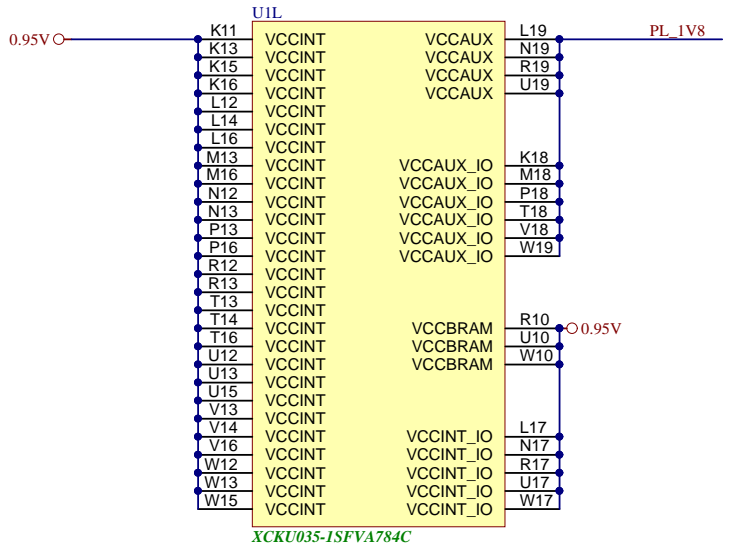
Title: TE0841		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page13 of 22
Filename: FPGA-MGT.SchDoc		


1

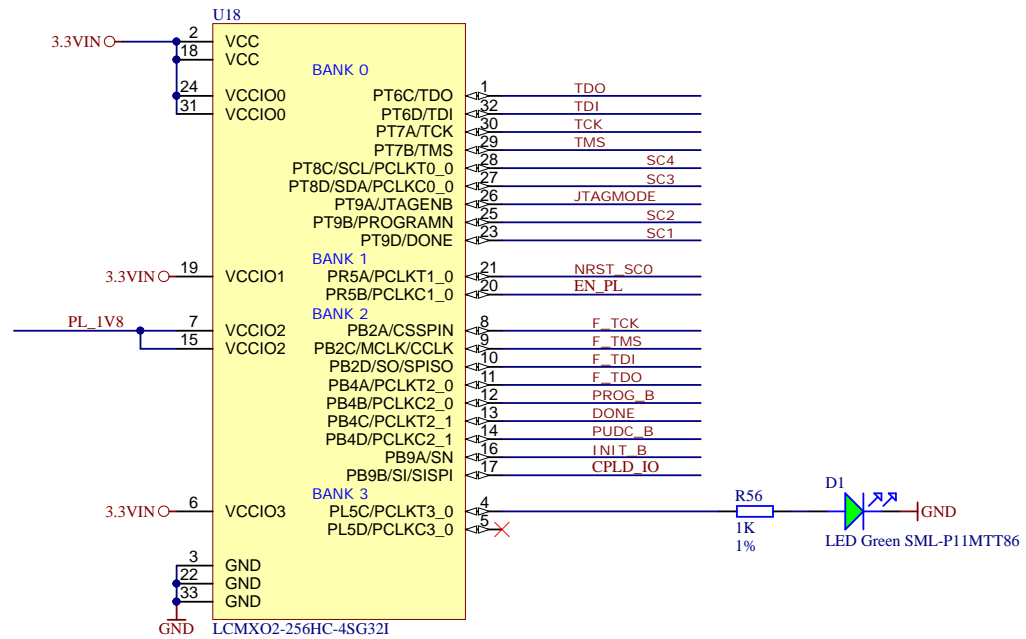
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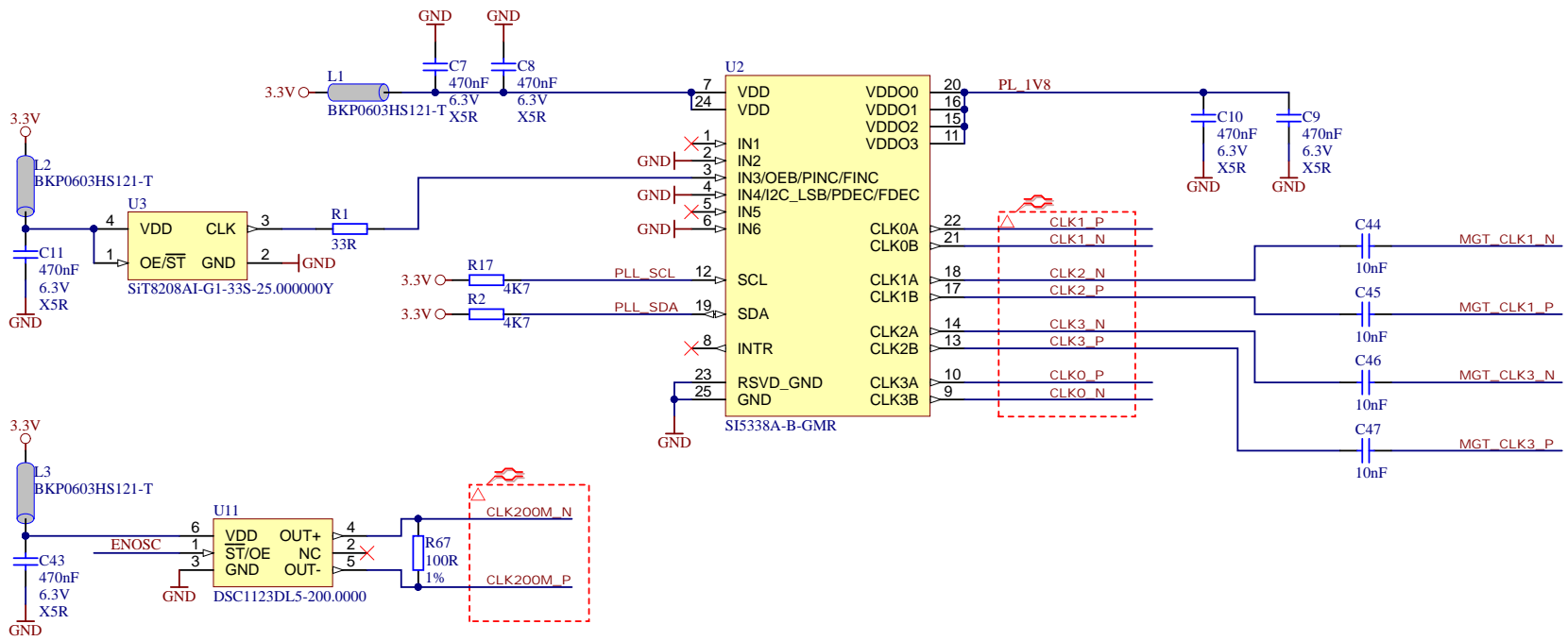
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	Title: TE0841		
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	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 14 of 22
	Filename: FPGA-PWR.SchDoc		



Title: TE0808		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 15 of 22
Filename: CPLD.SchDoc		



	Title: TE0841	
	A4	Number: TE0841 TE0841-01-035-1C
	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT
	Filename: Clock.SchDoc	Rev. 01 Page 16 of 22

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A

A

B

B

C

C

D

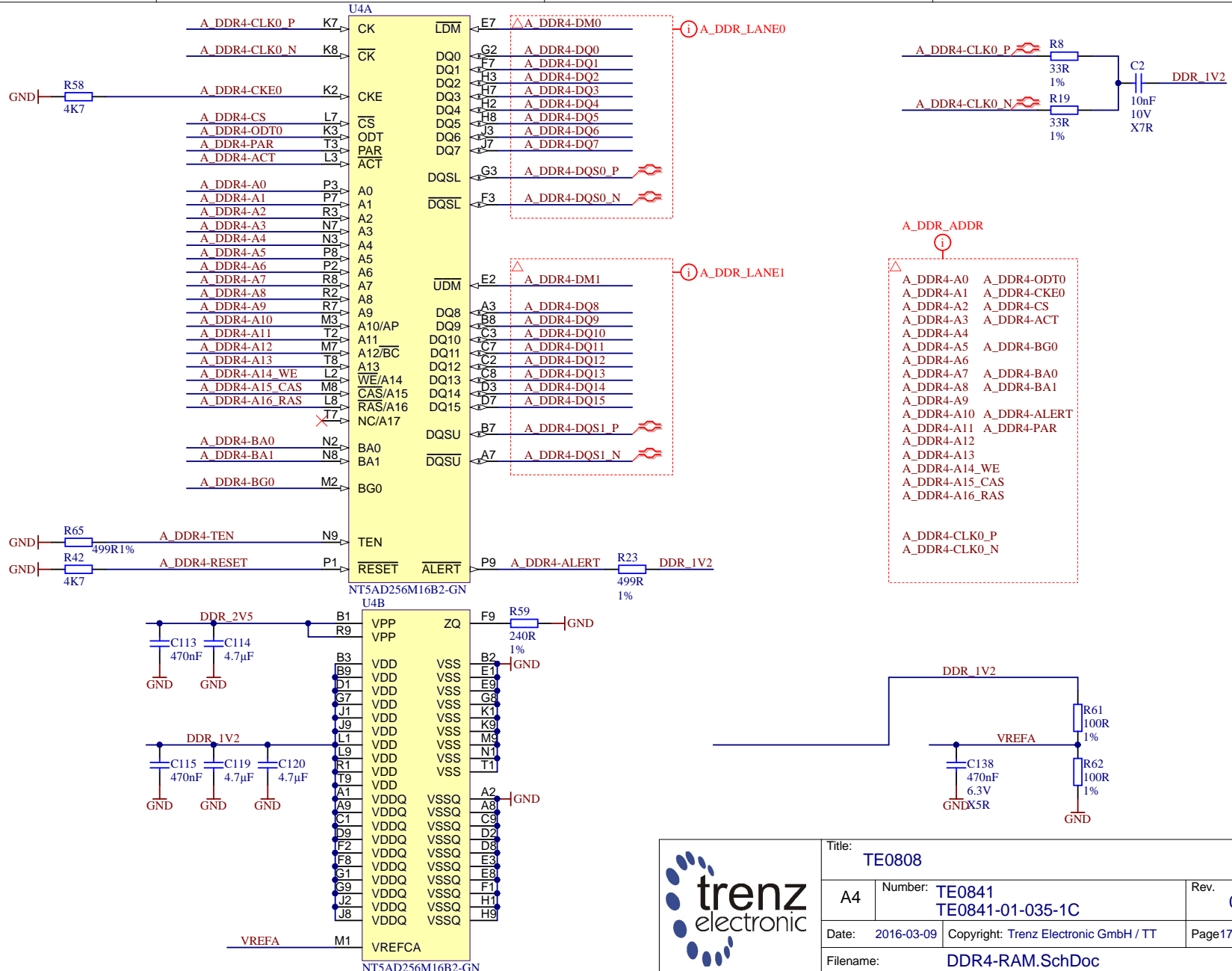
D

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A_DDR_ADDR

A_DDR4-A0	A_DDR4-ODT0
A_DDR4-A1	A_DDR4-CKE0
A_DDR4-A2	A_DDR4-CS
A_DDR4-A3	A_DDR4-ACT
A_DDR4-A4	
A_DDR4-A5	A_DDR4-BG0
A_DDR4-A6	
A_DDR4-A7	A_DDR4-BA0
A_DDR4-A8	A_DDR4-BA1
A_DDR4-A9	
A_DDR4-A10	A_DDR4-ALERT
A_DDR4-A11	A_DDR4-PAR
A_DDR4-A12	
A_DDR4-A14_WE	
A_DDR4-A15_CAS	
A_DDR4-A16_RAS	

A_DDR4-CLK0_P
A_DDR4-CLK0_N

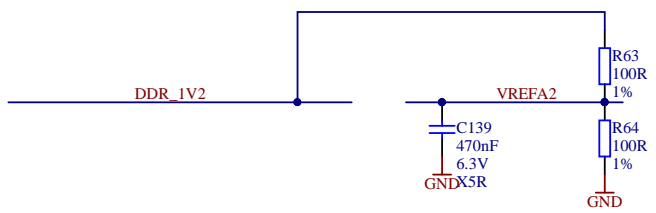
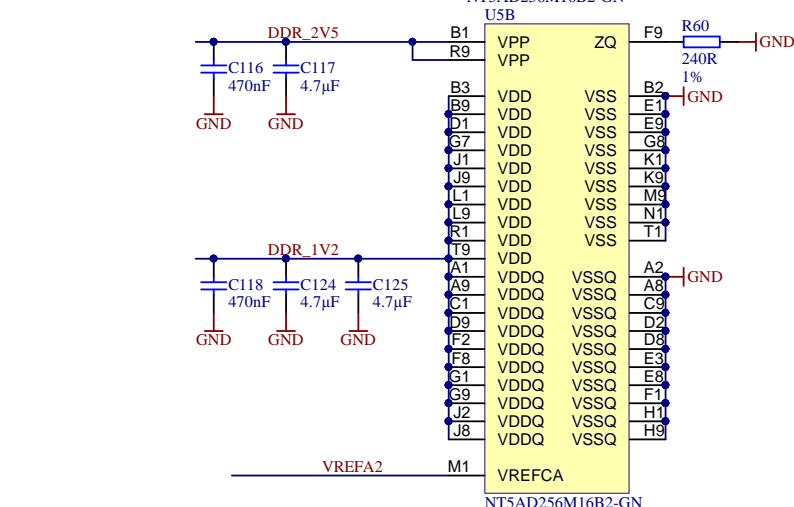
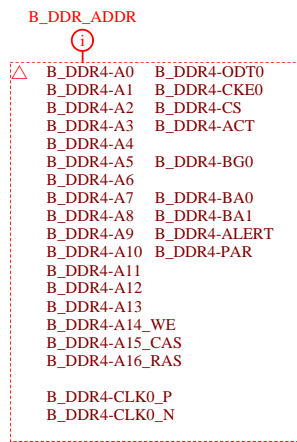
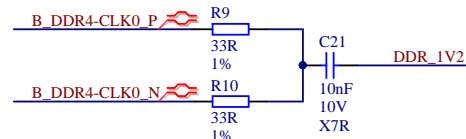
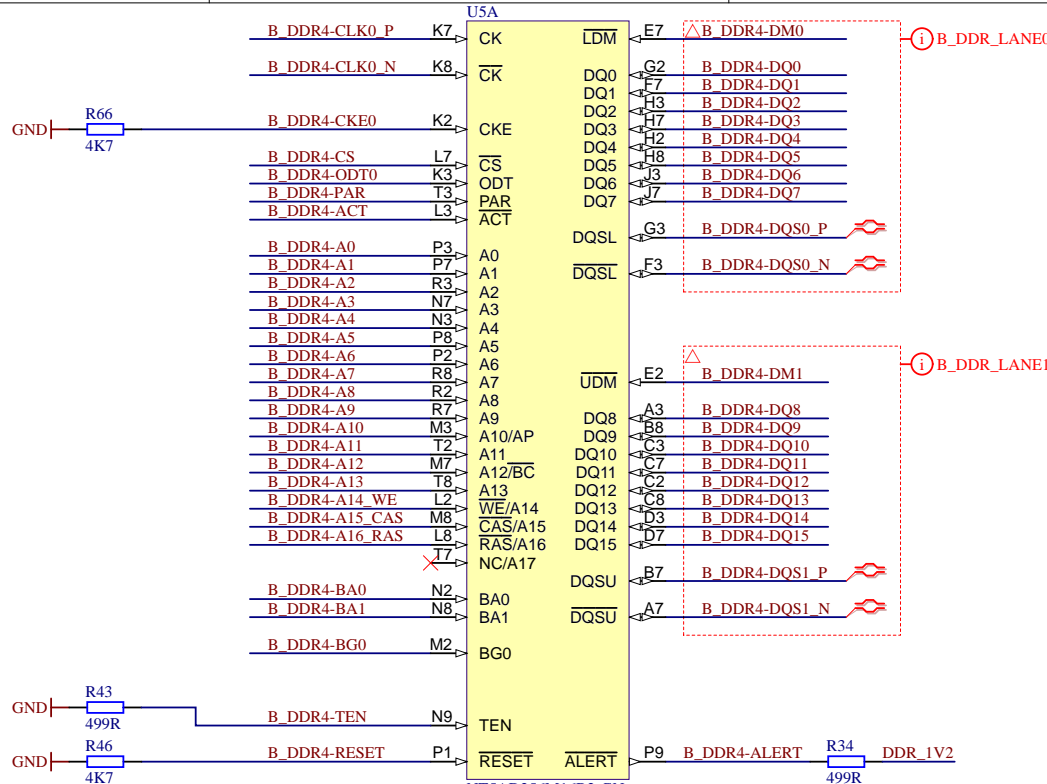
Title: TE0808		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 17 of 22
Filename: DDR4-RAM.SchDoc		

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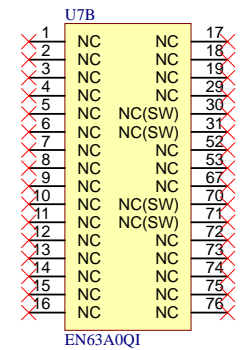
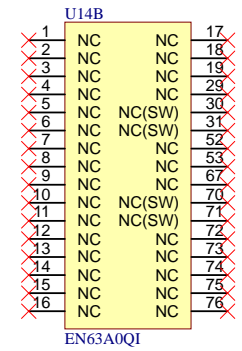
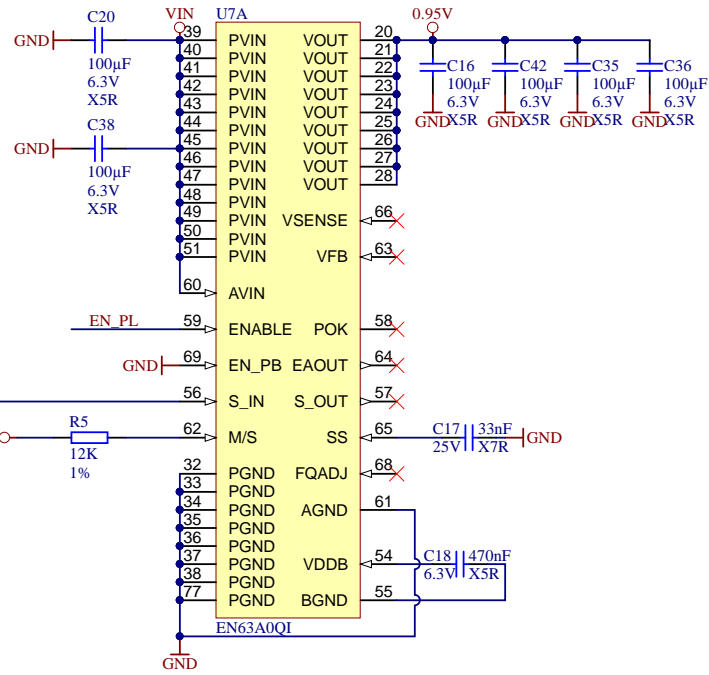
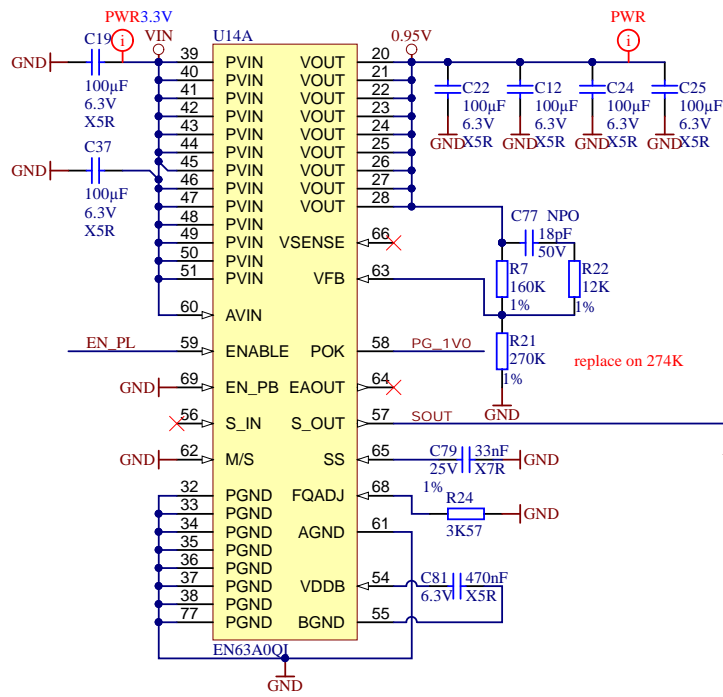
Title: TE0808		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 18 of 22
Filename: DDR4-RAM_2.SchDoc		

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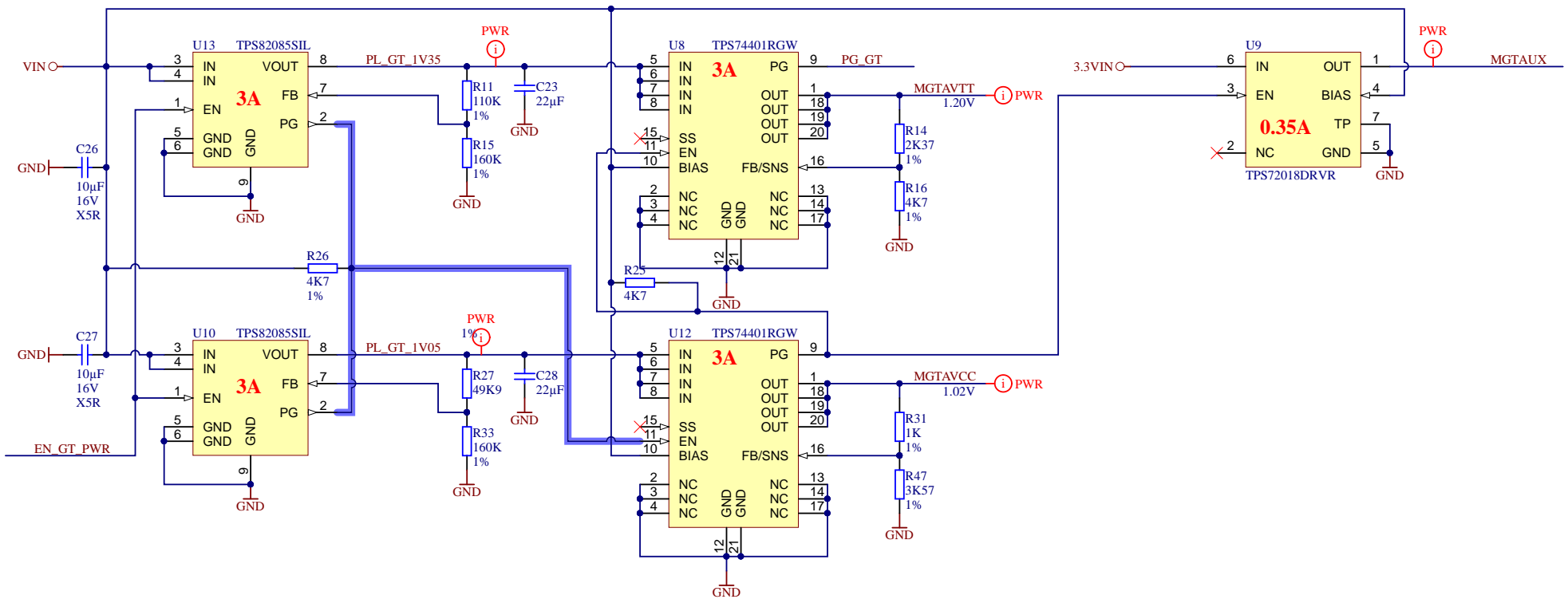
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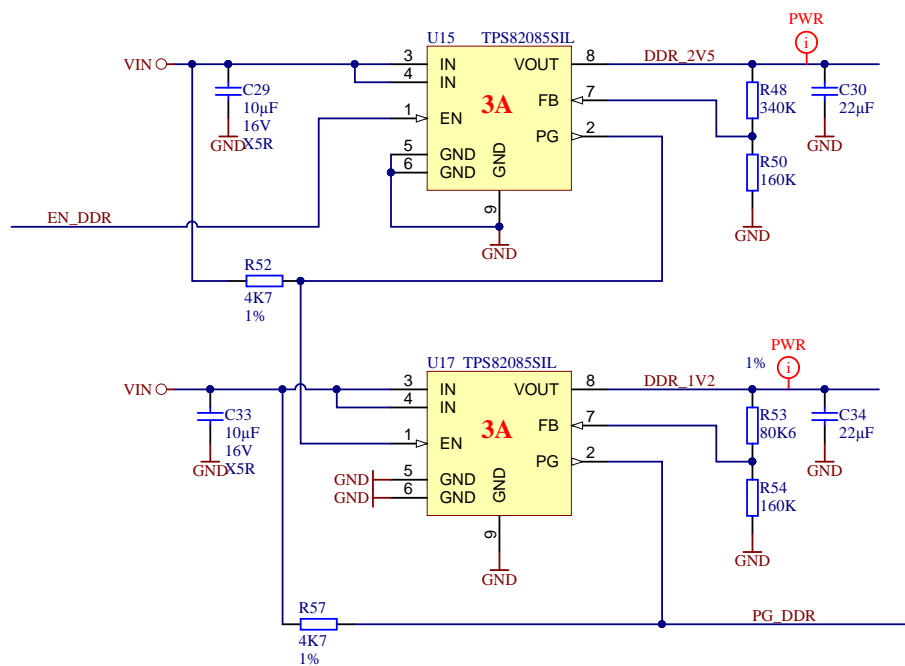
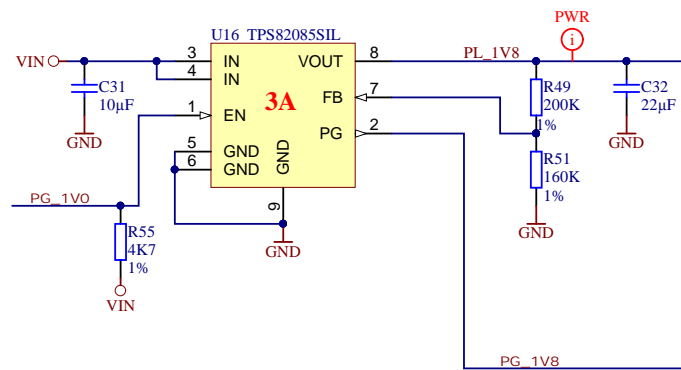
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Title: TE0841		
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Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 19 of 22
Filename: PWR1.SchDoc		



		Title: TE0841	
		A4	Number: TE0841 TE0841-01-035-1C
Date: 2016-03-09		Copyright: Trenz Electronic GmbH / TT	
Filename: PWR2.SchDoc		Page20 of 22	



Title: TE0808		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page21 of 22
Filename: POWER_2.SchDoc		

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CHANGES REV01 TO REV01A (08.16.2017):

1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:
 -- AE13 (IO_L6P_T0U_N10_AD6P_64)/AE12 (IO_L6N_T0U_N11_AD6N_64)
 -- J5 (IO_L18P_T2U_N10_AD2P_66)/J4 (IO_L18N_T2U_N11_AD2N_66)

2) Net names changed (no electrical changes):

JM1: swapped signals B64_L6:
 -- B64_L6_N - pin 40 (was pin 42)
 -- B64_L6_P - pin 42 (was pin 40)
 JM3: swapped signals B64_L6:
 -- B66_L18_N - pin 52 (was pin 54)
 -- B66_L18_P - pin 54 (was pin 52)

A

A

B

B

C

C

D

D

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Title: TE0808 - Changes list		
A4	Number: TE0841 TE0841-01-035-1C	Rev. 01
Date: 2017-08-16	Copyright: Trenz Electronic GmbH	Page 22 of 22
Filename: Revision_Changes.SchDoc		