AK4462
Application Note

1. General Description

This Application Note is intended to assist in designing systems using the AK4462.

2. Table of Contents

3. Block Diagram

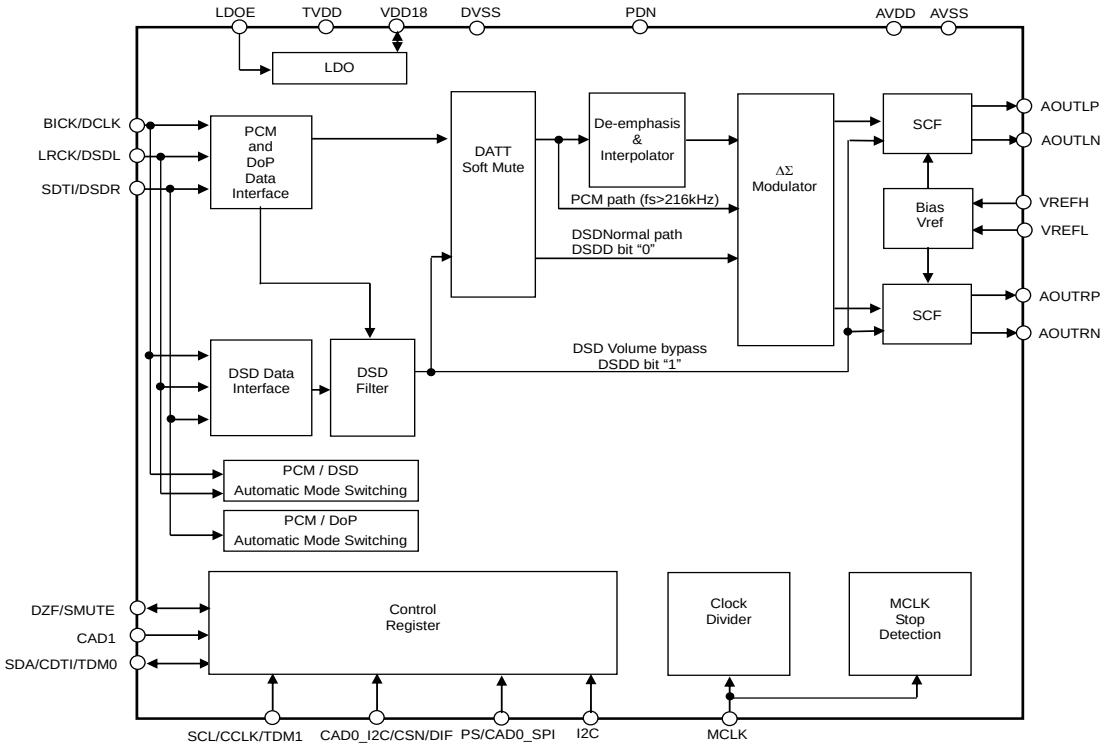

Figure 1. AK4462 Block Diagram

4. Comparison Table of D/A Converters

4.1. Premium DACs Comparison Table

Table 1 shows a comparison table of Premium DACs featuring AKM's LSI manufacturing process for premium audio.

Table 1. AKM Premium DAC Comparison Table (Y: Available, N/A: Not Available)

	AK4499	AK4497	AK4493	**AK4462**	AK4468
AVDD	4.75–5.25 V	1.7–3.6 V	1.7–3.6 V	3.0–5.5 V	3.0–5.5 V
VDDL/R	4.75–5.25 V	4.75–5.25 V	4.75–5.25 V	-	-
TVDD	1.7–3.6 V	1.7–3.6 V	1.7–3.6 V	1.7–3.6 V	1.7–3.6 V
Channels	4	2	2	2	8
Output type	Balanced	Balanced	Balanced	Balanced	Balanced
PCM sampling rate	8–768 kHz	8–768 kHz	8–768 kHz	8–768 kHz	8–768 kHz
DSD sampling rate (max.)	DSD512	DSD512	DSD512	DSD512	DSD512
DoP sampling rate (max.)	N/A	N/A	N/A	DoP256	N/A
S/N	134 dB	128 dB	123 dB	117 dB	117 dB
THD+N	−124 dB	−116 dB	−113 dB	−107 dB	−107 dB
Digital Filter (PCM mode)	6 types	6 types	6 types	6 types	6 types
External Filter Mode	Y	Y	Y	N/A	N/A
TDM	Y	Y	Y	Y	Y
Daisy Chain	Y	Y	N/A	N/A	Y
Automatic Switching (PCM/DSD mode)	Y	N/A	Y	Y	Y
Automatic Switching (PCM/DoP mode)	N/A	N/A	N/A	Y	N/A
Power Consumption	667 mW	343 mW	188 mW	70 mW	245 mW
Package	128-pin HTQFP	64-pin HTQFP	48-pin LQFP	24-pin QFN	48-pin QFN

4.2. Mid-Range Stereo DACs Comparison Table

The comparison table of Mid-Range Stereo DAC Series is shown in Table 2.

Table 2. Function and Characteristics Comparison Table of AK4432, AK4452 and AK4462
(Y: Available, N/A: Not available)

	AK4432	AK4452	**AK4462**
LSI Process for Premium Audio	N/A	N/A	Y
AVDD	3.0–3.6 V	3.0–5.5 V	3.0–5.5 V
TVDD	3.0–3.6 V	1.7–3.6 V	1.7–3.6 V
Power Consumption	26 mW	50 mW	70 mW
Output type	Single-Ended	Balanced	Balanced
PCM sampling rate	8–192 kHz	8–768 kHz	8–768 kHz
DSD sampling rate (max.)	N/A	DSD256	DSD512
DoP sampling rate (max.)	N/A	N/A	DoP256
S/N	108 dB	115 dB	117 dB
THD+N	−91 dB	−107 dB	−107 dB
Digital Filter (PCM mode)	5 types	5 types	6 types
De-emphasis Filter	N/A	Y	Y
TDM	Y	Y	Y
Daisy Chain	N/A	Y	N/A
Clock Synchronization Function	Y	Y	Y
Automatic Mode Switching (PCM/DSD mode)	N/A	N/A	Y
Automatic Mode Switching (PCM/DoP mode)	N/A	N/A	Y
Package	16-pin TSSOP	32-pin QFN	24-pin QFN
Pin/Register control select	Y	Y	Y

4.3. AK4462 Register Map (Compared with AK4452)

Register maps of the AK4462 and the AK4452 are shown in Table 3 and Table 4.
※yellow: Added in the AK4462 blue: Removed in the AK4462

Table 3. AK4462 Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF[2]	DIF[1]	DIF[0]	RSTN
01H	Control 2	0	0	SD	DFS[1]	DFS[0]	DEM[1]	DEM[0]	SMUTE
02H	Control 3	DP	ADP	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	Lch ATT	ATTL[7]	ATTL[6]	ATTL[5]	ATTL[4]	ATTL[3]	ATTL[2]	ATTL[1]	ATTL[0]
04H	Rch ATT	ATTR[7]	ATTR[6]	ATTR[5]	ATTR[4]	ATTR[3]	ATTR[2]	ATTR[1]	ATTR[0]
05H	Control 4	INVL	INVR	0	0	0	0	DFS[2]	SSLOW
06H	DSD1	DDM	DML	DMR	DDMOE	0	DDMT	DSDD	DSDSEL[0]
07H	Control 5	L	R	0	0	0	0	1	SYNCE
08H	Control 6	0	0	0	0	0	0	0	0
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL[1]
0AH	Control 7	TDM[1]	TDM[0]	SDS[1]	SDS[2]	1	PW	0	1
0BH	Control 8	ATS[1]	ATS[0]	0	SDS[0]	1	1	0	0
0CH	READONLY1	0	0	0	0	0	0	0	0
0DH	READONLY2	0	0	0	0	0	0	0	0
0EH	READONLY3	0	1	0	1	0	0	0	0
0FH	READONLY4	1	1	1	1	1	1	1	1
10H	READONLY5	1	1	1	1	1	1	1	1
11H	READONLY6	1	1	1	1	1	1	1	1
12H	READONLY7	1	1	1	1	1	1	1	1
13H	READONLY8	1	1	1	1	1	1	1	1
14H	READONLY9	1	1	1	1	1	1	1	1
15H	Control 12	ADPE	ADPT[1]	ADPT[0]	0	0	0	0	0
16H	DoP1	DOP	DMMI	ADOP	ADOPE	0	0	0	0
17H	DoP2	DOPSEL[1]	DOPSEL[0]	0	0	0	0	0	0
18H	DSDMARKERE	DMIE[7]	DMIE[6]	DMIE[5]	DMIE[4]	DMIE[3]	DMIE[2]	DMIE[1]	DMIE[0]
19H	DSDMARKERO	DMIO[7]	DMIO[6]	DMIO[5]	DMIO[4]	DMIO[3]	DMIO[2]	DMIO[1]	DMIO[0]

Table 4. AK4452 Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	0	DIF[2]	DIF[1]	DIF[0]	RSTN
01H	Control 2	0	0	SD	DFS[1]	DFS[0]	DEM1[1]	DEM1[0]	SMUTE
02H	Control 3	DP	0	DCKS	DCKB	MONO	DZFB	SELLR	SLOW
03H	L1ch ATT	ATTL[7]	ATTL[6]	ATTL[5]	ATTL[4]	ATTL[3]	ATTL[2]	ATTL[1]	ATTL[0]
04H	R1ch ATT	ATTR[7]	ATTR[6]	ATTR[5]	ATTR[4]	ATTR[3]	ATTR[2]	ATTR[1]	ATTR[0]
05H	Control 4	INVL1	INVR1	0	0	0	0	DFS[2]	SSLOW
06H	DSD1	DDM	DML1	DMR1	DMC	DMRE	0	DSDD	DSDSEL[0]
07H	Control 5	0	0	0	0	0	0	1	SYNCE
08H	Sound Control	L1	R1	0	0	0	0	SC[1]	SC[0]
09H	DSD2	0	0	0	0	0	0	DSDF	DSDSEL[1]
0AH	Control 6	TDM[1]	TDM[0]	SDS[1]	SDS[2]	1	PW1	0	1
0BH	Control 7	ATS[1]	ATS[0]	0	SDS[0]	1	1	DCHAIN	0
0CH	Control 8	0	0	0	0	0	FIR[2]	FIR[1]	FIR[0]
0DH	Reserved	0	0	0	0	0	0	0	0
0EH	Reserved	0	1	0	1	0	0	0	0
0FH	Reserved	1	1	1	1	1	1	1	1
10H	Reserved	1	1	1	1	1	1	1	1

■The functions added in the AK4462

・02H D6: ADP
Readback register for internal PCM/DSD operation mode. This bit is valid when ADPE bit = “1”.

・06H D4: DDMOE
Output Flag selection from the DZF pin

・06H D2: DDMT
DSD Signal Full-scale Detection Time setting

・15H D7: ADPE
PCM/DSD Automatic Mode Switching function enable bit

・15H D[6:5]: ADPT[1:0]
Time until PCM/DSD mode detection when input data becomes zero

・16H D4: ADOPE
PCM/DoP Automatic Mode Switching function enable bit

・16H D5: ADOP
Readback register for internal PCM/DoP operation mode. This bit is valid when ADOPE bit = “1”.

・16H D6: DMMI
DoP Data Detection Code setting

・16H D7: DOP
DoP Mode enable

・17H D[7:6]: DOPSEL[1:0]
DoP Sampling Speed setting

・18H D[7:0]: DMIE[7:0]
EVEN Marker setting (Valid only when DMMI bit = “1”)

・19H D[7:0]: DMIO[7:0]
ODD Marker setting (Valid only when DMMI bit = “1”)

5. AK4462 Function List

Table 5 shows the functions available in PCM/DSD/DoP modes. For details on how to use each function, refer to the corresponding sections of the AK4462 datasheet in Datasheet Section column. In Pin Control mode, only a few functions are available. Refer to the section 9.1 in the datasheet for the functions available in Pin Control mode.

Table 5. Function List of PCM/DSD/DoP mode @Register Control Mode
(Y: Available, N/A: Not available)

Function	Addr	Bit	PCM	DSD		DoP		Data-sheet Section
				Normal	Volume Bypass	Normal	Volume Bypass	
PCM/DSD/DoP Mode Selection	02H 16H	DP DOP	Y	Y	Y	Y	Y	9.2
System Clock Setting @PCM mode	00, 01, 05H	ACKS DFS[2:0]	Y	N/A	N/A	Y	Y	9.3.1
System Clock Setting @DSD mode	02H	DCKS DSDSEL[1:0]	N/A	Y	Y	N/A	N/A	9.3.2
System Clock Setting @DoP mode	00, 02, 17H	DCKS, ACKS DOPSEL[1:0]	N/A	N/A	N/A	Y	Y	9.3.3
Digital Filter Selection @PCM mode	01,02, 05H	SD, SLOW SSLOW	Y (Note 1)	N/A	N/A	N/A	N/A	9.5.1
Digital Filter Selection @DSD mode, DoP mode	09H	DSDF	N/A	Y	N/A	Y	N/A	9.5.2
De-emphasis Filter	01H	DEM[1:0]	Y (Note 2)	N/A	N/A	N/A	N/A	9.6
Path Selection @ DSD mode	06H	DSDD	N/A	Y	Y	Y	Y	9.2.3
Audio Data Interface Format @ PCM mode, DoP mode	00H	DIF[2:0]	Y	N/A	N/A	Y	Y	9.4.1 9.4.3
TDM Interface Format	0AH	TDM[1:0]	Y	N/A	N/A	N/A	N/A	9.4.1
Attenuation Level	03, 04H	ATTL/R[7:0]	Y	Y	N/A	Y	N/A	9.7
Data Zero Detection Enable	08H	L, R	Y	Y	N/A	Y	N/A	9.8.1
Mono/Stereo Mode Selection	02H	MONO	Y	Y	Y	Y	Y	9.9
Data Invert Mode Selection	05H	INVL, INVR	Y	Y	Y	Y	Y	9.9
Data Selection of L Channel and R Channel	02H	SELLR	Y	Y	Y	Y	Y	9.9
DSD Mute Function @ Full Scale Detected	06H	DDM	N/A	Y	Y	Y	Y	9.8.2
Soft Mute	01H	SMUTE	Y	Y	Y	Y	Y	9.12
RSTN	00H	RSTN	Y	Y	Y	Y	Y	9.15.3
Clock Synchronization Function	07H	SYNCE	Y	N/A	N/A	Y	Y	9.16
Automatic Mode Switching (PCM/DSD mode)	15H	ADPE	Y	Y	Y	N/A	N/A	9.10
Automatic Mode Switching (PCM/DoP mode)	16H	ADOPE	N/A	N/A	N/A	Y	Y	9.11

Note 1. The digital filter is fixed to super slow roll-off filter in Oct Speed Mode and Hex Speed Mode.
Note 2. Only available in Normal Speed Mode.

6. Recommended States when Changing Clock Frequency or Pin/Register Setting

Power Down, Standby and Reset functions of the AK4462 are controlled by PDN pin, PW bit, MCLK and RSTN bit (Table 6).

Table 6. Power Down, Standby, and Reset Function (x: do not care)

State	PDN pin	MCLK Input	PW bit	RSTN bit	Analog Output
Power Down	L	x	x	x	Hi-Z
Standby	H	No	x	x	Hi-Z
	H	Yes	0	x	Hi-Z
Reset	H	Yes	1	0	(VREFH +VREFL)/2
Normal Operation	H	Yes	1	1	Signal output

This chapter describes which states the AK4462 should be in when changing clock frequency, control pin settings and register settings.

6.1. Clock Frequency

Table 7 shows the states that are allowed when changing the clock frequencies or are stopped.

Table 7. Permitted States When Changing Clock Frequencies
(Y: Permitted, N/A: Not Permitted)

Clock	Power Down	Standby	Reset	Normal Operation	Notes
MCLK frequency	Y	Y	Y	N/A	-
BICK frequency	Y	Y	Y	N/A	Note 3 Note 4
LRCK frequency	Y	Y	Y	N/A	Note 3 Note 4
DCLK frequency	Y	Y	Y	N/A	Note 4

Note 3. When ACKS bit = “0”, BICK and LRCK frequencies must be changed in the standby or reset state. It is possible to change BICK and LRCK frequencies during normal operation when ACKS bit = “1”, but click noise may occur. This click noise can be avoided by the external mute circuit.

Note 4. When the AK4462 is in the auto-switching functions (ADPE bit = "1" or ADOPE bit = "1"), being in reset state is not necessarily required for switching the D/A conversion mode. Use these functions according to the procedures described in sections 9.10 and 9.11 in the datasheet.

6.2. Control Pin Setting (Pin Control Mode)

Table 8 shows the states that are allowed when changing the pin settings in pin control mode.

Table 8. Permitted States When Changing Control Pin Settings (Pin Control Mode)
(Y: Permitted, N/A: Not Permitted)

Pin	Power Down	Standby	Normal Operation	Notes
DIF	Y	Y	N/A	-
TDM0/1	Y	Y	N/A	-
SMUTE	Y	Y	Y	-

6.3. Register Setting (Register Control Mode)

Table 9 shows the states that are allowed when changing register settings in register control mode.

Table 9. Permitted States When Changing Register Settings (Register Control Mode)
(Y: Permitted, N/A: Not Permitted)

Register	Standby	Reset	Normal Operation	Notes
DIF[2:0]	Y	Y	N/A	-
ACKS	Y	Y	N/A	-
SMUTE	Y	Y	Y	-
DEM[1:0]	Y	Y	Y	Note 5
DFS[2:0]	Y	Y	N/A	-
SD, SLOW, SSLOW	Y	Y	N/A	Note 6
SELLR	Y	Y	Y	Note 5
DZFB	Y	Y	Y	-
MONO	Y	Y	Y	Note 5
DCKB	Y	Y	N/A	-
DCKS	Y	Y	N/A	-
DP	Y	Y	N/A	-
ATTL[7:0], ATTR[7:0]	Y	Y	Y	-
INVL, INVR	Y	Y	Y	Note 5
DSDSEL[1:0]	Y	Y	N/A	-
DSDD	Y	Y	N/A	-
DDMT	Y	Y	N/A	-
DDMOE	Y	Y	Y	-
DDM	Y	Y	N/A	-
SYNCE	Y	Y	N/A	-
L, R	Y	Y	Y	-
DSDF	Y	Y	Y	Note 5
SDS[2:0]	Y	Y	Y	Note 5
TDM[1:0]	Y	Y	N/A	-
ATS[1:0]	Y	Y	Y	Note 7
ADPT[1:0]	Y	Y	N/A	-
ADPE	Y	Y	N/A	-
ADOPE	Y	Y	N/A	-
DMMI	Y	Y	N/A	-
DOP	Y	Y	N/A	-
DOPSEL[1:0]	Y	Y	N/A	-
DSDMARKERE/O	Y	Y	N/A	-

Note 5. When switching in the normal operation state, it is recommended to switch at zero-data input or soft-mute state by SMUTE bit = "1" in order to avoid click noise during switching.

Note 6. Click noise may occur when the digital filter setting is changed. If click noise can be avoided by the external mute circuit, digital filter setting can be changed during normal operation.

Note 7. Do not change the ATS[1:0] bits while operating gain transition by SMUTE bit, ATTL[7:0] bits and ATTR[7:0] bits switching.

7. Latency in Each Playback Mode

Latency is the internal processing time it takes for the input digital data to be output as an analog signal.

7.1. PCM mode

Latency in PCM mode is the time from when the impulse data is set in the input register until the peak of the analog signal is output (Figure 2). The latency at PCM mode is the sum of the digital filter group delay and the other operational delays shown below.

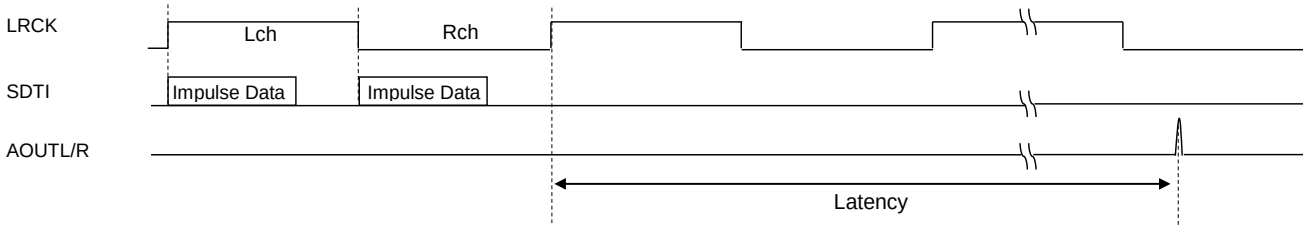

Figure 2. PCM mode Latency

In PCM mode, group delays such as Table 10 occur according to the settings of the digital filter.

Table 10. Group Delay (PCM mode)

SSLOW bit	SD bit	SLOW bit	Mode	Group Delay (Note 8)	
0	0	0	Sharp roll-off filter	26.8/fs	
0	0	1	Slow roll-off filter	6.3/fs	
0	1	0	Short delay sharp roll-off filter	5.8/fs	(default)
0	1	1	Short delay slow roll-off filter	4.8/fs	
1	0	x	Super slow roll-off filter	1.0/fs–2.5/fs (Note 9)	
1	1	x	Low dispersion short delay filter	10.5/fs	

Note 8. When the AK4462 is in Oct Speed Mode or Hex Speed Mode, Super Slow roll-off filter is selected regardless of SSLOW/SD/SLOW bit setting.

Note 9. 1.0/fs in Normal Speed Mode. It varies in the range of 1.0/fs-2.5/fs depending on the Sampling Speed setting.

When PCM/DSD automatic mode switching function is used (ADPE bit = "1"), a delay of 18/fs occurs due to internal operation (Table 11).

Table 11. Operational Delay Caused by ADPE Setting (PCM mode)

ADPE bit	Operation Delay	
0	0/fs	(default)
1	18/fs	

In addition, in PCM mode, there is a delay error due to the timing of capturing data at the data interface. The delay error depends on the Synchronization Function (SYNCE bit) setting (Table 12).

Table 12. Delay Error at the Data Interface (PCM mode)

SYNCE bit	Delay Error	
0	<±1/fs	
1	<±0.3 μs	(default)

(e.g.) Latency when PCM mode, fs = 44.1 kHz, Sharp Roll-off filter, ADPE bit = "1" and SYNCE bit = "0"

Latency = (26.8 + 18 ± 1)/fs = (44.8 ± 1)/fs = 1016 ± 23 μs

7.2. DSD mode

Latency in DSD mode is approximately 8 µs in DSD64 mode, which varies slightly depending on the operation rate and DSDF bit.

However, when the DSD full-scale detection function is used (DDM bit = "1"), a register delay described in Table 13 occurs according to DDMT bit setting.

Table 13. Register Delay (DSD mode, x: Do not Care)

DDM bit	DDMT bit	Register Delay	
0	x	0	(default)
1	0	264 DCLK cycle	
1	1	136 DCLK cycle	

(e.g.) Latency when DSD64 (DCLK = 2.8224 MHz), DSDF bit = "0", DDM bit = "1", and DDMT bit = "0"

Latency = 8 µs + 264 DCLK = 102 µs

7.3. DoP mode

Latency in DoP mode is the time from when the impulse data is set in the input register until the peak of the analog signal is output (Figure 3). The latency at DoP mode is the sum of the group delay and the register delay shown below.

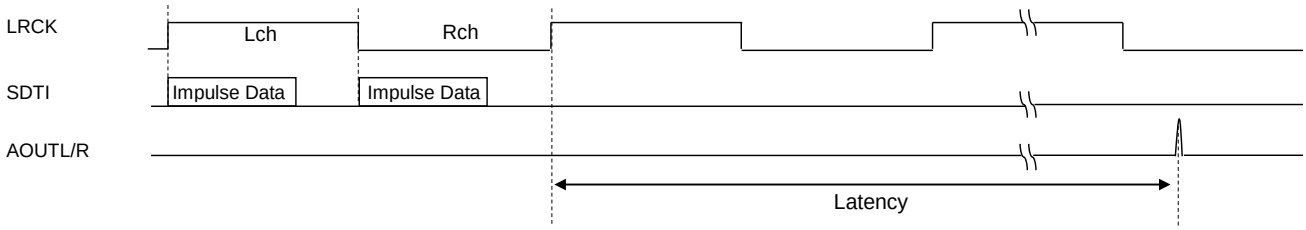

Figure 3. DoP mode Latency

In DoP mode, group delays such as Table 14 occur according to DSDF bit settings.

Table 14. Group Delay (DoP mode)

DSDF	Group Delay	
	DoP64/128/256	
0	2.4 LRCK cycle	(default)
1	1.9 LRCK cycle	

When the DSD full-scale detection function is used (DDM bit = "1"), a register delay described in Table 15 is generated according to DDMT bit setting.

Table 15. Register Delay (DoP mode)

DDM bit	DDMT bit	Register Delay	
0	x	0	(default)
1	0	16.5 LRCK cycle	
1	1	8.5 LRCK cycle	

In addition, in DoP mode, there is a delay error due to the timing of capturing data at the data interface. The delay error depends on the synchronization Function (SYNCE bit) setting (Table 16).

Table 16. Delay Error at the Data Interface (DoP mode)

SYNCE bit	Delay Error	
0	<±1 LRCK cycle	
1	<±0.3 μs	(default)

(e.g.) Latency when DoP64 (BCLK = 2.8224 MHz, LRCK = 176.4 kHz), DSDF bit = "0", DDM bit = "1", DDMT bit = "0", and SYNCE bit = "0"

Latency = (2.4 + 16.5 ± 1) LRCK cycle = 107 ± 6 μs

8. Design of Analog Output Post-Circuit

8.1. Calculation of the DC load resistance

The external circuit after the analog output pins (AOUTP, AOUTN) must be designed so that its DC load resistance (R_L) complies with the "Load Resistance" specifications given in section 8.1 in the datasheet. The R_L is the effective resistance between the analog output pins and the system analog ground (Figure 4). This section describes how to calculate the DC load resistance by referring to the circuit as shown in Figure 5.

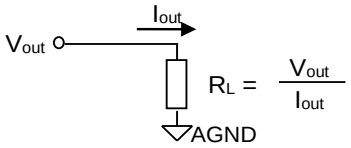

Figure 4. Schematic Diagram of the R_L

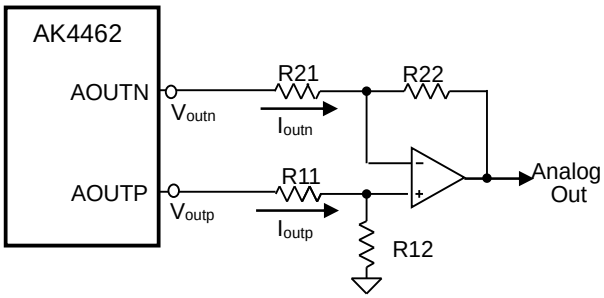

Figure 5. Example of Differential-to-Single Circuit

The R_L is determined by $R_L = V_a/I_a$ from I_a at full-scale output current and output voltage V_a of AOUTx pin (Figure 6). For normal operation of the AK4462, both the R_{Lp} (R_L of AOUTP pin) and the R_{Ln} (R_L of AOUTN pin) must satisfy the specification ($R_L \geq 1.4$ kΩ).

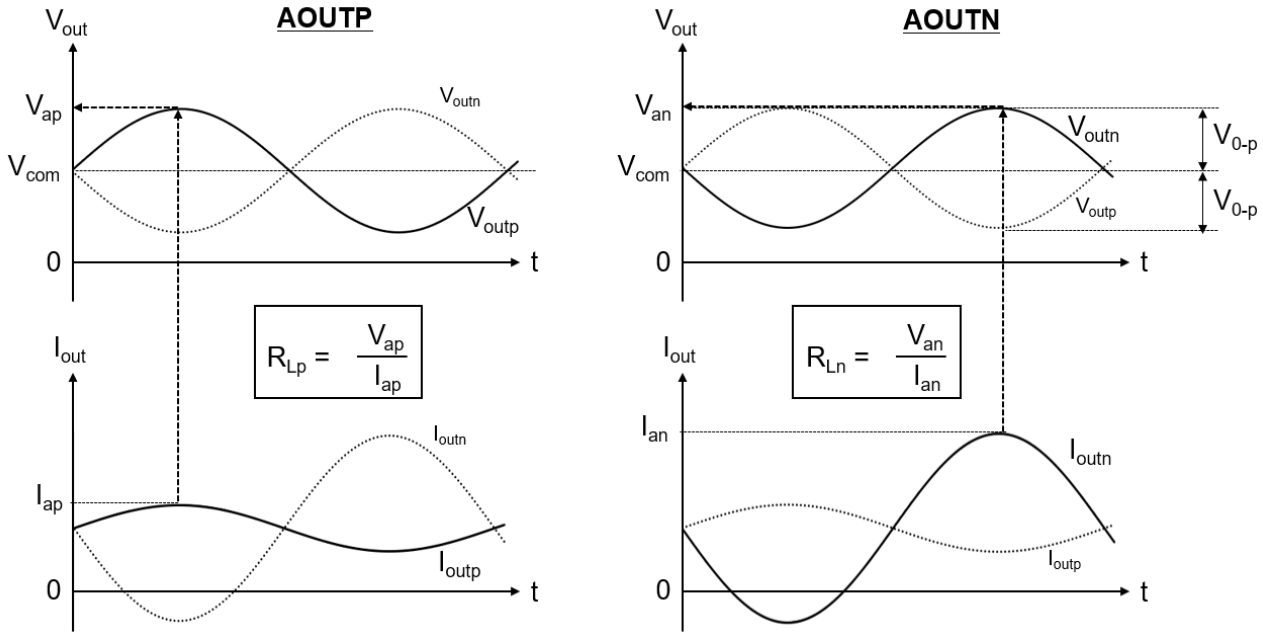

Figure 6. R_{Lp} and R_{Ln} in the Figure 5 Schematic

In Figure 5 case, the R_{Lp} and the R_{Ln} are,

$$R_{Lp} = \frac{V_{ap}}{I_{ap}} = R_{11} + R_{12}$$

$$R_{Ln} = \frac{V_{an}}{I_{an}} = \frac{\left(V_{com} + V_{0-\mathrm{p}}\right)(R_{11} + R_{12})R_{21}}{R_{11}V_{com} + (R_{11} + 2R_{12})V_{0-\mathrm{p}}}$$

Where,

$$V_{COM} = 0.5(VREFH - VREFL)$$

$$V_{0-\mathrm{p}} = 0.28(VREFH - VREFL)$$

8.2. Filter Design

The formula for calculating the parameters of the second-order low-pass filter shown in Figure 7 is shown below.

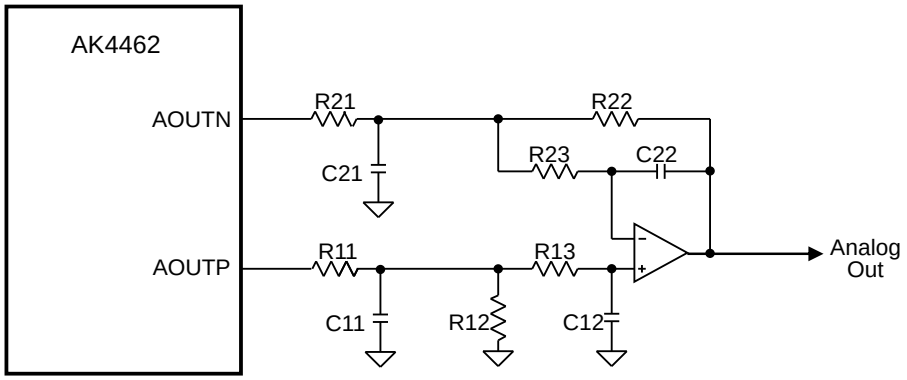

Figure 7. Second-Order Low-Pass Filter Circuit Example

$$DC\ Gain = \frac{0.5(R_{21}R_{12} + R_{11}R_{22}) + R_{12}R_{22}}{R_{21}(R_{11} + R_{12})}$$

$$f_{cp} = \frac{\omega_{0p}}{2\pi} \quad , \quad f_{cn} = \frac{\omega_{0n}}{2\pi}$$

$$\omega_{0p} = \frac{1}{\sqrt{C_{11}C_{12}R_{12}R_{13}}} \quad , \quad \omega_{0n} = \frac{1}{\sqrt{C_{21}C_{22}R_{22}R_{23}}}$$

$$Q_p = \frac{C_{11}\omega_{0p}}{\frac{1}{R_{11}} + \frac{1}{R_{12}} + \frac{1}{R_{13}}} \quad , \quad Q_n = \frac{C_{21}\omega_{0n}}{\frac{1}{R_{21}} + \frac{1}{R_{22}} + \frac{1}{R_{23}}}$$

$$R_{Lp} = \frac{V_{ap}}{I_{ap}} = R_{11} + R_{12}$$

$$R_{Ln} = \frac{V_{an}}{I_{an}} = \frac{(V_{com} + V_{0-p})(R_{11} + R_{12})R_{21}}{R_{11}V_{com} + (R_{11} + 2R_{12})V_{0-p}}$$

9. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
20/08/17	01	First Edition		
20/09/1	02	Error Correction	9	Table9 DSDD in Normal Operation "Y" → "N/A"
		Description Addition	10	Added Note9