Intel® Programmable Acceleration Card (PAC) with Intel® Arria® 10 GX FPGA Data Sheet

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Contents

1. Introduction

Figure 1. Intel® Programmable Acceleration Card with Intel® Arria® 10 GX FPGA

This datasheet for the Intel® PAC with Intel Arria® 10 GX FPGA shows electrical, mechanical, compliance, and other key specifications. This datasheet assists data center operators and system integrators to properly deploy this PAC into their servers. It also documents the FPGA power envelope, connectivity speeds to memory, and network connectivity, so that accelerator function unit (AFU) developers can properly design and test their IP.

The PAC is supported by the Intel Acceleration Stack for Intel Xeon® CPU with FPGAs. The Intel Acceleration Stack provides a common developer interface to both application and acceleration function developers and includes drivers, Application Programming Interfaces (APIs) and an FPGA Interface Manager (FIM).

Along with acceleration libraries and development tools, the Acceleration Stack saves development time and enables code re-use across multiple Intel FPGA form-factor products, allowing the developer to focus on the unique value-additon of their solution. Developers can use the Accelerator Functional Unit Developer's Guide for Intel FPGA Programmable Acceleration Card to get started.

Intel validates each Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA to support large scale deployments requiring FPGA acceleration. This platform is targeted for market-specific acceleration in applications such as:

- Big Data Analytics
- Artificial Intelligence
- Video Transcoding
- Cyber Security
- Genomics
- High-Performance Computing
- Finance

Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Arria 10 GX FPGA

2. Overview

This chapter provides an overview of the programmable acceleration card and describes the board architecture and its components.

2.1. Views of the Intel PAC with Intel Arria 10 GX FPGA

Figure 2. Intel PAC with Intel Arria 10 GX FPGA

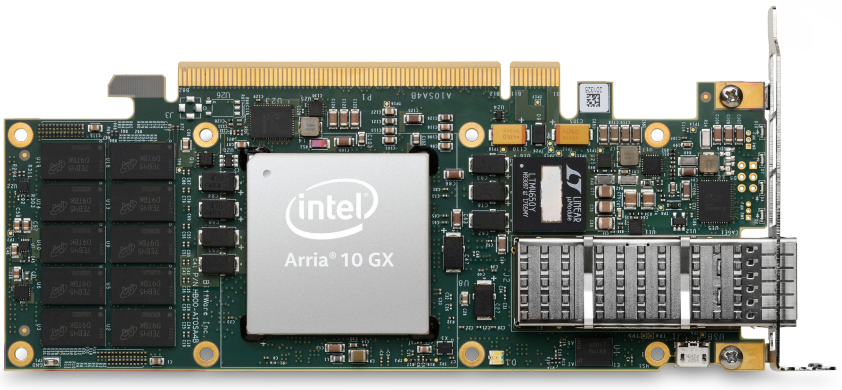
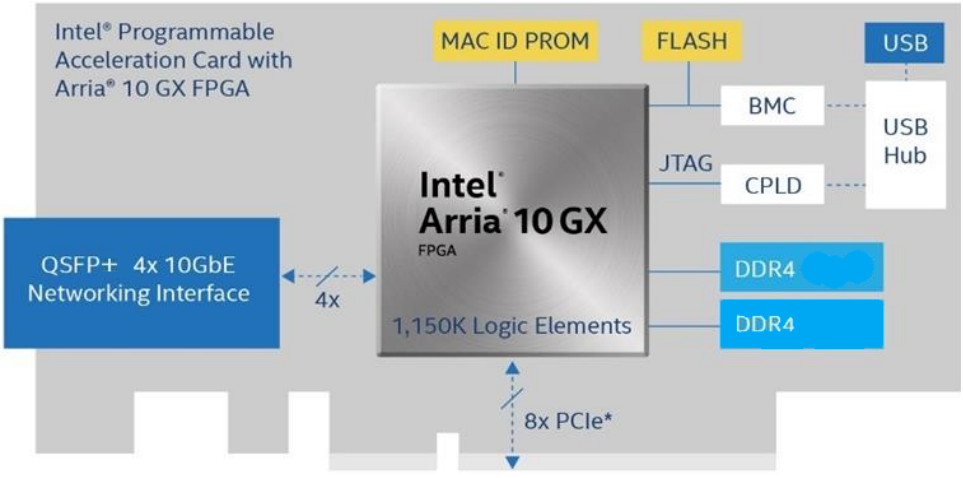


Figure 3. Intel PAC with Intel Arria 10 GX FPGA Conceptual View



2.2. Overview of Product Features

2.2.1. Intel Arria 10 GX FPGA

The Intel Arria 10 FPGAs feature industry-leading programmable logic built on 20 nm process technology that integrate a rich feature set of embedded peripherals, embedded high-speed transceivers, hard memory controllers and IP protocol controllers. Variable-precision digital signal processing (DSP) blocks integrated with hardened floating point (IEEE 754-compliant) enable the Intel Arria 10 FPGAs to deliver floating point performance of up to 1.5 TFLOPS. Arria 10 FPGAs have a comprehensive set of power-saving features. Combined, these features allow developers to build versatile set of acceleration solutions.

When developing the accelerator function for the Intel PAC, select the 10AX115N2F40E2LG device.

Related Information

- Intel FPGA Devices
  Detailed information about features of the Intel Arria 10 GX FPGA family
- Intel Arria 10 Device Datasheet
  This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Intel Arria 10 devices.
- Intel Arria 10 Device Overview
  This device overview provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

2.2.2. On-Board Memory

- 8 GB Double Data Rate 4 (DDR-4 SDRAM) memory
  - Two 4 GB DDR-4 memory banks, part number MT40A512M16JY-083E:B
  - 2133 MT/s per DDR-4 memory bank
  - Transfer width: 64 data bits

  Note: Refer to the *Accelerator Functional Unit Developer's Guide for Intel FPGA Programmable Acceleration Card* for access within the FIM to this memory link.
- One 1 GB (128 MB) Flash – for use with the FIM

Related Information

Accelerator Functional Unit (AFU) Developer's Guide

2.2.3. Interfaces and Dimensions

- PCI Express (PCIe) x8 Gen3 electrical, x16 mechanical for stability

  Note: The Intel PAC with Intel Arria 10 GX FPGA does not support PCIe Gen4.
- USB 2.0 interface for debugging.
- 1x Quad Small Form Factor Pluggable+ (QSFP+) with 4x 10GbE or 40GbE support.
- The Intel PAC fits into 1U servers.

- ½ Length, full height card with air duct installed (default)
- ½ Length, ½ height card with air duct removed and low profile bracket installed
- Standard bracket available with air duct addition available.

Note: One rack unit is 44.5 mm (1.75 inches) high. One rack unit is commonly designated as "1U".

2.2.4. Software

- Acceleration Stack for Intel Xeon CPU with FPGAs
- FIM Installed in Intel PAC board flash

  Note: Certain development sample boards may be supplied without the FIM installed.
- Board Management Controller firmware

Related Information

Intel FPGA Acceleration Hub
Information about the Intel Acceleration Stack.

2.2.5. Power

- 66 W Thermal Design Power (TDP)
  - The TDP is based on the max current, per the PCIe specification, of 5.5A on the 12V rail.
  - As the developers or solution provider, you must ensure that the AFU does not exceed this limit or the limit provided by the qualified server vendor. Functionality and reliability of the server is not supported for AFUs that exceed the specification.
- Up to 45 W FPGA power consumption
- The PAC source power is from the 12V rail of the PCIe* edge connector. The PAC does not draw power from the 3.3V rail.

2.2.6. CPLD

The CPLD is an Intel FPGA Download Cable. JTAG is used for debug and instances where the FIM image is corrupted or needs to be updated.

2.2.7. QSFP+

The Intel PAC with Intel Arria 10 GX FPGA has a QSFP+ cage on the front panel which supports 40GbE or four 10GbE.

The table below details the Intel-supported connectors. For volume deployment, you must use Intel-validated QSFP+ cables.

Successful functioning of 40GbE and 10GbE requires appropriate physical medium attachment (PMA) settings. Run the provided PMA settings script as detailed in the *10Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide* or *40Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide*.

Table 1. QSFP+ Support for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

	Model Number
Intel Ethernet QSFP+ 1-meter direct attach cable (DAC) twinaxial cables	XLDACBL1
Intel Ethernet QSFP+ 3-meter direct attach cable (DAC) twinaxial cables	XLDACBL3
Intel Ethernet QSFP+ short reach (SR) optic module	E40GQSFPSR
Intel Ethernet QSFP+ 1-meter Passive Breakout Cable	X4DACBL1
Intel Ethernet QSFP+ 3-meter Passive Breakout Cable	X4DACBL3

Switches

Intel has used the following switches in their validation configuration.

Table 2. Intel-Validated Switches

Ethernet AFU	Switch Brand	Switch Model Number
40 Gbps Ethernet	Dell*	Z9100-ON
	Extreme Networks*	x870-32C
	Mellanox*	SN2700
10 Gbps Ethernet	Cisco*	Nexus N9K-C93180YC-EX
	Lenovo*	8272
	Dell	8024F

QSFP+ SerDes

The QSFP+ interface has four Serializer/Deserializer (SerDes) lanes connected directly to the FPGA.

Related Information

- *Running 10GbE PAC-to-PAC Test between two connected PACs* in the *10Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide*
- *Running 40GbE PAC-to-PAC Test between two connected PACs* in the *40Gbps Ethernet Accelerator Functional Unit (AFU) Design Example User Guide*

2.2.8. Control and Support

The following features are available on this acceleration card for configuration, control and support:

- PCIe
- Board Management Controller (BMC)

2.2.8.1. PCIe Overview

This acceleration card has a PCIe interface for configuration in select cases. When Intel Acceleration Stack for Intel Xeon CPU with FPGAs version 1.2.1 and the latest BMC firmware are installed, the PCIe interface can be used for the following:

- Read/write Intel Arria 10 FPGA configuration in Flash
- Read manufacturing data
- Monitor on-board temperature and power
- Update the board's BMC firmware

2.2.8.2. Board Management Controller Overview

The Board Management Controller (BMC) is responsible for controlling, monitoring and giving low-level access to board features. The BMC microcontroller interfaces with on-board sensors, the FPGA and the flash, and it controls power and resets. The microcontroller communicates over PCIe I^2C using:

- Platform Level Data Model (PLDM) for Platform Monitoring and Control version 1.1.1
- The Open Programmable Acceleration Engine (OPAE) FPGA tool

The firmware that runs on the BMC microcontroller is field upgradeable over PCIe.

You can flash the BMC firmware and read sensor data with the OPAE commands `fpgasupdate` and `fpgainfo`.

For more details, refer to the *Board Management Controller* section.

Related Information

Board Management Controller on page 19

3. System Compatibility

This section describes the platforms and Linux™ distribution targeted for the acceleration card validation.

Platforms

Refer to the Qualified Servers and Ordering Information page for a list of the latest qualified servers.

Operating System Validation

Table 3. Operating System Validation

Operating Systems (OS)	OS Family
RHEL™ 7.6 Kernel 3.10	RHEL
Ubuntu 18.04 Kernel 4.15	Ubuntu

Adapters must have the following PCIe ID and power/thermal budget.

Note:

- VID - Vendor ID
- SVID - Sub Vendor ID
- DID - Device ID
- SDID - Sub Device ID

Table 4. PCIe ID and Power/Thermal Budget

PAC	PCIe VID	PCIe DID	PCIe SVID	PCIe SDID
Intel PAC with Intel Arria 10 GX FPGA	0x8086	0x09C4	0x8086	0x0000

Table 5. Ordering Code vs. Intel Acceleration Stack Version Compatibility

	Intel Acceleration Stack Version			
Ordering Code	1.0	1.1	1.2	1.2.1
DK-ACB-10AX115**1A**ES	Yes	Yes	Yes	Yes
DK-ACB-10AX115**2A**ES	Not validated	Yes	Yes	Yes

Note: If you purchased a board from a qualified OEM, please contact the OEM to confirm which version(s) of the Acceleration Stack it supports.

Table 6. Validated BMC and Intel Acceleration Stack Versions

Intel Acceleration Stack Version	BMC Firmware Version
1.0	26815
1.1 Alpha	26819
1.1 Beta and Production	26822
1.2	26889
1.2.1 PV	26895

PACs ordered under the following codes are development samples and should not be used for volume deployment.

Table 7. Development Samples

OPN	MM#
DK-ACB-10AX1151AES	980016
DK-ACB-10AX1152AES	980017

4. Mechanical Information

Dimensions of the Intel PAC with Intel Arria 10 GX FPGA

- Standard height, half length PCIe card
- Low profile option available
- Card Weight with air duct: 255 g
- Maximum component height: 14.47 mm
- PCIe x16 mechanical

Figure 4. Acceleration Card - Standard Profile Bracket with Airduct

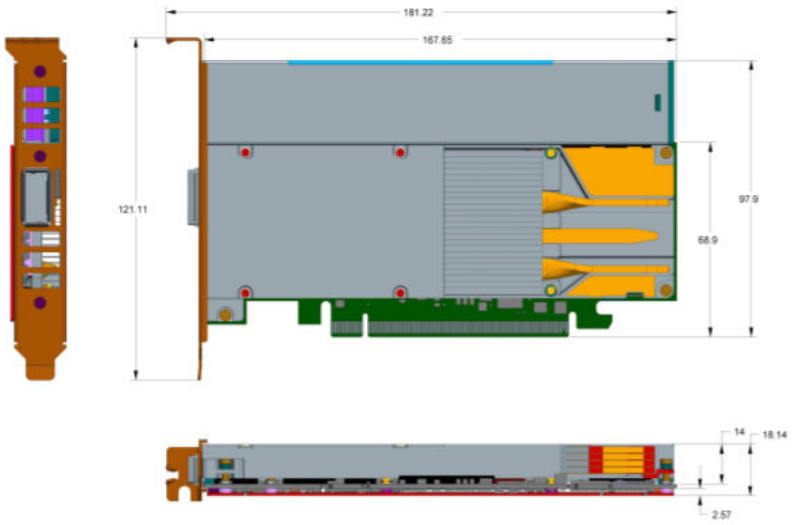


Figure 5. Air Duct Assembly

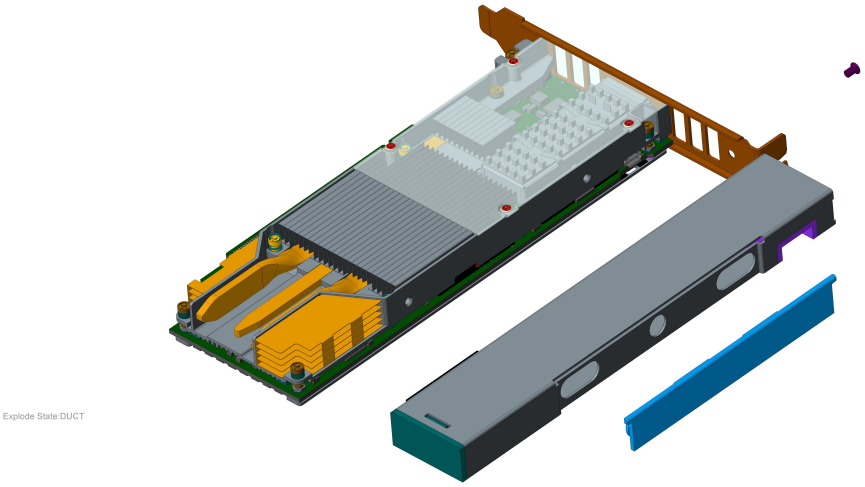


Figure 6. Acceleration Card - Low Profile Bracket

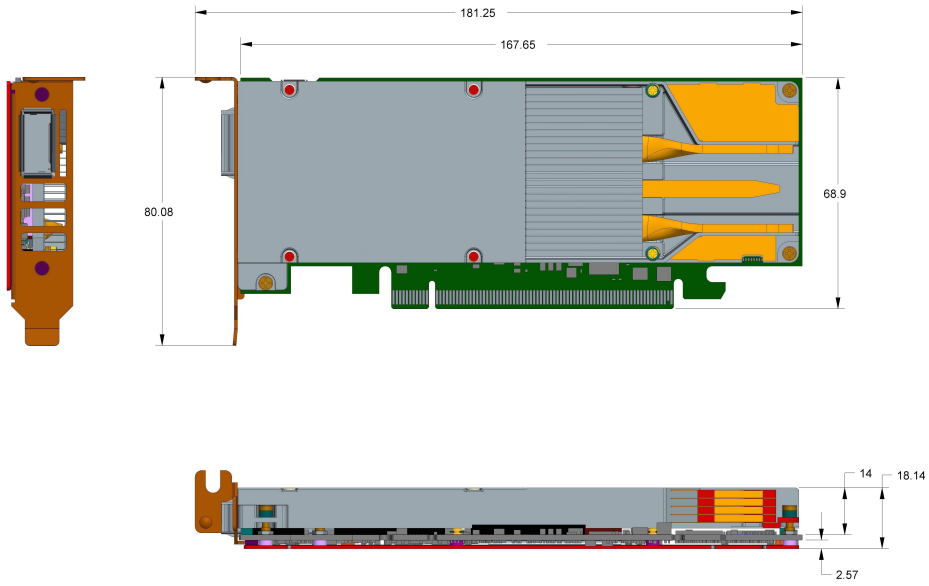
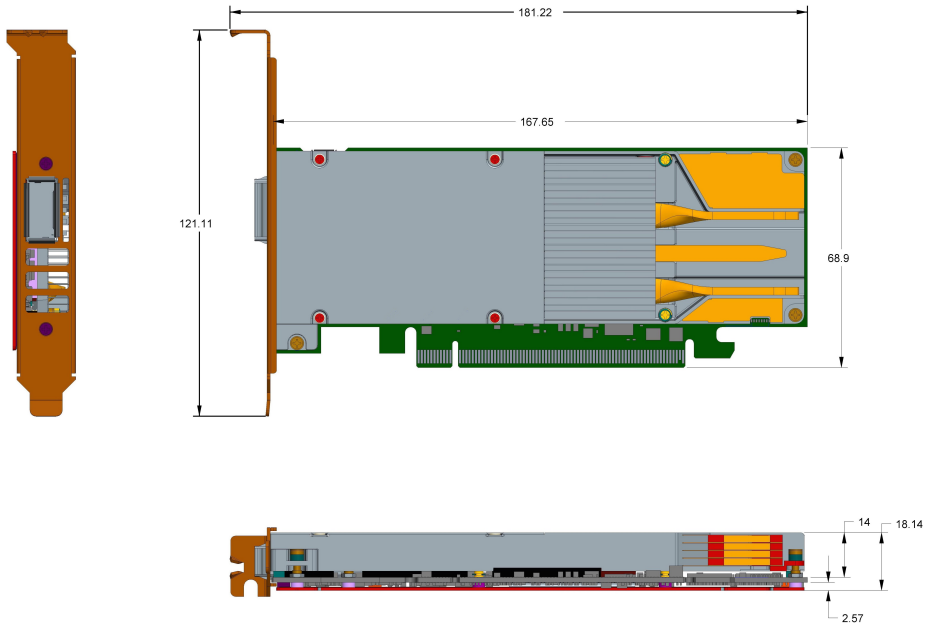


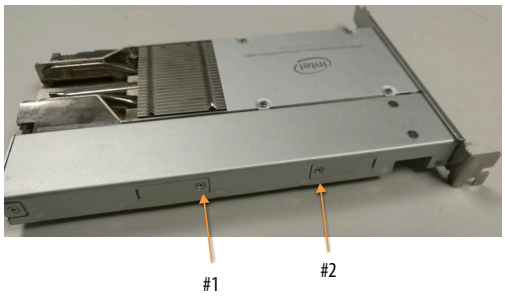
Figure 7. Acceleration Card - Standard Profile Bracket with No Air Duct

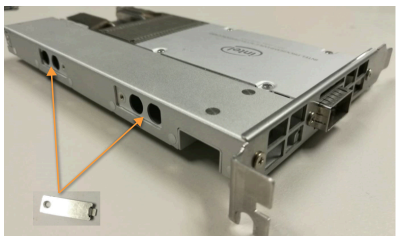


4.1. Air Duct Disassembly

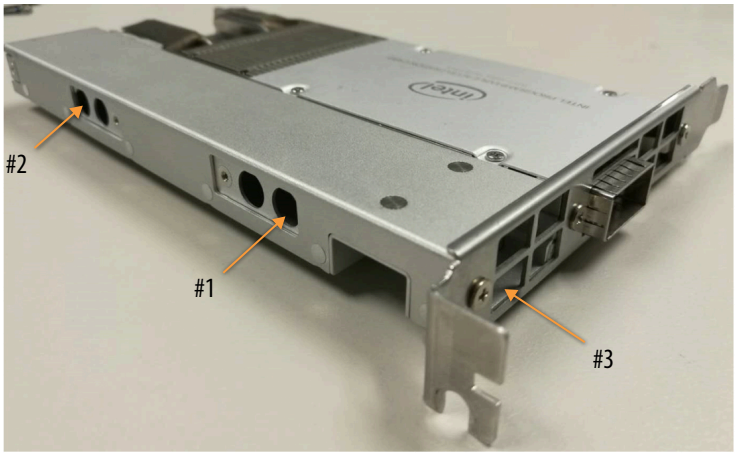
Removal of air duct requires a different bracket to be used. Additional bracket options are available in Development Sample only to support the Intel PAC with Intel Arria 10 GX FPGA without air duct.

1. Unscrew two M2x3 screws with 1.5+/-0.5 LBF.INCH torque and then remove two piece covers from air duct.

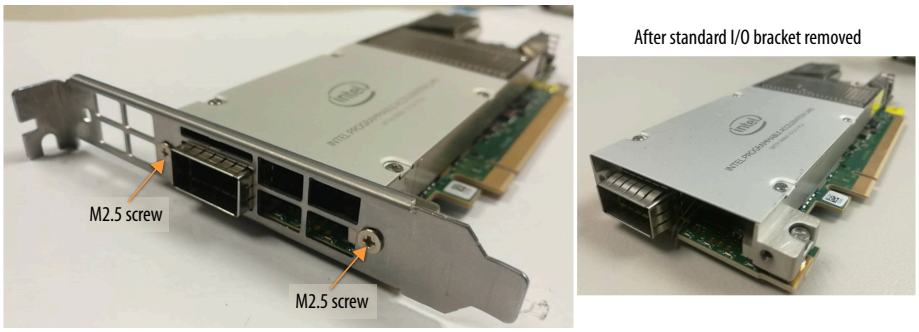



Cover Removed

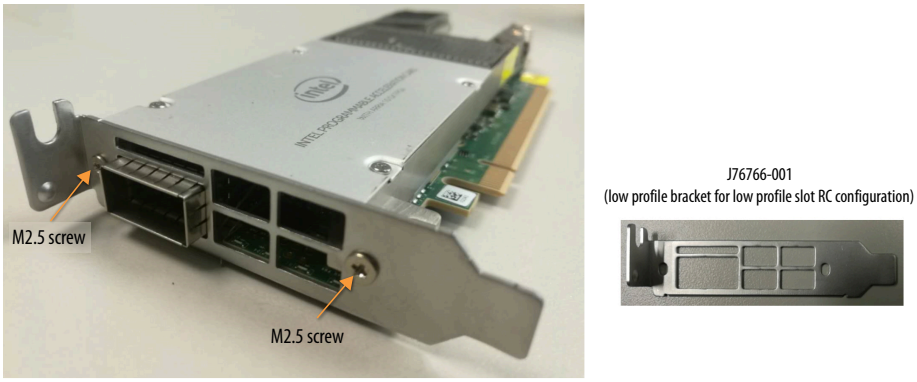
2. After removing the covers, unfasten the two captive screws (#1 & #2) from the slots on air duct side wall. Also unscrew other M2.5 screw (#3) from I/O bracket. The whole air duct can now be easily disassembled.



3. For I/O Bracket disassembly, remove the other two M2.5 screws then take out PCIe bracket from the Intel PAC with Intel Arria 10 GX FPGA.



4. For Low Profile I/O Bracket Assembly, use a Phillips screwdriver with 3+/-0.5LBF.inch torque to fasten two M2.5 screws with low profile I/O Bracket.



5. Thermal Specifications

This acceleration card is thermally limited to dissipate no more than 45 W on the FPGA. FPGA junction temperature must not exceed 95°C. Make sure the temperature of the QSFP+ module is within the vendor specification, usually 70°C or 85°C.

- Operating Temperature: 95 °C
- Shutdown Temperature: 100 °C

Refer to the Power Estimator Guide to avoid exceeding 95 °C. Refer to *AN 872: Thermal and Power Guidelines: For Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA* to verify and ensure that the AFU operates within the power supported by the Intel PAC with Intel Arria 10 GX FPGA.

AFU Developers should use the Arria 10 PowerPlay Early Power Estimator and the Intel Quartus® Prime Power Analyzer to estimate power consumption.

Figure 8. Airflow Pattern

Related Information

- Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition
  The Intel Quartus Prime Pro Edition software provides a complete design environment for FPGA and SoC designs. The Power Analyzer is described in the Power Analysis and Optimization User Guide: Intel Quartus Prime Pro Edition.
- AN 872: Thermal and Power Guidelines: For Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

5.1. Thermal Test Performance Results

Table 8. Terms and Descriptions

Term	Description
Linear Feet per Minute (LFM)	Air velocity is calculated by dividing the volumetric flow rate by the cross-sectional area of the flow passage.
T_{LA}	The measured ambient temperature locally surrounding the FPGA. The ambient temperature should be measured just upstream of a passive heatsink or at fan inlet for an active heatsink.

Table 9. T_{LA} vs. Velocity Profile with Air Duct

T_{LA} (°C)	Velocity (LFM) (85 °C QSFP spec)	Velocity (LFM) (70 °C QSFP spec)
30	270	270
35	300	300
40	360	360
45	420	420
50	510	510
55	660	690

Table 10. T_{LA} vs. Velocity Profile without Air Duct

T_{LA} (°C)	Velocity (LFM) (85 °C QSFP spec)	Velocity (LFM) (70 °C QSFP spec)
30	330	330
35	390	390
40	420	420
45	510	510
50	600	630
55	810	870

6. FPGA Interface Manager

The FPGA Interface Manager (FIM) contains the FPGA logic to support the accelerators, including the PCIe IP core, the Core Cache Interface protocol (CCI-P) fabric, the onboard DDR memory interface, and management engine. Specific features of the FIM are listed in the following documents:

- Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
- OPAE Intel FPGA Linux Device Driver Architecture Guide
- FPGA Interface Manager Data Sheet for Intel FPGA Programmable Acceleration Card with Intel Arria 10 GX FPGA

The 1024 Mb flash memory stores the FPGA Interface Manager (FIM) which provides a common user interface for placement of accelerator functions. In addition, the FIM allows dynamic downloading of new accelerator functions and updates to the FIM.

The FIM can read all sensor data from the BMC, using the Intel Acceleration Stack. For example, to read the FPGA temperature, use the following command:

```
sudo fpgainfo temp
```

To read voltage and current data, use the following command:

```
sudo fpgainfo power
```

Refer to the Intel Acceleration Stack Quick Start Guide for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA to learn how to use these features.

6.1. Updating the FIM

The FIM image in flash memory can be updated over PCIe via the Acceleration Stack. This loads the FIM image into the onboard flash memory. Upon power up, the board loads the image from flash onto the FPGA.

Note: Please refer to the Intel Acceleration Stack Quick Start Guide for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA for instructions on updating the FIM.

7. Board Management Controller

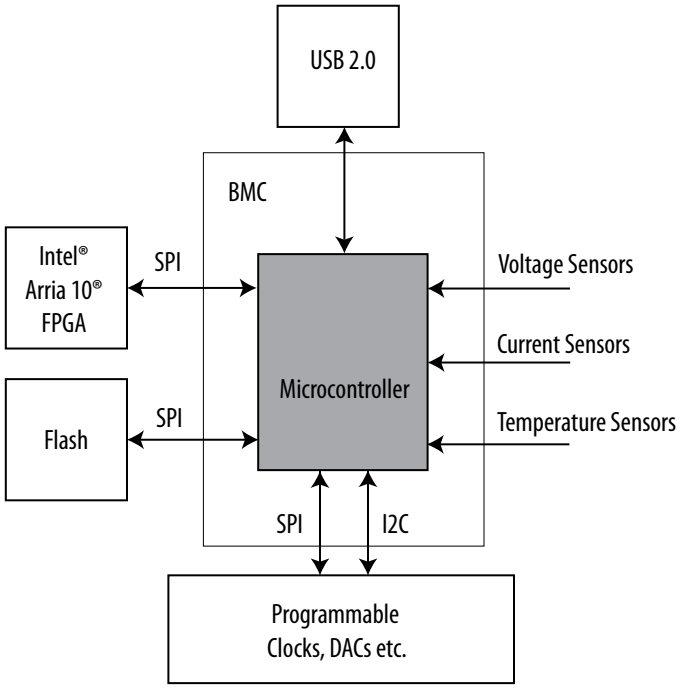
A board management controller (BMC) resides on the Intel PAC with Intel Arria 10 GX FPGA.

7.1. Features

The on-board microcontroller:

- Provides low-level access to board features.
- Interfaces with sensors, FPGA, flash and QSFP.
- Controls power and resets on the board.
- Monitors temperatures, voltages and currents and provides protective action when readings are outside of critical thresholds.
- Provides Platform Level Data Model (PLDM) for PCIe I^2C communication. The I^2C slave address is 0xCE.
- Supports field upgrades of BMC firmware.

Figure 9. Board Management Controller for the Intel PAC with Intel Arria 10 GX FPGA



7.1.1. BMC Voltage and Thermal Handling

The BMC powers down the Intel PAC with Intel Arria 10 GX FPGA and reboots the server if the power, temperature or voltage reaches a certain threshold. This response prevents damage to the server or Intel PAC with Intel Arria 10 GX FPGA.

For threshold limits refer to the *Device Peripheral Table* section. This table shows the upper non-recoverable (UNR) value, which specifies the shutdown condition. The BMC will shut down power to the board under conditions that include the following:

- Backplane voltage reaches 14 V, or current reaches 6A (i.e., a maximum of 84W total power)
- FPGA junction temperature reaches 100°C

Note: The backplane power limits shown above are sufficient to protect the Intel PAC with Intel Arria 10 GX FPGA hardware. If your server components require more conservative limits, you can change any threshold using PLDM commands as described in *PLDM Commands for the Board Management Controller*.

To avoid unintended shutdown and loss of data:

- Use an Intel-validated server.
- Perform extensive power validation and consumption analysis on worst-case workloads.
- Use a qualified solution that is stress-tested across multiple servers and long durations.
- Enable the *pacd* daemon. This system service monitors sensor readings versus defined thresholds, and disables access to the Intel PAC when it exceeds a threshold. For information about *pacd*, refer to *OPAE FPGA Tools* in the Open Programmable Acceleration Engine page.

You can identify whether the BMC has detected a board failure from the two on-board LEDs. Looking into the bracket of the Intel PAC through the venting holes on the back side of the server, you can see four steadily ON green LEDs. Behind them (further into the board), there is either a green LED or red LED that is on. The green LED blinks whenever the BMC is operating and is steadily on if the BMC is being initialized. When the BMC detects a failure condition and holds off board power, a red LED (next to the green LED) will be steadily on. Board failure conditions may occur because of an overheated FPGA or too much power draw from the board.

Related Information

PLDM Commands for the Board Management Controller on page 23

7.2. Device Peripheral Table

The following table describes the peripherals, currents or voltages that you can monitor on the Intel PAC with Intel Arria 10 GX FPGA:

- Type: Indicates the origin of measurement
- Channel and Address columns: Indicate the virtual I^2C channel and address that are used to access the peripheral through the microcontroller.
- ID (DEV/PDR): Indicates the platform descriptor record (PDR) index; otherwise, indicates the device number (DEV), if any, to be passed to the relevant PLDM command.
- UNC: Upper non-critical value
- UC: Upper critical value
- UNR: Upper non-recoverable value: the threshold for power shutdown(1)

Table 11. Device Peripheral Table

Name	Type	Channel	Address	ID (DEV/ PDR)	UNC	UC	UNR	Description
Board Power	Sensor	-	-	0	75	100	113	-
12v Backplane Current	Sensor	5	0xD4	1	5.5	6	6	LTC4151 Input Current
12v Backplane Voltage	Sensor	5	0xD4	2	13.5	14	14	LTC4151 Input Voltage
1.2v Current	Sensor	6	0xD0	4	12	13	15	LTC4151 Output Current
1.2v Voltage	Sensor	6	0xD0	3	1.26	1.3	1.4	LTC4151 Output Voltage
1.8v Current	Sensor	6	0xD2	6	6	7	8	LTC4151 Output Current
1.8v Voltage	Sensor	6	0xD2	5	1.9	2	2.04	LTC4151 Output Voltage
3.3v Current	Sensor	6	0xD4	8	6	7	8	LTC4151 Output Current
3.3v Voltage	Sensor	6	0xD4	7	3.47	3.6	3.96	LTC4151 Output Voltage
FPGA Core Voltage	Sensor	6	0xDA	9	0.95	1	1.08	LTC4151 Output Voltage
FPGA Core Current	Sensor	6	0xDA	10	50	55	60	LTC4151 Output Current
FPGA Core Temperature	Sensor	0	0x98	11	90	95	100	NCT72CMTR2G External
Core Supply Temperature	Sensor	-	-	15	100	110	120	-
Board Temperature	Sensor	0	0x98	12	70	75	80	NCT72CMTR2G Local
QSFP Temperature	Sensor	3	0xA0	14	70	80	90	-
QSFP Voltage	Sensor	3	0xA0	13	3.4	3.5	3.7	-
VCCR Voltage	Sensor	-	-	17	-			
VCCT Voltage	Sensor	-	-	18	-	-	-	-

continued...

(1) For a detailed discussion of UNR, refer to *BMC Voltage and Thermal Handling*

Name	Type	Channel	Address	ID (DEV/ PDR)	UNC	UC	UNR	Description
VCCR Current	Sensor	-	-	19	-	-	-	-
VCCT Current	Sensor	-	-	20				
VPP Voltage	Sensor	-	-	21	-	-	-	-
VTT Voltage	Sensor	-	-	22	-	-	-	-
QSFP	SFP/QSFP	-	0xA0	1	-	-	-	-
Si5338	Programmable Clock	0	0xE0	0	-	-	-	Defaults to 125, 125, 266.666667, 266.666667
MAC Prom	Network	4	0xA0	-	-	-	-	AT24CS04

Note: The table above lists **ID (DEV/PDR)** (device IDs) based at 0, as shown by the `fpgainfo` command. However, the PLDM commands use device IDs based at 1. Therefore, when using PLDM commands, you must add 1 to the table device ID to obtain the PLDM device ID. For example, the board power ID is listed as 0 in the *Device Peripheral Table*, but in PLDM commands the board power ID is 1.

Refer to the Intel Acceleration Stack Quick Start Guide for the Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA for information about the `fpgainfo` command.

7.3. Updating the BMC Configuration and Firmware

Note: Refer to the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX* for information on updating the BMC Configuration and Firmware.

Related Information

- Intel Acceleration Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
- Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

8. PLDM Commands for the Board Management Controller

The BMC on the Intel PAC with Intel Arria 10 GX FPGA can communicate with a server BMC over the PCIe I^2C bus. The supported protocol is the PLDM over Management Component Transport Protocol (MCTP) stack.

The PAC BMC supports a subset of PLDM and MCTP commands, to enable a server BMC to obtain sensor data for fan control. The BMC supports version 1.1.1 of the PLDM for Platform Monitoring and Control standard (DTMF specification DSP0248). It does not support version 1.1.0.

For more information about the PLDM and MCTP protocol specifications, refer to *DMTF Specifications* on the Platform Management Components Intercommunication website.

Note: The PAC BMC does not break large MCTP packets down to 64-byte packets, as described in the MCTP specification for baseline transmission unit size. Otherwise the BMC is fully compliant to the DMTF specifications.

Related Information

Platform Management Components Intercommunication

8.1. I^2C/SMBus Address

The PCIe I^2C slave address of the Intel PAC with Intel Arria 10 GX FPGA is fixed at `0xCE`. There is no Address Resolution Protocol (ARP) support.

8.2. Supported SMBus Commands

- smbus_get_udid

8.3. Supported MCTP Commands

8.3.1. MCTP Control Messages

- mctp_set_endpoint_id
- mctp_get_endpoint_id
- mctp_get_endpoint_uuid
- mctp_get_mctp_version_support
- mctp_get_message_type_support
- mctp_get_vendor_defined_message_support

8.4. Supported PLDM Commands

8.4.1. PLDM Base Specification Commands

- pldm_settid
- pldm_gettid
- pldm_getterminusuid
- pldm_getpldmversion
- pldm_getpldmtypes
- pldm_etpldmcommands

8.4.2. PLDM for Platform Monitoring and Control Specification Commands

- pldm_settid
- pldm_gettid
- pldm_setnumericsensorenable
- pldm_getsensorreading
- pldm_getsensorthresholds
- pldm_setsensorthresholds
- pldm_restoresensorthresholds
- pldm_getsensorhysteresis
- pldm_setsensorhysteresis
- pldm_getpdrrepositoryinfo
- pldm_getpdr

8.5. Defined Platform Descriptor Records

71 Platform Descriptor Records (PDRs) for A10SA4 rev 26815

- NumericSensorPDR_1
- NumericSensorPDR_2
- NumericSensorPDR_3
- NumericSensorPDR_4
- NumericSensorPDR_5
- NumericSensorPDR_6
- NumericSensorPDR_7
- NumericSensorPDR_8
- NumericSensorPDR_9
- NumericSensorPDR_10
- NumericSensorPDR_11
- NumericSensorPDR_12
- NumericSensorPDR_13

- NumericSensorPDR_14
- NumericSensorPDR_15
- NumericSensorPDR_16
- NumericSensorPDR_17
- NumericSensorPDR_18
- NumericSensorPDR_19
- NumericSensorPDR_20
- NumericSensorPDR_21
- NumericSensorPDR_22
- NumericSensorPDR_23
- NumericSensorInitializationPDR_1
- NumericSensorInitializationPDR_2
- NumericSensorInitializationPDR_3
- NumericSensorInitializationPDR_4
- NumericSensorInitializationPDR_5
- NumericSensorInitializationPDR_6
- NumericSensorInitializationPDR_7
- NumericSensorInitializationPDR_8
- NumericSensorInitializationPDR_9
- NumericSensorInitializationPDR_10
- NumericSensorInitializationPDR_11
- NumericSensorInitializationPDR_12
- NumericSensorInitializationPDR_13
- NumericSensorInitializationPDR_14
- NumericSensorInitializationPDR_15
- NumericSensorInitializationPDR_16
- NumericSensorInitializationPDR_17
- NumericSensorInitializationPDR_18
- NumericSensorInitializationPDR_19
- NumericSensorInitializationPDR_20
- NumericSensorInitializationPDR_21
- NumericSensorInitializationPDR_22
- NumericSensorInitializationPDR_23
- SensorAuxiliaryNamesPDR_1
- SensorAuxiliaryNamesPDR_2
- SensorAuxiliaryNamesPDR_3
- SensorAuxiliaryNamesPDR_4
- SensorAuxiliaryNamesPDR_5

- SensorAuxiliaryNamesPDR_6
- SensorAuxiliaryNamesPDR_7
- SensorAuxiliaryNamesPDR_8
- SensorAuxiliaryNamesPDR_9
- SensorAuxiliaryNamesPDR_10
- SensorAuxiliaryNamesPDR_11
- SensorAuxiliaryNamesPDR_12
- SensorAuxiliaryNamesPDR_13
- SensorAuxiliaryNamesPDR_14
- SensorAuxiliaryNamesPDR_15
- SensorAuxiliaryNamesPDR_16
- SensorAuxiliaryNamesPDR_17
- SensorAuxiliaryNamesPDR_18
- SensorAuxiliaryNamesPDR_19
- SensorAuxiliaryNamesPDR_20
- SensorAuxiliaryNamesPDR_21
- SensorAuxiliaryNamesPDR_22
- SensorAuxiliaryNamesPDR_23
- TerminusLocatorPDR
- FRURecordSetPDR_0

8.6. Sensor and Threshold Information

Refer to *Device Peripheral Table* for a list of the peripherals, currents and voltages that can be monitored through the BMC.

Note: Although the PLDM commands use device IDs based at 1, the *Device Peripheral Table* lists device IDs based at 0[(2)] in the **ID (DEV/PDR)** column. Therefore, when referring to a device ID in the table, you must add 1 to obtain the device ID used by the PLDM commands. For example, the board power ID is listed as 0 in the *Device Peripheral Table*, while PLDM commands use 1.

(2) as shown by the `fpgainfo` command

A. Regulatory Information

Regulatory Model Number: 10AX115

United States Federal Communications Commission (FCC) Class A User Information

The Class A Product: Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept the interference received, including interference that may cause undesired operation.

Attention: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with other instrcutions, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference is at his/her own expense.

Caution: If this device is changed or modified without permission from Intel, the user may void his or her authority to operate the equipment.

VCCI Class A Statement

この装置は、クラスＡ情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。 ＶＣＣＩ－Ａ

BSMI Class A Statement

警告使用者:
此為甲類資訊技術設備，於居住環境中使用時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適當的對策。

Republic of Korea KCC Notice Class A

Canada EMC Compliance Statement

This Class A digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

European Community Manufacturer Declaration

CE

Belgium

Par la présente, Intel Corporation déclare que la carte Intel PAC with Intel Arria 10 GX FPGA est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante: Declaration of Conformity

Denmark

Intel Corporation erklærer hermed, at Intel PAC with Intel Arria 10 GX FPGA overholder direktiverne 2014/30/EU, 2014/35/EU og 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Den fulde tekst for EUs overensstemmelseserklæring findes på engelsk på følgende adresse: Declaration of Conformity

Netherlands

Intel Corporation verklaart hierbij dat Intel PAC with Intel Arria 10 GX FPGA in overeenstemming is met de richtlijnen 2014/30/EU, 2014/35/EU en 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

De volledige Engelse tekst van de EU-conformiteitsverklaring is hier beschikbaar: Declaration of Conformity

Germany

Hiermit erklärt die Intel Corporation, dass die Intel PAC with Intel Arria 10 GX FPGA den Richtlinien 2014/30/EU, 2014/35/EU und 2011/65/EU entspricht.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Die vollständige EU-Konformitätserklärung ist in englischer Sprache unter der folgenden URL einsehbar: Declaration of Conformity

Sweden

Härmed intygar Intel Corporation att Intel PAC with Intel Arria 10 GX FPGA överensstämmer med direktiven 2014/30/EU, 2014/35/EU och 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Den fullständiga engelska texten för EU-överensstämmelsen finns på följande internetadress: Declaration of Conformity

Finland

Intel Corporation vakuuttaa täten, että Intel PAC with Intel Arria 10 GX FPGA on direktiivien 2014/30/EU, 2014/35/EU ja 2011/65/EU määräysten mukainen.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

EU-vaatimustenmukaisuusvakuutuksen koko englanninkielinen teksti on saatavilla osoitteessa: Declaration of Conformity

Ireland

Hereby, Intel Corporation declares that the Intel PAC with Intel Arria 10 GX FPGA is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL: Declaration of Conformity

Portugal

A Intel Corporation declara, por este meio, que a Intel PAC with Intel Arria 10 GX FPGA cumpre as Diretivas 2014/30/UE, 2014/35/UE e 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Pode consultar o texto da declaração de conformidade da UE na íntegra, disponível em inglês através do seguinte URL: Declaration of Conformity

Spain

Por la presente, Intel Corporation declara que Intel PAC with Intel Arria 10 GX FPGA cumple las directivas 2014/30/UE, 2014/35/UE y 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

El texto completo (en inglés) de la declaración de conformidad de la UE está disponible en la siguiente URL: Declaration of Conformity

France

Par la présente, Intel Corporation déclare que la carte Intel PAC with Intel Arria 10 GX FPGA est conforme aux directives 2014/30/UE, 2014/35/UE et 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Le texte intégral en anglais de la déclaration européenne de conformité est disponible à l'adresse suivante: Declaration of Conformity

Italy

Con il presente documento, Intel Corporation dichiara che la scheda di accelerazione programmabile Intel PAC with Intel Arria 10 GX FPGA è conforme alle direttive 2014/30/EU, 2014/35/EU e 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

Il testo completo della dichiarazione di conformità UE in lingua inglese è disponibile al seguente indirizzo: Declaration of Conformity

United Kingdom

Hereby, Intel Corporation declares that the Intel PAC with Intel Arria 10 GX FPGA is in compliance with Directives 2014/30/EU, 2014/35/EU and 2011/65/EU.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

The full text of the EU declaration of conformity is available at the following URL: Declaration of Conformity

Poland

Firma Intel Corporation niniejszym oświadcza, że karta Intel PAC with Intel Arria 10 GX FPGA jest zgodna z dyrektywami 2014/30/UE, 2014/35/UE i 2011/65/UE.

Att. Corp Quality, Intel Deutschland GmbH, Am Campeon 10-12, Neubiberg, 85579 - Germany

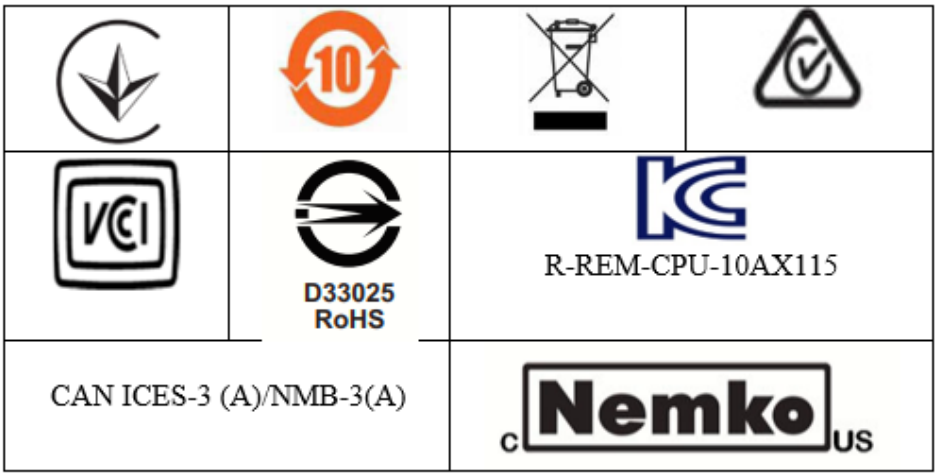
Pełny tekst deklaracji zgodności z wymogami UE w języku angielskim jest dostępny na stronie: Declaration of Conformity

End-of-Life/ Product Recycling

Product recycling and end-of-life take-back systems and requirements vary by country.

Contact the retailer or distributor of this product for information about product recycling and/or take-back.

Regulatory Markings



Hazardous Substances Table

产品中有毒有害物质的名称及含量

部件名称 Component Name	有毒有害物质或元素 Hazardous Substance					
	铅 Pb	汞 Hg	镉 Cd	六价铬 Cr (VI)	多溴联苯 PBB	多溴二苯醚 PBDE
金属部件 Metal Parts	○	○	○	○	○	○
印刷电路板组件 Printed Board Assemblies (PBA)	X	○	○	○	○	○

○：表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572标准规定的限量要求以下。

○: Indicates that this hazardous substance contained in all homogeneous materials of such component is within the limits specified in GB/T 26572.

×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出GB/T 26572标准规定的限量要求。

×: Indicates that the content of such hazardous substance in at least a homogeneous material of such component exceeds the limits specified in GB/T 26572.

对销售之日的所售产品,本表显示我公司供应链的电子信息产品可能包含这些物质。注意：在所售产品中可能会也可能不会含有所有所列的部件。

This table shows where these substances may be found in the supply chain of our electronic information products, as of the date of sale of the enclosed product. Note that some of the component types listed above may or may not be a part of the enclosed product.

除非另外特别的标注,此标志为针对所涉及产品的环保使用期限标志. 某些可更换的零部件可能会有一个不同的环保使用期限(例如,电池单元模块).

此环保使用期限只适用于产品在产品手册中所规定的条件下工作.

The Environment-Friendly Use Period (EFUP) for all enclosed products and their parts are per the symbol shown here, unless otherwise marked. Certain field-replaceable parts may have a different EFUP (for example, battery modules) number. The Environment-Friendly Use Period is valid only when the product is operated under the conditions defined in the product manual.

B. References

Related Information

Intel Arria 10 GX/GT Device Errata and Design Recommendations
This errata sheet provides information about known device issues affecting Intel Arria 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

C. Revision History

Table 12. Revision History for Intel Programmable Acceleration Card (PAC) with Intel Arria 10 GX FPGA Data Sheet

Document Version	Changes
2020.10.26	Added Air Duct Disassembly on page 14
2020.03.06	Sections Updated: • Introduction on page 3 • On-Board Memory on page 6 • Interfaces and Dimensions on page 6 • Control and Support on page 8 • PCIe Overview on page 8 • Board Management Controller Overview on page 9 • System Compatibility on page 10 [Tables Updated] • Thermal Specifications on page 16 [Added links to related documents] • Board Management Controller on page 19 • BMC Voltage and Thermal Handling on page 20 [OPAE link updated] • Updating the BMC Configuration and Firmware on page 22 • Updating the FIM on page 18
2019.05.30	• Updated *Figure: Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*. • Updated *Appendix: Regulatory Information*.
2019.03.26	Updated Views of the Intel PAC with Intel Arria 10 GX FPGA on page 5. Removed reference to ECC from PAC block diagram.
2018.12.04	• Updated for Acceleration Stack version 1.2. Maintains support for Acceleration Stack version 1.1. • Updated BMC version with support for PCIe update • Added *PLDM Commands for the Board Management Controller* chapter • Updated the following sections: — *FPGA Interface Manager* in the *FPGA Interface Manager* chapter — *BMC Voltage and Thermal Handling* in the *Board Management Controller* chapter — *BwMonitor* in the *Board Management Controller* chapter — *Updating the BMC Configuration and Firmware* in the *Board Management Controller* chapter • ECC not supported in on-board memory • Clarified: BMC communication based on PLDM for Platform Monitoring and Control • Terminology correction: previously SDR, now PDR
2018.08.16	Corrected broken link in *FPGA Interface Manager*.
2018.08.06	Updated the following sections: • Introduction • Block Diagram • QSFP+ • System Compatibility • Interfaces and Dimensions Added substantial content to the *Board Management Controller* chapter
2018.04.11	Updated the following sections:

continued...

Document Version	Changes
	• On-Board Memory on page 6 • QSFP+ on page 7 • Power on page 7 • Board Management Controller on page 19 • System Compatibility on page 10 • Mechanical Information • Thermal Specifications on page 16
2018.01.22	Updated the following sections: • Introduction on page 3 • On-Board Memory on page 6 • Interfaces and Dimensions on page 6 • Power on page 7 • CPLD on page 7 • Board Management Controller on page 19 • Mechanical Information • Thermal Test Performance Results on page 16 • Regulatory Information on page 27
2017.11.03	Initial Release