Introduction

The HIP1011 was the first device designed to be fully compatible with the PCI Hot Plug specification. This device facilitates “HOT PLUGGING”, the removal or insertion of PCI compliant cards without the need to power down the server voltage bus. The HIP1011 controls all four (-12V, +12V, +3.3V, +5V) supplies found in PCI applications, monitoring and protecting against over current (OC) and under voltage (UV) conditions. Reference the HIP1011 data sheet (4311) and the PCI Hot Plug specification available from www.pcisig.com.

Figure 2 illustrates the typical implementation of the HIP1011. Additional components for optimizing performance in particular applications, ambient electrical noise levels or desired features will be necessary.

The ease of implementation of the HIP1011 Hot Plug Solution (HIP1011 and as few as 2 N-Channel MOSFETs like the ITF86130 UltraFET) is complemented by the small PCB foot print necessary, since both are available in 0.150 inch SOICs. The typical application requires only 1.1 sq. inches of PCB board space (see Figure 1).

Key Feature Description and Operation

The HIP1011, two power MOSFETs and a few passive components as configured in Figure 2, create a small and simple yet complete power control solution. It provides the maximum specified current for each supply to the PCI adapter slot. Over current monitoring and protection for the 3.3V and 5V supplies is provided by sensing the voltage across external current-sense resistors. For the +12V and -12V inputs, over current protection is provided internally. On-chip references are used to monitor the +5V, +3.3V and +12V outputs for under voltage conditions. During an over current condition on any output, or an under voltage condition on the +5V, +3.3V or +12V outputs, all MOSFETs are immediately latched-off and a LOW (0V) is presented to the FLTN output. During initial power-up of the main V_{CC} supply (+12V), the PWRON input is inhibited from turning on the switches, and the latch is held in the reset state until the V_{CC} input is greater than 10V. If FLTN is latched low