

# HEF4104B-Q100

Quad low-to-high voltage translator with 3-state outputs

Rev. 2 — 14 December 2021

Product data sheet

## 1. General description

The HEF4104B-Q100 is a quad low-to-high voltage translator with complementary 3-state outputs ( $B_n$  and  $\bar{B}_n$ ). A LOW on the output enable input (OE) causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

## 2. Features and benefits

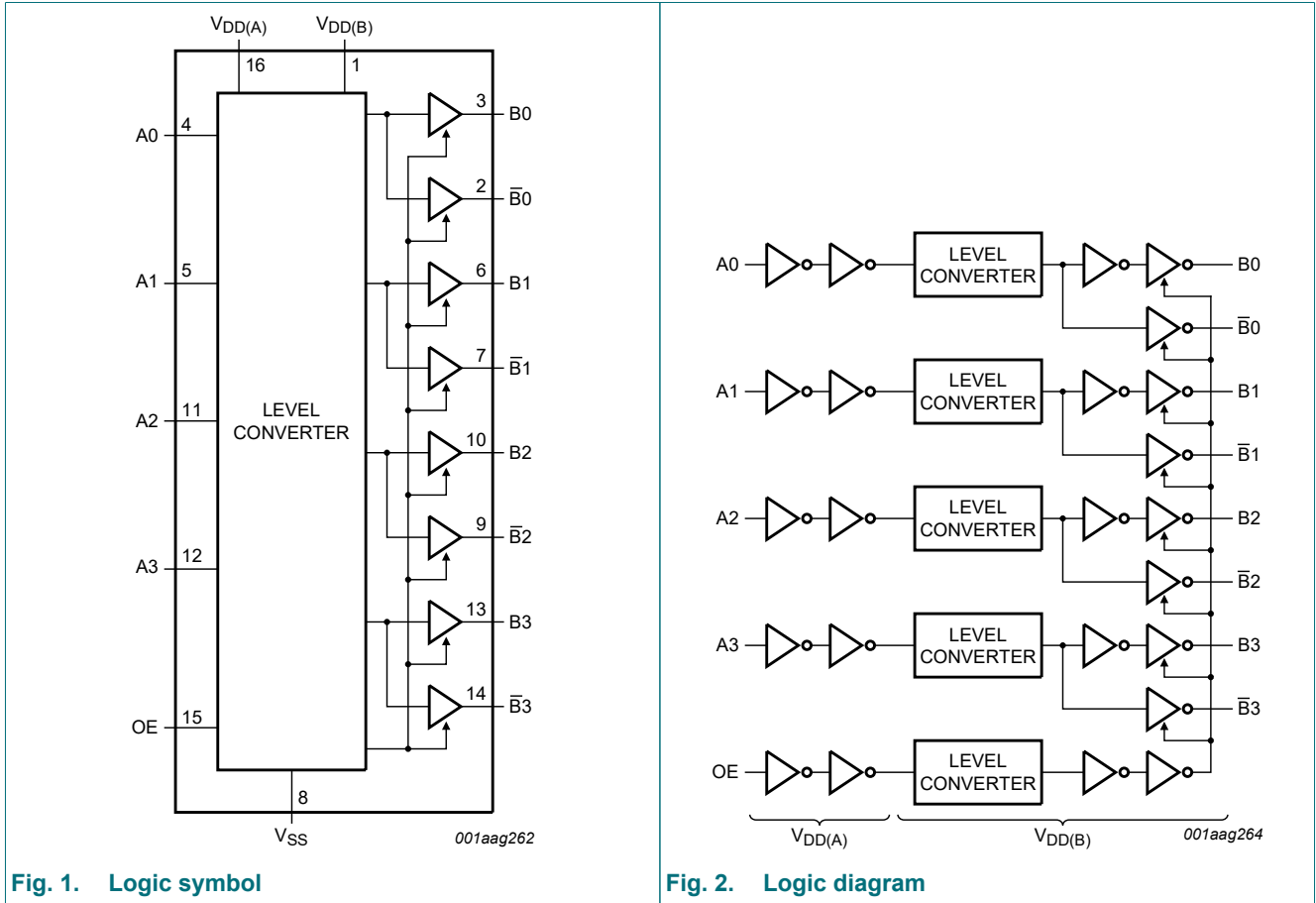
- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )

## 3. Ordering information

Table 1. Ordering information

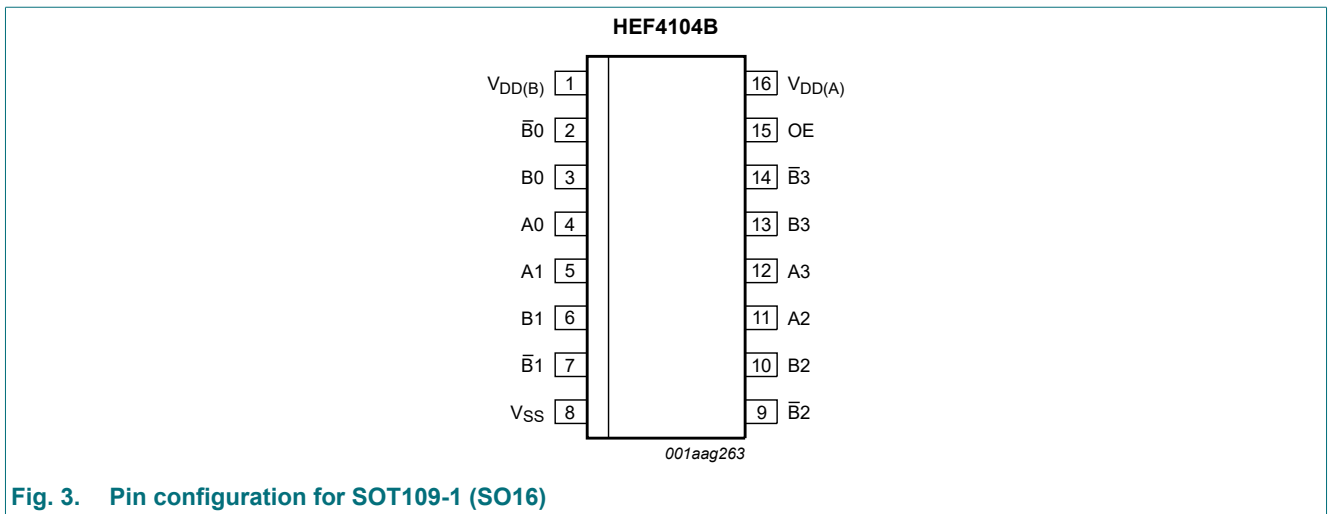
Type number	Package			
	Temperature range	Name	Description	Version
HEF4104BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DD(B)}$	1	supply voltage port B
$\bar{B}0, \bar{B}1, \bar{B}2, \bar{B}3$	2, 7, 9, 14	complementary data output
B0, B1, B2, B3	3, 6, 10, 13	data output
A0, A1, A2, A3	4, 5, 11, 12	data input
$V_{SS}$	8	common negative supply voltage (0 V)
OE	15	output enable input
$V_{DD(A)}$	16	supply voltage port A

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Control	Output	
OE	Bn	$\bar{B}n$
H	An	$\bar{A}n$
L	Z	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to  $V_{SS} = 0$  V (ground).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(A)}$	supply voltage A	port A; $V_{DD(A)} \leq V_{DD(B)}$	-0.5	+18	V
$V_{DD(B)}$	supply voltage B	port B; $V_{DD(B)} \geq V_{DD(A)}$	-0.5	+18	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD(A)} + 0.5$ V	-	$\pm 10$	mA
$V_I$	input voltage		-0.5	$V_{DD(A)} + 0.5$	V
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD(B)} + 0.5$ V	-	$\pm 10$	mA
$I_{I/O}$	input/output current		-	$\pm 10$	mA
$I_{DD}$	supply current	[1]	-	50	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

[1]  $I_{DD}$  is the combined current of  $I_{DD(A)}$  and  $I_{DD(B)}$ .

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD(A)}$	supply voltage A		3	-	$\leq V_{DD(B)}$	V
$V_{DD(B)}$	supply voltage B		$\geq V_{DD(A)}$	-	15	V
$V_I$	input voltage		0	-	$V_{DD(A)}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD(A)} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD(A)} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD(A)} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 9. Static characteristics

Table 6. Static characteristics

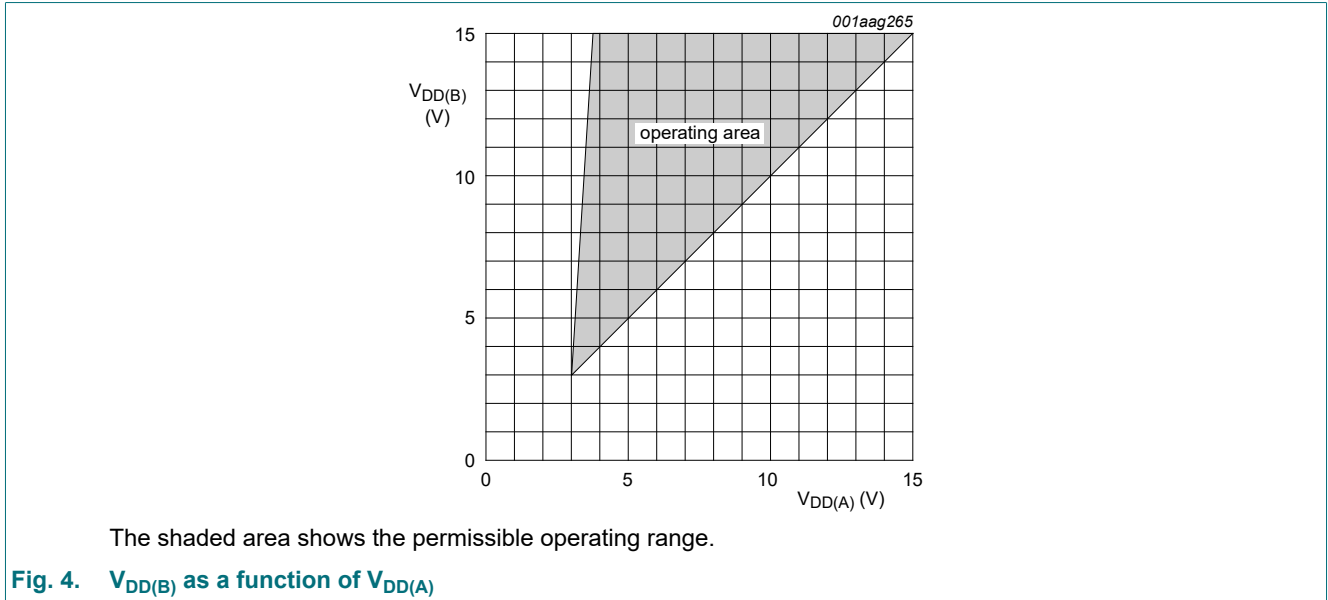
$V_{DD(A)} = V_{DD(B)}$ ;  $V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD(A)}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$ [1]	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	all valid input combinations; $I_O = 0\text{ A}$	5 V [2]	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	HIGH; $V_O = V_{DD(B)}$	15 V	-	1.6	-	1.6	-	12.0	$\mu\text{A}$
		LOW; $V_O = V_{SS}$	15 V	-	-1.6	-	-1.6	-	-12.0	$\mu\text{A}$

Quad low-to-high voltage translator with 3-state outputs

Symbol	Parameter	Conditions	V <sub>DD</sub> [1]	T <sub>amb</sub> = -40 °C		T <sub>amb</sub> = +25 °C		T <sub>amb</sub> = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
C <sub>I</sub>	input capacitance	digital inputs	-	-	-	-	7.5	-	-	pF

- [1] V<sub>DD</sub> is the same as V<sub>DD(A)</sub> and V<sub>DD(B)</sub>.
- [2] I<sub>DD</sub> is the combined current of I<sub>DD(A)</sub> and I<sub>DD(B)</sub>.



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

T<sub>amb</sub> = 25 °C unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	Extrapolation formula[1]	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	An to Bn, $\bar{B}n$ ; see Fig. 5					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V	143 ns + (0.55 ns/pF)C <sub>L</sub>	-	170	340	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V	69 ns + (0.23 ns/pF)C <sub>L</sub>	-	80	160	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V	57 ns + (0.16 ns/pF)C <sub>L</sub>	-	65	135	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	An to Bn, $\bar{B}n$ ; see Fig. 5					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V	143 ns + (0.55 ns/pF)C <sub>L</sub>	-	170	340	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V	69 ns + (0.23 ns/pF)C <sub>L</sub>	-	80	160	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V	62 ns + (0.16 ns/pF)C <sub>L</sub>	-	70	140	ns
t <sub>THL</sub>	HIGH to LOW output transition time	Bn or $\bar{B}n$ ; see Fig. 6					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns
t <sub>TLH</sub>	LOW to HIGH output transition time	Bn or $\bar{B}n$ ; see Fig. 6					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns

## Quad low-to-high voltage translator with 3-state outputs

Symbol	Parameter	Conditions	Extrapolation formula[1]	Min	Typ	Max	Unit
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	OE to Bn, $\bar{B}n$ ; see Fig. 6					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V		-	70	135	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V		-	55	110	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V		-	60	120	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	OE to Bn, $\bar{B}n$ ; see Fig. 6					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V		-	70	135	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V		-	55	105	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V		-	55	110	ns
t <sub>PZH</sub>	OFF-state to HIGH propagation delay	OE to Bn, $\bar{B}n$ ; see Fig. 6					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V		-	195	395	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V		-	95	195	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V		-	80	165	ns
t <sub>PZL</sub>	OFF-state to LOW propagation delay	OE to Bn, $\bar{B}n$ ; see Fig. 6					
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 5 V		-	195	395	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 10 V		-	95	190	ns
		V <sub>DD(A)</sub> = V <sub>DD(B)</sub> = 15 V		-	80	160	ns

[1] Typical value of the propagation delay and output transition time can be calculated with the extrapolation formula ( $C_L$  in pF).

**Table 8. Dynamic power dissipation**

$V_{DD(A)} = V_{DD(B)}$ ;  $V_{SS} = 0$  V;  $t_r = t_f \leq 20$  ns;  $T_{amb} = 25$  °C.

Symbol	Parameter	V <sub>DD</sub> [1]	Typical formula (μW)	where
P <sub>D</sub>	dynamic power dissipation	5 V	$P_D = 3000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f <sub>i</sub> = input frequency in MHz; f <sub>o</sub> = output frequency in MHz; C <sub>L</sub> = output load capacitance in pF; Σ(f <sub>o</sub> × C <sub>L</sub> ) = sum of the outputs; V <sub>DD</sub> = supply voltage in V.
		10 V	$P_D = 12200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 31000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

[1] V<sub>DD</sub> is the same as V<sub>DD(A)</sub> and V<sub>DD(B)</sub>.

10.1. Waveforms and test circuit

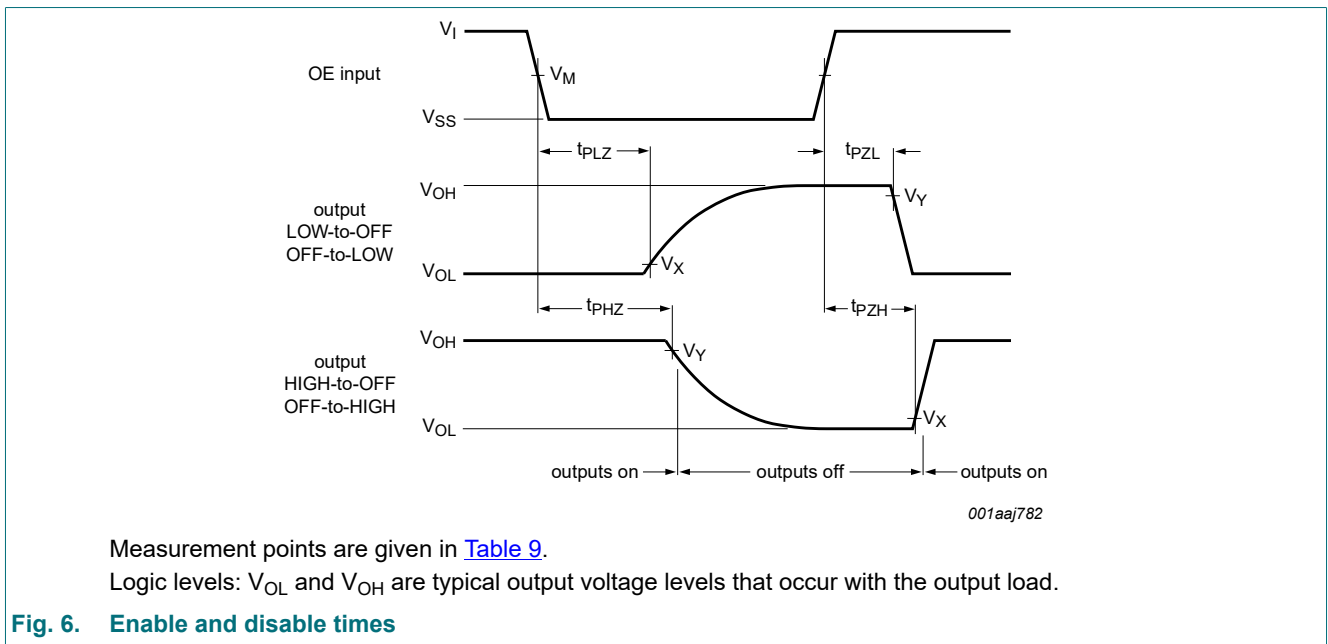
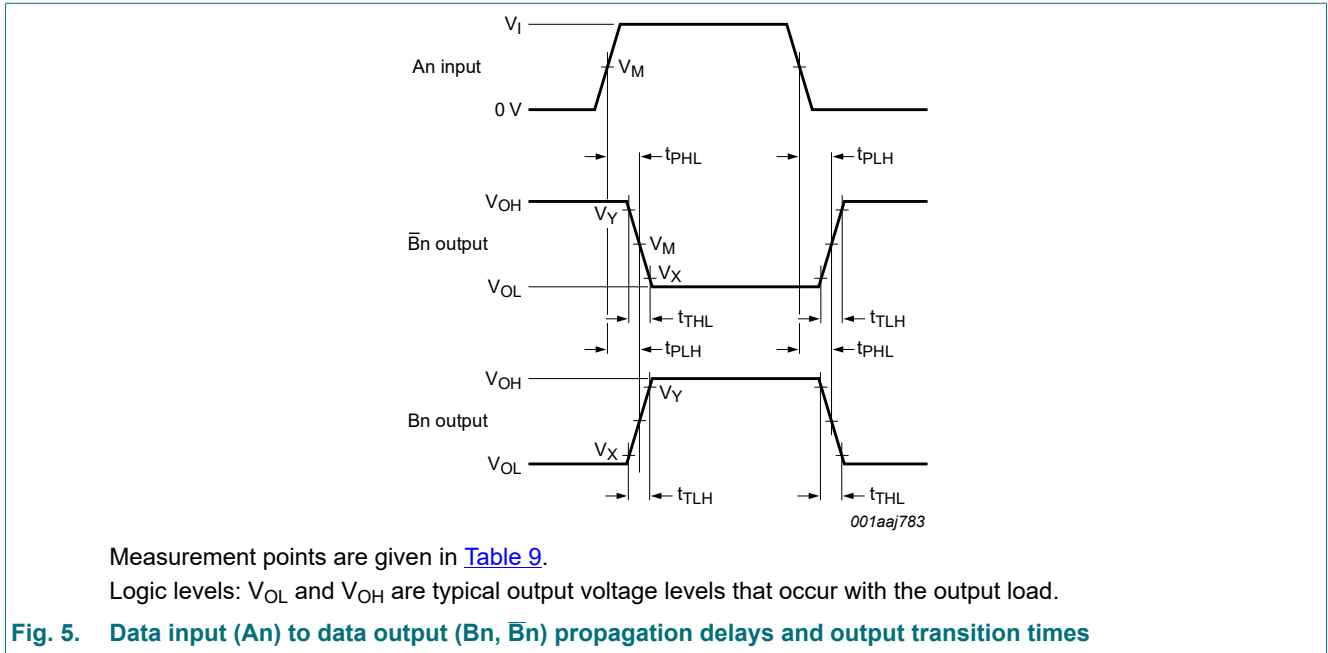
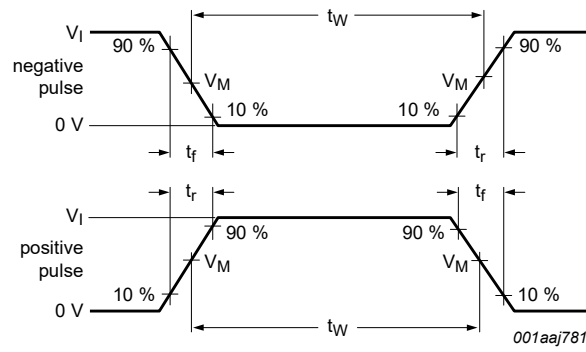


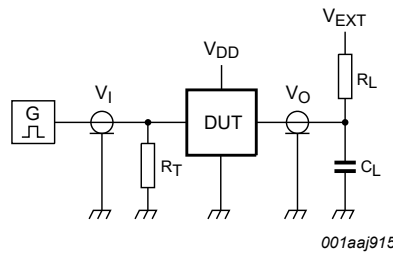
Table 9. Measurement points

Input		Output		
$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
$V_{SS}$ or $V_{DD(A)}$	$0.5V_{DD(A)}$	$0.5V_{DD(B)}$	$0.1V_{DD(B)}$	$0.9V_{DD(B)}$

Quad low-to-high voltage translator with 3-state outputs



a. Input waveforms



b. Test circuit

Test data given in [Table 10](#).

Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance

$R_L$  = Load resistance

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Supplies	Input	Load		$V_{EXT}$		
$V_{DD(A)} = V_{DD(B)}$	$t_r, t_f$	$R_L$	$C_L$	$t_{PHL}, t_{PLH}$	$t_{PZL}, t_{PLZ}$	$t_{PZH}, t_{PHZ}$
5 V to 15 V	$\leq 20$ ns	1 k $\Omega$	50 pF	open	$V_{DD(B)}$	$V_{SS}$



### 11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig. 8. Package outline SOT109-1 (SO16)

## 12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model

## 13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4104B_Q100 v.2	20211214	Product data sheet	-	HEF4104B_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 12</a> added.</li> </ul>			
HEF4104B_Q100 v.1	20140324	Product data sheet	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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