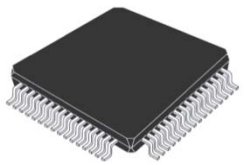
L99UDL01

Automotive universal door lock IC

Data brief



TQFP64L 10x10

Features

- AEC-Q100 qualified
- Six integrated fully protected 0.09 Ω half-bridges
- Integrated half-bridges can be fully independent or paralleled up to three in parallel
- Two levels of Standby
  - Standby (SPI initiated)
  - Sleep (VDD=0 V)
- Very low current consumption in standby
  - Only wake-up circuit active
- High level of Programmability
  - On-time duration
  - Direction
  - Current level
  - Off-state fault detection
- 2 external half bridge controllers (using external N-channel MOSFETs or Smart Power devices)
- External Half bridges protected by drain source monitoring and off-state fault detection
- 2 stage charge pump for low voltage operation
- PWM current regulation up to 25 kHz
- 4 MHz 24 bit SPI interface for control and diagnostics
- Output enable for high security
- High Level Diagnostics
- 10 bit digital current feedback (via SPI) for load integrity check
- Thermal Warning and Shutdown protection
- Reverse battery protection using an external N-Ch MOSFET.
- TQFP64L exposed pad package

Applications

The L99UDL01 is designed for use in a central door lock system driving all of the door lock actuators.This device is able to adapt to most central door lock configurations.

Description

The L99UDL01 is a multiple half-bridge IC with 6 integrated outputs that are PWM configurable and current regulated and up to two externally configured half bridges for higher current nodes. The level of diagnostics includes open load, short to battery, short to ground, and load integrity via 10 bits current feedback.

The L99UDL01 is commanded entirely by SPI using duration and current level commands.

Table 1. Device summary

Package	Order Codes	
	Tray	Tape and Reel
TQFP64L	L99UDL01	L99UDL01TR

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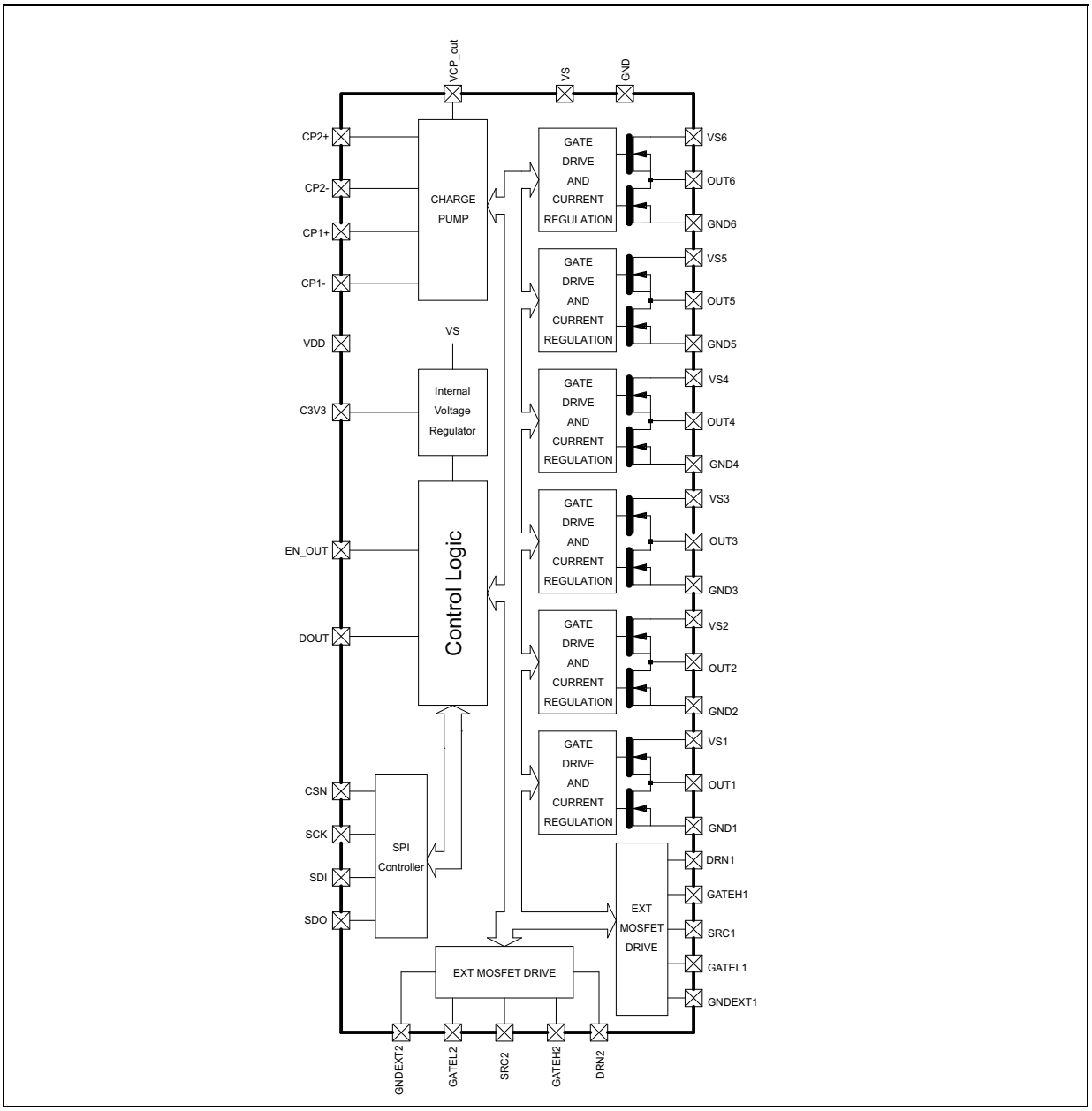
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Table 2. Pin description

Pin #	Name	Description
1	VS1_2	Supply for half bridge 1
2	OUT1_1	Half bridge output 1
3	OUT1_2	Half bridge output 1
4	GND1_1	Ground for half bridge 1
5	GND1_2	Ground for half bridge 1
6	VS2_1	Supply for half bridge 2
7	VS2_2	Supply for half bridge 2
8	OUT2_1	Half bridge output 2
9	OUT2_2	Half bridge output 2
10	GND2_1	Ground for half bridge 2
11	GND2_2	Ground for half bridge 2
12	VS3_1	Supply for half bridge 3
13	VS3_2	Supply for half bridge 3
14	OUT3_1	Half bridge output 3
15	OUT3_2	Half bridge output 3
16	GND3_1	Ground for half bridge 3
17	GND3_2	Ground for half bridge 3
18	EN_OUT	Failsafe logic input. On its rising edge, EN_OUT activates outputs including External MOSFET drivers. Low disables all actuations.
19	DOUT	Programmable I/O pin / Default as Global Fault Flag
20	GNDEXT1	Ground for VDS reference for low side MOSFET
21	GATEL1	Gate drive for low side external MOSFET
22	SRC1	Source – Drain node between high and low side MOSFETS. Used for VDS detection of both high and low side MOSFETs
23	GATEH1	Gate drive for high side external MOSFET
24	DRN1	Drain connection for external H-Bridge, Sensing for VDS fault
25	GNDEXT2	Ground for VDS reference for low side MOSFET
26	GATEL2	Gate drive for low side external MOSFET
27	SRC2	Programmable I/O pin / Optional Source – Drain node between high and low side auxiliary MOSFETS. Used for VDS detection of both high and low side MOSFETs
28	GATEH2	Programmable I/O pin / optional external gate drive for auxiliary high side MOSFET
29	DRN2	Drain connection for external H-Bridge, Sensing for VDS fault
30	GND	Ground pin
31	NC	Not Connected pin; to leave floating

Table 2. Pin description (continued)

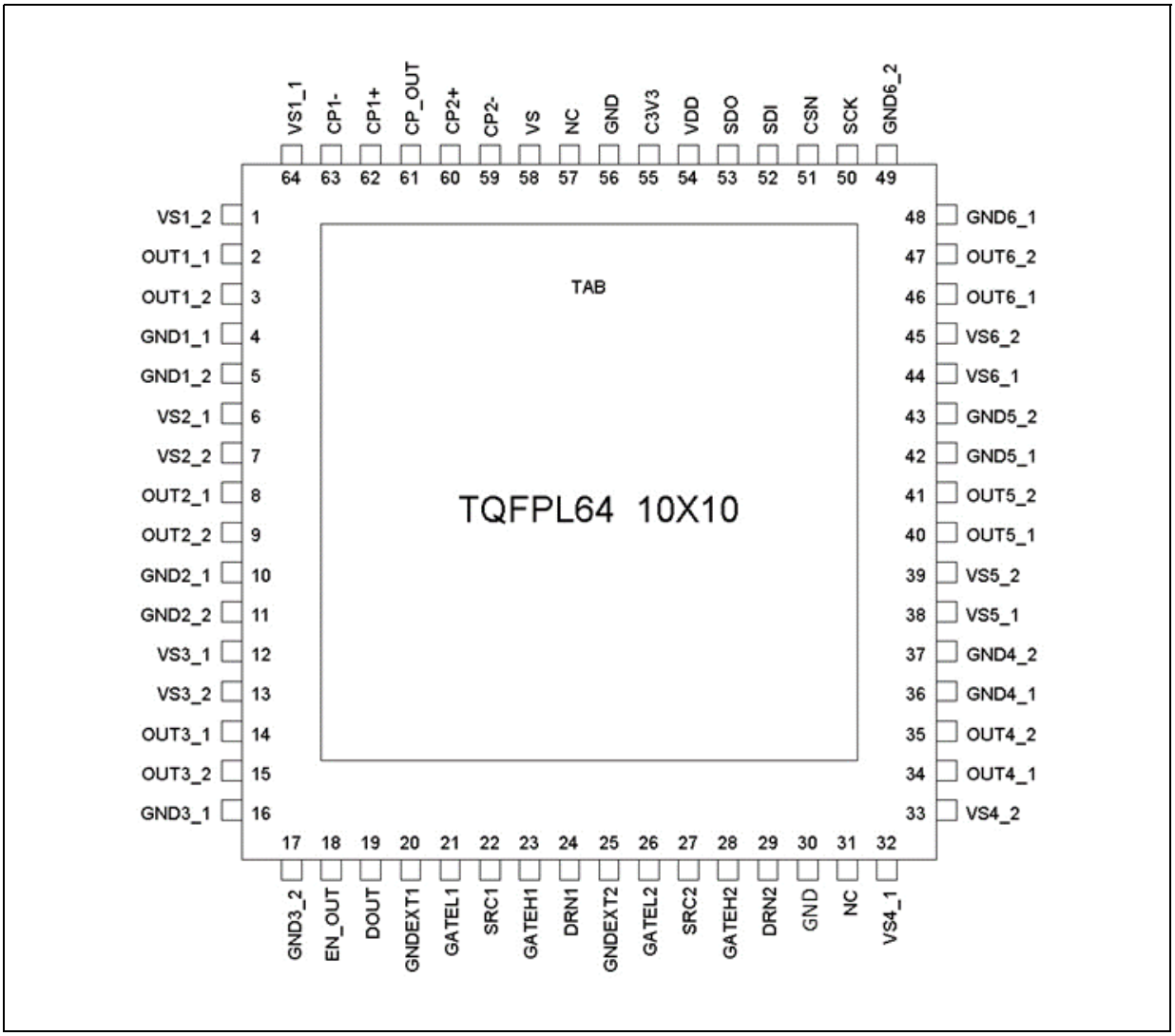
Pin #	Name	Description
32	VS4_1	Supply for half bridge 4
33	VS4_2	Supply for half bridge 4
34	OUT4_1	Half bridge output 4
35	OUT4_2	Half bridge output 4
36	GND4_1	Ground for half bridge 4
37	GND4_2	Ground for half bridge 4
38	VS5_1	Supply for half bridge 5
39	VS5_2	Supply for half bridge 5
40	OUT5_1	Half bridge output 5
41	OUT5_2	Half bridge output 5
42	GND5_1	Ground for half bridge 5
43	GND5_2	Ground for half bridge 5
44	VS6_1	Supply for half bridge 6
45	VS6_2	Supply for half bridge 6
46	OUT6_1	Half bridge output 6
47	OUT6_2	Half bridge output 6
48	GND6_1	Ground for half bridge 6
49	GND6_2	Ground for half bridge 6
50	SCK	SPI Clock - This SCK provides the clock of the SPI. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK) into the internal shift registers while on the falling edge data from the internal shift registers are shifted out to Serial Data Out (SDO).
51	CSN	SPI Chip Select Not -The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low. The Serial Data Out (SDO) is in high impedance when CSN is high or a communication timeout was detected
52	SDI	Serial Data In - This input is used to transfer data serially into the device. Data is latched on the rising edge of Serial Clock (SCK).
53	SDO	Serial Data Out - This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).
54	VDD	I/O Supply (+5 V or 3.3 V)
55	C3V3	Capacitor decoupling pin for internal 3.3 V regulator
56	GND	Ground for IC and I/O
57	NC	Not Connected pin; to leave floating
58	VS	Supply for IC
59	CP2-	Charge pump capacitor pin

Table 2. Pin description (continued)

Pin #	Name	Description
60	CP2+	Charge pump capacitor pin
61	CP_OUT	Charge pump out, also used for biasing reverse battery MOSFET
62	CP1+	Charge pump capacitor pin
63	CP1-	Charge pump capacitor pin
64	VS1_1	Supply for half bridge 1
TAB		Connect to ground

1.3 Pin connections (top view)

Figure 2. Pin connection diagram



2 Device description

2.1 Overview

The L99UDL01 is a 6+2 channel half bridge driver monolithic integrated circuit designed to power a centralized door lock system. This device is made possible by the incorporation of current regulated drivers limiting the current in the door lock motors to a preset level (for example the current levels seen at a 9 V battery).

The current is regulated by PWMming the door lock actuators at a programmed frequency and duty cycle.

2.2 Supply monitoring

2.2.1 Low Voltage Inhibit (VS_{LVI})

The Vs supply has a low voltage warning function with hysteresis. When Vs drops below VS_{LVI_F} the outputs (internal half bridges and drivers for external MOSFET) are disabled and the VS_{LVI} bit is set in the SPI diagnostic register.

Once Vs rises above the rising VS_{LVI_R} threshold the outputs are re-enabled and ready for use. Actuation can be restarted via SPI frame or EN_OUT rising edge according to configuration registers. The VS_{LVI} bit remains set in the SPI diagnostic register and is cleared only upon read & clear.

2.2.2 Overvoltage (VS_{OVSD})

When VS rises above VS_{OVSD} the outputs (internal half bridges and drivers for external MOSFETs) are disabled and the V_{OVSD} bit is set in the SPI diagnostic register.

Once VS falls below VS_{OVSD} the outputs are re-enabled and ready for use. Actuation can be restarted according to configuration registers via SPI frame or EN_OUT rising edge or by setting the EN_ON bit. The VSOVSD bit (diagnostic register 02H) remains set until read & clear SPI frame.

2.2.3 VDD Monitoring

The VDD pin (5V/3.3V) is a supply pin for the L99UDL01 I/O. This pin is monitored by 2 under voltage conditions. In case of an undervoltage condition during operational mode (VDD < VDDUV) the device will enter into stand-by mode and all of the control registers will be reset to their default values after tVDDUV. In case of an undervoltage condition (VDD<VDDSLEEP), the device enters into the ultra-low quiescent sleep mode and the internal regulator is disabled.

Upon rising out of VDD_{SLEEP} the device will perform a power-on reset and enter into Standby mode until a CSN wake-up has occurred. The reset (RSTB) bit will remain set until the first SPI communication.

2.2.4 3V3 Monitoring

The internal 3.3 V regulator, 3V3, is monitored for under voltage conditions to ensure the logic integrity. The 3V3 supply has a low voltage warning function with hysteresis. When the

3V3 regulator drops below $3V3_{UV}$ threshold the outputs (internal half bridges and drivers for external MOSFET) are disabled and the V3V3IUV bit is set in the SPI diagnostic register 13h.

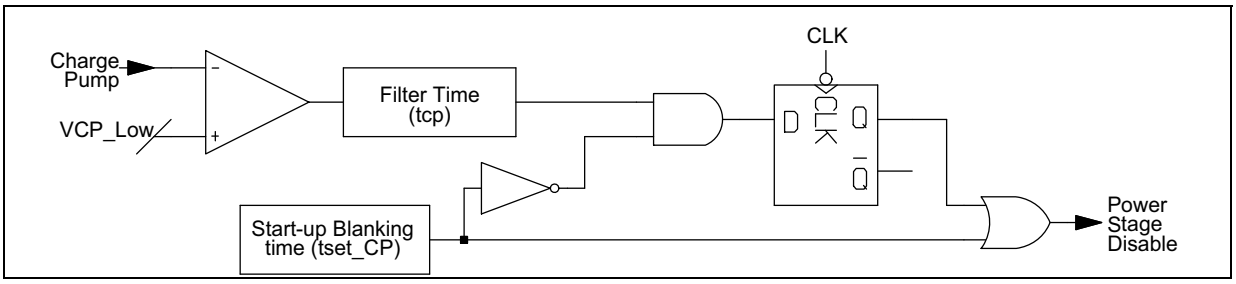
If, for any reason the 3V3 supply falls below $3V3_{RST}$ for t_{3V3UV}, the Logic State machine and all of the registers are RESET to their default state and held there.

Upon rising out of $3V3_{RST}$ RESET will be disabled and the L99UDL01 will enter Standby mode.

2.3 Charge pump

The charge pump uses two external capacitors, which are switched with f_{CP}. The output of the charge pump has a current limitation. In standby mode or after a global thermal shutdown has been triggered the charge pump is disabled.

Figure 3. Charge pump low filtering and start-up



At coming out of standby the outputs are enable t_{set_CP} seconds after the charge pump voltage crosses the VCPLOW threshold. The CPLOW bit will remain set indicating that the charge pump was low since the last reading of the register.

At any time the charge pump output voltage drops below VCPLOW and remains there for longer than t_{CP}, the internal half bridges and the H-Bridge MOSFET gate drivers are pulled low, switching off the external MOSFETs, and CPLOW bit is set.

The outputs are enabled as soon as the charge pump voltage exceeds the VCPLOW threshold for greater than t_{CP}. Actuation can be restarted via SPI frame or EN_OUT rising edge according to configuration registers. Outputs that are actuated by the output override (OUTx_on) bits will automatically turn back on when the charge pump is above CPLOW for greater than t_{CP}.

The CPLOW bit will remain set indicating that the charge pump was low since the last read & clear of the register.

In case of reaching the over-voltage shutdown threshold, VS_{OVSD}, the charge pump is disabled and automatically restarted after VS recovered to normal operating voltage.

The charge pump frequency can be dithered to reduce the impact on radio frequency emissions. This option is set via bit DITHN in register 03H. By default DITHN=0 and dithering is enabled.

2.4 Output functionality

There are two groups of three drivers each. The three drivers in each group can be paralleled or driven independently.

The output configuration registers allow to identify which are the grouped outputs.

The output configuration registers also provide a range of current regulation levels and on-time durations.

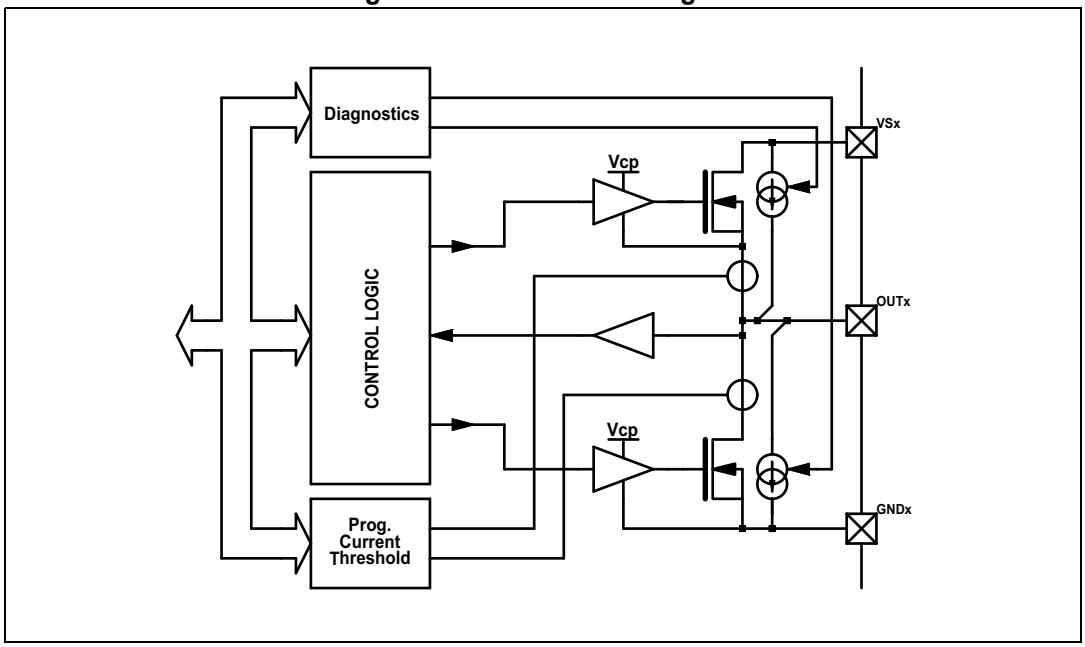
The command to actuate an output has three components (after the parallel links and current regulation levels have been programmed) that comprise an actuation command. These are direction (HS/LS), on-time and braking duration (ex. 300 ms on-time, 100 ms braking time) and which side (HS/LS) is providing the current regulation. The unregulated side is protected by the overcurrent protection.

All outputs, internal and external, are driven with active circuitry. Once an actuation cycle is completed and all devices have been commanded off, the active circuitry is disabled after ~10 µs to reduce quiescent loading. All outputs are then in a passive off state that will keep the outputs off (gates tied to their sources) in the face of noise on the load or supply.

2.4.1 Integrated Half Bridge Drivers (OUT1-OUT6)

Three outputs are configured as switching drivers incorporating active recirculation to minimize power dissipation. The dead time between high and low side drivers is fixed within the functionality of the output drivers.

Figure 4. OUT1-6 Block diagram



All integrated outputs can be driven in timed voltage control (PWM duty cycle), timed current regulation control or on/off control.

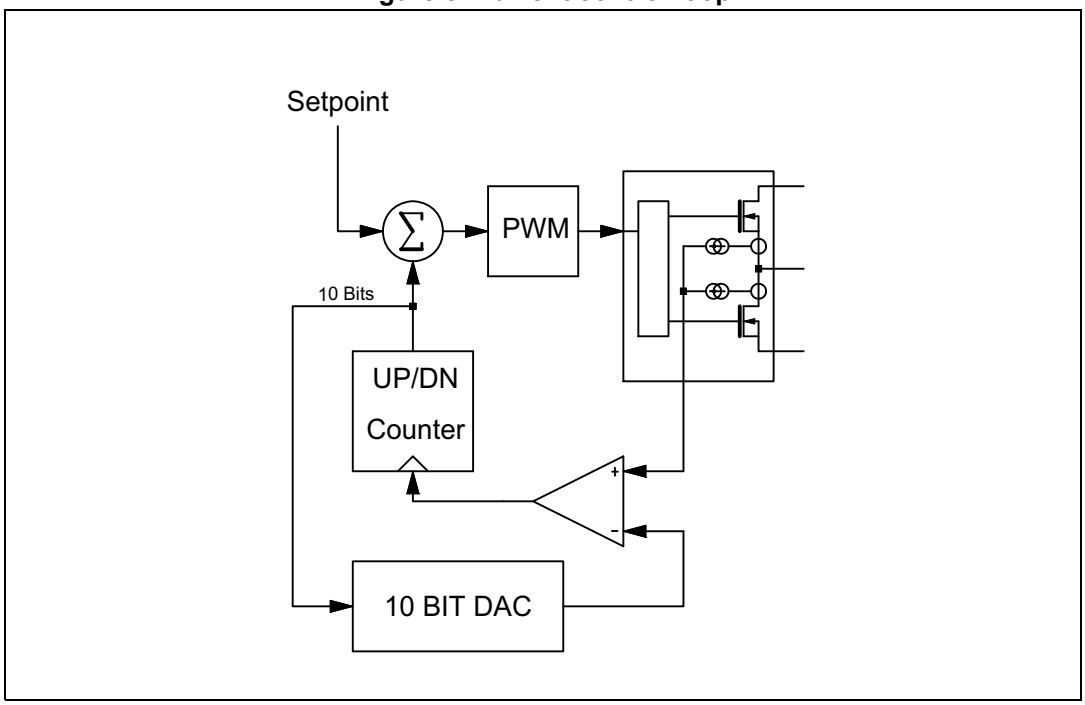
These outputs have over current protection, under current detection, and off-state diagnostics. Off state diagnostics may provide for non-active detection of Lock motor status.

The output rise and fall times are controlled to provide the lowest EMI while minimizing the switching losses. This is done by controlling the edges to smooth out the corners of the waveform while maintaining a fast transition from one level to the other.

2.4.2 Current regulation control

All integrated outputs can work in current regulation mode. Each power MOS has a configurable bidirectional current sense which provides an image of the load current during on mode and recirculation phase. This current image is compared to the target value written in the configuration register in a digital algorithm so that the mean current value through the load is equal to the chosen value.

Figure 5. Current control loop



The control loop for the current regulation is programmable. There are two parameters that are adjustable through SPI. It should be noted that there is a default setting that will work for the most of the lock motor applications known. These parameters are provided to aid in any possible scenario. Typically, these parameters can be left alone:

- Integral Gain, Ki, (3 bits)
- Proportional Gain, Kp, (3 bits)

Integral and proportional gain settings are the standard control loop parameters for integral gain and proportional gain. The default settings for these parameters are Ki =2^{-2} = 1/4, and Kp = 2^{6} = 64.

This register is set up for a nominal control loop. Most, if not all, applications will be stable enough to use this default setting.

Current regulation mode can be initiated via EN_OUT rising edge or via OUT_ON bit (register 01H) provided EN_OUT=1 and OUTx_on =0 for the timed output x. Once started, a timed actuation can be stopped only with EN_OUT=0, fault condition, Emergency mode or at the natural end of timers. No other time controlled output can be started when a timed actuation is ongoing.

2.4.3 Current feedback

The Integrated drivers can provide a 10 bits word representing the current regulation loop current value. This is done to provide load integrity information in addition to the CNR bit (a current not reached, CNR, bit is set if the current in the output does not reach the regulated current level during the entire on-time actuation).

This is a buffered value of the 10 bits up/down counter in the current regulation loop. This information is retrieved at the falling edge of CSN when accessing the appropriate current loop register.

The conversion of the 10 bits information found in registers 13h – 18h to a typical value of current is a simple equation:

$$\text{Typical Current} = \frac{\text{Regx}}{\text{0A0h}}$$

2.4.4 PWM frequency adjustment

The current regulation or PWM control PWM frequency can be adjusted to optimize the motor current regulation. This is accomplished in 2 kHz intervals from 10 kHz to 24 kHz using three FPWMx bits in register 00H.

2.4.5 External FET Controllers

The external FET controllers are designed to be drivers for MOSFETS configured as half bridges. These outputs are not intended to be PWMmed and are limited in their switching speed to aid in reducing EMC issues.

The external MOSFETS are protected by a programmable drain to source voltage (V_{DS}) monitor. Both the voltage threshold and reaction delay are programmable. The default setting is 1V for 1µs.

In the event of a Drain-Source fault the appropriate fault bit will be set as well as a fault bit in the Global Status Byte. A faulted driver will be switched off and is enabled again only after clearing fault bit (register 11H).

Since these outputs are not intended to be PWMmed there is no active recirculation option.

The external MOSFET control has off-state diagnostic capability as well.

The external MOSFETs can be driven in timed on/off control or purely on/off control.

2.4.6 External MOSFET Dead Time Control

At the end of every timed actuation all outputs are pulled to ground for the off-time duration as determined in the control register 02H. This requires that the external H-Bridge controller has a dead time between when the high side MOSFET is commanded off and when the low side MOSFET is commanded on. This is a fixed value set to t_{DT} (6 ms).

2.4.7 DOUT

The Data OUT pin provides the host processor with a real time fault indication. The Global Fault bit may be reflected on this pin.

2.4.8 EN_OUT

The output Enable pin has three states: It enables the output functionality while held high, and disables the outputs when held low. This pin can also be used to initiate an output actuation, based on programmed parameters, on a rising edge. There is a filter time on the rising edge of EN_OUT of t_{EN}. This is used to prevent noise from accidentally actuating a timed actuation.

2.4.9 Paralleling Outputs

Up to three the integrated outputs can be paralleled in two groups for the purpose of sharing higher current loads.

Some of the possible combinations:

- 2 groups of 3
- 2 groups of 2 and 2 single outputs
- 1 group of 2, 1 group of 3 and a single output
- 1 group of 3, and 3 single outputs
- 1 group of 2, and 4 single outputs
- 6 single outputs, no groups

Paralleled outputs have all of their current regulation, protection, and diagnostic information tied together. Once a set of outputs has been grouped the master registers are used to command and diagnose that group. The master registers are output 1 for outputs 1 through 3 and output 4 for outputs 4 through 6.

When paralleling multiple half bridges all the channels in the group will provide the current monitoring for the master current regulation loop.

Current values programmed for each channel in the group are added to create the total current for the group. Each output can have different values (for ex; 1 A for ch1 and 1.2 A for ch2 to generate 2.2 A total current regulation for the group). The Slave outputs must be programmed as current regulating when using current regulation.

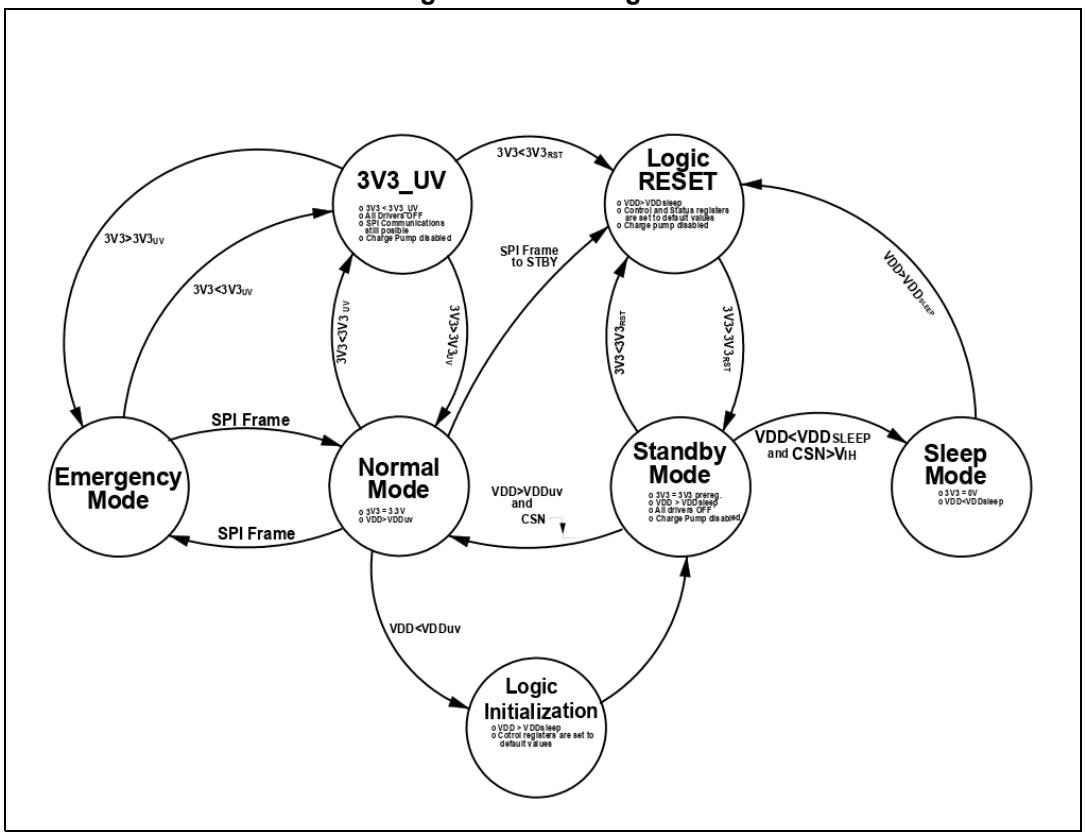
PWM values will be taken from the master registers only. The remaining slave registers will be ignored when in PWM mode. The Slave outputs must be programmed as PWM when using PWM mode.

All diagnostics in a group must be cleared prior to restarting that group**.**

2.5 Operating modes

We can distinguish between 4 different operating modes: Normal mode, Standby mode, Sleep mode and Emergency override mode. The L99UDL01 powers up in Standby mode by default.

Figure 6. State diagram



In Sleep mode no active circuitry is supplied. In standby mode logic is initialized but not operational. There is no function present in either modes in order to minimize the current consumption. Only wake-up circuitry is active in Standby mode.

2.5.1 Sleep mode

In sleep mode all circuitry is disabled. There is no charge pump or internal voltages. This is the lowest quiescent current mode.

Sleep mode is entered when the VDD input falls below VDD_{SLEEP}. Prior to entering sleep mode all registers are reset to their default values. Sleep mode is exited when VDD rises above VDD_{SLEEP}. Sleep mode only exits into Standby mode.

2.5.2 Standby mode

Standby mode has only the 3V3 pre-regulator active for purposes of watching for wake-up. The charge pump is off and the outputs are disabled.

Standby is entered, from operational mode, when the device is commanded by SPI message (it requires two bits set in two different registers) or by VDD falling below VDD_{UV}. To attain the low quiescent state in Standby the EN_OUT pin must be held low.

Standby cannot be entered while in timed actuation or when any output is active. This operation is not supported.

Standby is entered from sleep mode when VDD rises above VDD_{SLEEP} as long as V3V3 > $V3V3_{RST}$. Other than Emergency override mode Standby is the only mode that Normal operation can be entered.

2.5.3 Normal mode

The L99UDL01 exits Standby mode and enters Normal mode when the CSN pin is pulled down meanwhile VDD is higher than VDD_{SLEEP} and V3V3 is higher $V3V3_{RST}$.

This delay has to do with the charge pump and 3V3 regulator stabilization. When these voltages have reached their proper levels, the SDO pin is pulled low from a tri-stated condition. At that point, logic is operating, all circuits are activated and the SPI controller can be used to update the register configuration.

When coming out from Standby, the configuration registers are set to their default values. In this startup phase, the Charge Pump circuit starts to work. When the charge pump rises above the CPLOW threshold actuation can be initiated via EN_OUT pin or via an appropriate SPI frame. The CPLOW bit is not cleared until the register is read and cleared.

2.5.4 Emergency override mode

Emergency override mode is a crash override mechanism that will interrupt any current actuation command in progress and drives outputs according to the programmed values in the command and configuration registers.

This mode also overrides all protections. In an Emergency override mode the device will not latch off if an overcurrent threshold is exceeded. Instead of latching off the driver and reporting a fault the output will continue to retry as in normal current regulation mode.

All faults will be reported while not acted upon.

Emergency override mode is initiated when a (1, 0) is entered in the EMCY bits (register 01H). All other bit configurations result in normal operation.

When emergency override is enabled all current actuation activity will stop. To initiate a new actuation routine the OUT_ON bit must be set or the EN_OUT pin must be toggled.

2.6 Diagnostics and protections

2.6.1 Shorted load detection

All integrated drivers are protected for shorts to ground or supply by a simple over current detection and latch off strategy. At turn on there is a blanking time ($t_{OC\_BLANKING}$) where the output is given time to turn on. After the blanking time if the output current exceeds (I_{OC}) for longer than the filter time the faulted output(s) will be latched off.

If a shorted condition occurs after an output is active only the filtering time applies to the latch-off action.

The fault will be reported in the fault register (register 10H). The Global fault Functional Error 1 bit (FE1) will also be set.

I_{OC} applies to a single output. Multiple outputs in parallel will multiply the I_{OC} value accordingly. Two outputs in parallel will garner a 2x increase in the I_{OC} value. The same concept applies to have three outputs in parallel.

Since this system relies on current limitation for normal running I_{OC} can occur in one of two ways. First, the I_{OC} threshold can occur if the current rise time is faster than the minimum on time ($t_{OC\_BLANKING}$) of the driver. This occurs when a shorted load has very little inductance.

The second method is when the integrated driver is programmed as a simple switch and does not provide the current regulation. Then I_{OC} is the only means of overcurrent protection.

The external half bridges are used as a simple switch (not current regulated). However, when both sides of the H-Bridge are set up by the use of integrated half bridges (outputs 1-6) then one of the integrated half bridges should be programmed as a simple switch. This is done by programming the output to be Voltage controlled (by setting the PWM_SW_x bit to 1) and setting the duty cycle to 100%.

This allows the other half bridge to provide the lock motor current regulation without confusion.

In the case of the external half bridges Drain-Source voltage detection is implemented as an overload protection once the driver is active. The Drain-Source threshold, V_{DS}, and duration, t_{VDS_BLANK}, are both programmable with a wide range to select.

Shorted outputs may be detected in the off-state as well (see *Section 2.6.3*).

2.6.2 Thermal protection

There is a thermal sensor associated with each pair of drivers. There are two reported thermal thresholds. These are thermal warning T_{Wx} and thermal shutdown T_{SDx}.

Thermal warning only provides a SPI register indication of the condition (T_{Wx}). Thermal shutdown either shuts down the offending half bridge or disables the entire device. This option is programmable via SPI command. Thermal shutdown is indicated in the SPI register via the T_{SDx} bits.

In the case where more than one driver is linked in parallel the hottest driver will cause a thermal indication (T_{Wx} or T_{SDx}). All linked drivers have their diagnostic bits linked as well. That is, they will all demonstrate the same diagnostic state.

Drivers cannot be activated until its corresponding temperature is below thermal shutdown threshold and corresponding fault register bit is cleared.

2.6.3 Off-state load detection

Along with the standard shorted load and thermal protections the L99UDL01 has the ability to verify load integrity without actuating loads.

This is done by incorporating enable-able weak pull-up (ODCHx) / pull-down (ODCLx) currents at each output. By using the weak pull-up/pull-down currents the following conditions can be determined:

- Shorted output to either ground or supply
- Open load

One method would be first to bias a motor node by either a weak pull-up or weak pull-down current then reading the Dynamic Output State (DOSx, DOS_EXTx) bits. A weak pull-up on one output should cause all nodes associated with that output to pull high. A weak pull-down on one output should cause all nodes associated with that output to pull low. An open circuit or shorted output would prevent either one or the other from happening.

2.6.4 Enable-able Weak Pull-up/down currents

The weak pull-up/pull-down currents are enable-able through SPI command (register 07H). Each output can have enabled a weak pull up current or a weak pull down current individually.

Activating a weak pull-up on one of a paralleled output and a weak pull-down in another of the same parallel group will be ignored and set a WRT_fail bit. Alternatively, activating a weak pull-up and a weak pull-down on the same output will be ignored and set a WRT_fail bit.

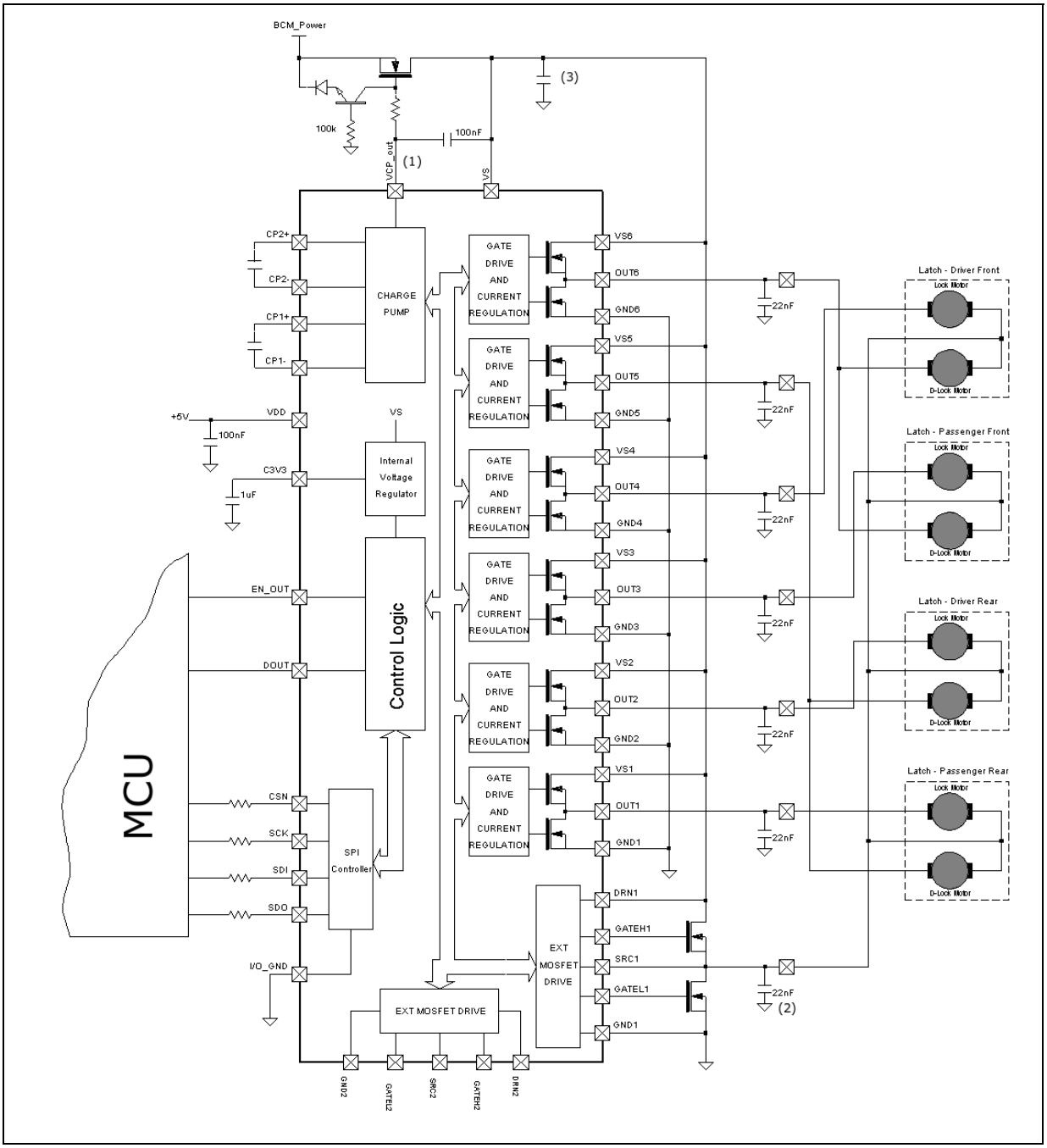
Weak pull-up/pull-down currents are available for both the integrated and the external Half-bridge controllers. This allows the user to determine if there is a short to ground or supply condition on these outputs prior to actuate.

2.6.5 Dynamic output state detection

All outputs, internal and external have the ability to detect if the output voltage is above or below a specific threshold (V_{OUT_th}). If the Output voltage at the time CSN falls is above the threshold the corresponding bit in Diagnostic register 11H is set high. If the output voltage is below the threshold then the corresponding bit is set low.

3 Application schematic

Figure 7. Typical application diagram example



(1) Recommended VCP_out capacitors for optimum EMC performance. These capacitors need to be placed as close to the VS-VCP pins as possible to optimize their effectiveness at reducing EMC.
(2) A 22nF capacitor should be used on each output for ESD performance and output stability.
(3) The Bulk capacitance should be dimensioned according to the user's design practices.

4 Electrical characteristics

4.1 Absolute maximum ratings

The absolute maximum ratings are the values at which if exceeded the device may become damaged.

Table 3. Absolute maximum ratings

PIN/Parameter Name	Parameter	Value		Unit
		Min	Max	
VS_X	Supply Voltage (Continuous)	-0.3	+28	V
VS_X	Supply Voltage 400 ms transient (Load Dump)	-0.3	+40	V
VCP_OUT	Charge pump output voltage	-0.3 VS-0.3	+55 VS+13.5(1)	V
VDD	VDD input	-0.3	+6	V
3V3	3.3 V regulator maximum allowable voltage		3.6	V
GNDx	Differential voltage between Grounds and TAB	-0.3	+0.3	V
SRCx max	t<400 ms Continuous		+40 +28	V
SRCx min	t<200 ms Continuous	-5 -1		V
GATEHx	External High Side MOSFET control	V_{SRCx} – 0.3	V_{SRCX}+12, V_{CP}+0.3(1)	V
GATELx	External Low Side MOSFET control	-0.3	12 V_{CP}+0.3(1)	V
DOUT, EN_OUT		-0.3	VDD+0.3	V
OUT_{X_max}	All half bridge outputs		+35 VS+0.3(1)	V
OUT_{X_min}	All internal half bridge outputs 4 A from ground, Outputs inactive, t_{Recirc}<10 ms	-1(2)		V
CP1-, CP2-	Charge pump pins	-0.3	+40 VS+0.3	V
CP1+, CP2+	Charge pump pins	-0.3 VS-0.3	+55 VS+13.5 V_{cp_out}+0.3(1)	V
CSN, SCK, SDI, DSO		-0.3	VDD+0.3	V
$T_{J(Operating)}$	Junction temperature	-40	175(3)(4)(5)	°C
$T_{J(Storage)}$	Storage temperature	-55	+150	°C

1. Of the values listed whichever is the lesser of them applies.

2. Power MOSFET body diode voltage when 4 A are recirculating through it.
3. All parameters are guaranteed, and tested, in the temperature range -40°C to 130°C (unless otherwise specified). The L99UDL01 will still operate and be functional at temperatures up to 175°C.
4. Parameter limits at higher temperatures than 130°C may change with respect to what is specified as per the standard temperature range.
5. Device functionality at temperatures greater than 130°C is guaranteed by design.

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
19-Jul-2017	1	Initial release.
12-Apr-2018	2	Updated *Figure 2: Pin connection diagram*.
02-May-2019	3	Updated *Table 2: Pin description* and *Table 3: Absolute maximum ratings*. Updated *Figure 2: Pin connection diagram*, *Figure 6: State diagram* and *Figure 7: Typical application diagram example*.

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