EVBUM2254/D

KAF-4320 Evaluation Timing Specification

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EVAL BOARD USER'S MANUAL

Altera Code Version Description

The Altera code described in this document is intended for use in the ADS−93x Timing Board. The code is written specifically for use with the following system configuration:

Table 1. SYSTEM CONFIGURATION

Evaluation Board Kit:	PN 4H0475
Timing Generator Board	3E8290 (ADS−933 3 MHz)
KAF−4320 CCD Imager Board	3E8371
Framegrabber Board	National Instruments PCI−1424

ALTERA CODE FEATURES / FUNCTIONS

The Altera Programmable Logic Device (PLD) performs the following functions:

Timing Generator

The PLD serves as a state machine based timing generator whose outputs interface to KAF−4320, the ADS−933 A/D converter, and the PCI−1424 Framegrabber. The behavior of these output signals is dependent upon the current state of the state machine. External digital inputs, as well as jumpers on the board can be used to set the conditions of certain state transitions (See Table 2). In this manner, the board may be run in any of the following operating modes:

- Continuous Capture Mode
- Triggered Capture Mode
- Internally or Externally Controlled Integration Timing Modes
- CCD Output Amplifier Enable/Disable during Integration Time Mode Option
- 2 x 2 Binning Mode Option

Timing Signal Adjustments

The PLD contains addressable registers that can be accessed via the digital input interface to adjust certain timing conditions on the board. The pulse−width and position of the H1, H2, RESET, CLAMP and AD_CLK can be adjusted in increments of $1/16^{th}$ of a pixel time. When operating in internally controlled integration time mode, the Integration time can be adjusted to be any one of 32 pre−programmed times.

Upon power up, or when the BOARD_RESET button is depressed, the PLD will reset these registers to their original (default) values.

ALTERA CODE I/O

Table 2. INPUTS

Symbol	Description
POWER_ON_DELAY	The rising edge of this signal clears and re−initializes the PLD
SYSTEM_CLK	48 MHz clock, 16X the desired pixel clock rate
INTEGRATE_CLK	100 Hz clock, Provides 10 ms unit integration time
SCLOCK	Digital input, Used as the external trigger in Triggered Capture Mode
SLOAD	Not Used
SDATA	Not used
JMP0	Output mode Control: HIGH = Triggered Capture Mode LOW = Continuous Capture Mode
JMP1	Binning Mode Control: HIGH = 2 X 2 Binning LOW = No Binning
JMP2	Internal/External Integration Mode Control: HIGH = External Integration Control using DIO15 LOW = Pre−set Integration Time selected by INT MODE register value
JMP3	Output Amplifier Enable Mode Control: HIGH = Disable amplifier during integration time. LOW = Always enable amplifier.
DIO[1..0]	Multiplexed CCD Video control lines
DIO[5..2]	Timing PLD Register Address Select Lines
DIO[13..6]	Timing PLD Register Data Select Lines
DIO14	Update Register Write Strobe
DIO15	User−Defined Integration control line; bring HIGH to end Integration

Table 3. OUTPUTS

Signal	Function	Description
Timing_Out11	AMP_ENABLE	Control line for alternate VDD supply to CCD output amplifier during Integration Time
Timing_Out10	Not Used	
Timing_Out9	MUX_SEL1	CCD VOUT Multiplexer control line
Timing_Out8	MUX_SEL0	CCD VOUT Multiplexer control line
Timing_Out7	V2_CLK	KAF−4320 CCD V2 Clock
Timing_Out6	V1_CLK	KAF−4320 CCD V1 Clock
Timing_Out5	R_CLK	KAF−4320 CCD Reset Clock
Timing_Out4	Not Used	
Timing_Out3	H1_CLK	KAF−4320CCD H1 Clocks
Timing_Out2	H2_CLK	KAF−4320 CCD H2 Clocks
Timing_Out1	H1L_CLK	KAF−4320 CCD H1L Clock
Timing_Out0	Not Used	
CLAMP	CLAMP	Pixel−Rate CDS Clamp Signal
AD_CLK	A/D CLOCK	ADS−933 A/D Clock (CDS Sample Signal)
PIX	PIXEL SYNC	PCI−1424 Frame Grabber Pixel Rate Synchronization
FRAME	FRAME SYNC	PCI−1424 Frame Grabber Frame Rate Synchronization

Table 3. OUTPUTS

Signal	Function	Description
LINE	LINE SYNC	PCI−1424 Frame Grabber Line Rate Synchronization
INTEGRATE	INT SYNC	High During CCD Integration Time

KAF−4320 SYSTEM TIMING CONDITIONS

Table 4. SYSTEM TIMING CONDITIONS

Description	Symbol	Time	Notes
System Clock Period	Tsys	21 ns	48 MHz system clock
Unit integration time	Uint	10 ms	Typical
Power stable delay	Tpwr	10 ms	Typical

Table 5. CCD TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
H1, H2, RESET period	Tpix	333 ns	1	3 MHz clocking of H1, H1L, H2, RESET
VCCD delay	Tvd	333 ns	1	Between Hclks stopping and V1 rising edge
V1, V2 Pulse Width	TVCCD	30 μs	90	Between V rising edge and V falling edge
Horizontal setup time	Ths	10 μs	30	Between 2nd V1 falling edge and Hclks startup
Vertical transfer period	Vperiod	100 μs	301	Vperiod = Tvd + (3 * TVCCD) + Ths
Pixels per line	PIX_X	350 μs	1050	1050 CCD pixels per line (1042 active)
Lines per frame	PIX_Y		1046	1046 CCD lines per frame (1042 active)
Vertical flush period	Fperiod	60 μs	180	Time to flush one line
Flush duration	Flines			Number of lines flushed = 2084
Flush delay	Fdelay	~5 ms		Time between last flush line and next UNIT INT clock
Flush time	Ftime	~135 ms		Ftime = (Fperiod x Flines) + Fdelay
External Trigger delay	Trig delay	0−10 ms		Variable due to asynchronous trigger

Table 6. ADS−933 A/D CONVERTER TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
AD CLK period	Tpix	333 ns	1	3 MHz clocking of A/D Clock

Table 7. PCI−1424 TIMING CONDITIONS

Description	Symbol	Time	Pixel Counts	Notes
PIX period	Tpix	333 ns	1	3 MHz clocking of PIX sync signal
PIX per line			1050	Number of PIX syncs per line
2 X 2 Binning PIX per line			525	Number of PIX syncs per line in binning mode
LINE per frame			1046	Number of LINE syncs per line
2 X 2 Binning LINE per frame			522	Number of LINE syncs per line in binning mode

PIXEL RATE CLOCKS GENERATION

The pixel rate clocks are derived from the system clock. They operate at $1/16^{th}$ the frequency of the system clock. The system clock is divided down to create sixteen different time steps per pixel. Each of the pixel rate signals start and stop positions can be adjusted by loading the desired start and stop positions into the appropriate register. In this way both the signals position and duty cycle can be adjusted. The timing of these signals is reset back to the original default positions on power−up or when the board reset button is pressed.

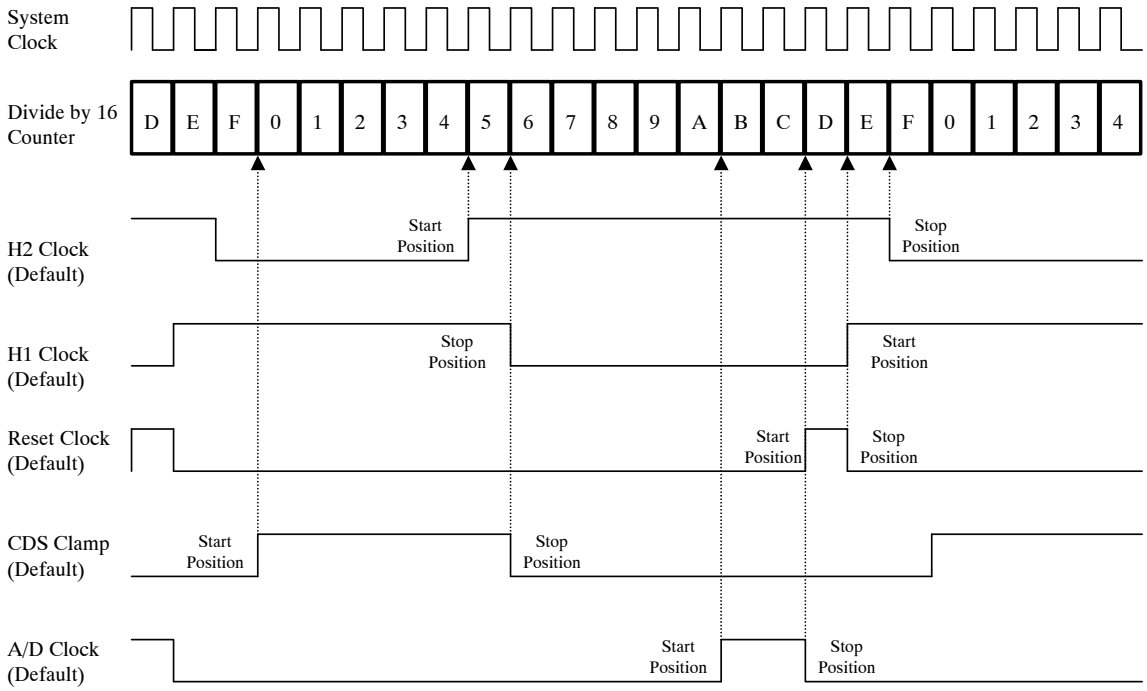

Figure 1. Pixel Clock Generation Timing

PARALLEL INTERFACE TIMING AND INTERNAL REGISTER DESCRIPTION

Table 8. INTERNAL REGISTER DESCRIPTION

Register Name	Address	D0	D1	D2	D3	D4	D5	D6	D7	Default Value (HEX)
Not Used	0	X	X	X	X	X	X	X	X	X
Not Used	1	X	X	X	X	X	X	X	X	X
Not Used	2	X	X	X	X	X	X	X	X	X
Not Used	3	X	X	X	X	X	X	X	X	X
Not Used	4	X	X	X	X	X	X	X	X	X
Not Used	5	X	X	X	X	X	X	X	X	X
Not Used	6	X	X	X	X	X	X	X	X	X
H1 Clock Position	7	Start Position				Stop Position				6E
		LSB			MSB	LSB			MSB	
H2 Clock Position	8	Start Position				Stop Position				F5
		LSB			MSB	LSB			MSB	
Reset Clock Position	9	Start Position				Stop Position				ED
		LSB			MSB	LSB			MSB	
Clamp Position	10	Start Position				Stop Position				60
		LSB			MSB	LSB			MSB	
A/D Clock Position	11	Start Position				Stop Position				DB
		LSB			MSB	LSB			MSB	
Not Used	12	X	X	X	X	X	X	X	X	X
Integration Mode Setting	13	LSB					MSB	X	X	0
Not Used	14	X	X	X	X	X	X	X	X	X
Not Used	15	X	X	X	X	X	X	X	X	X

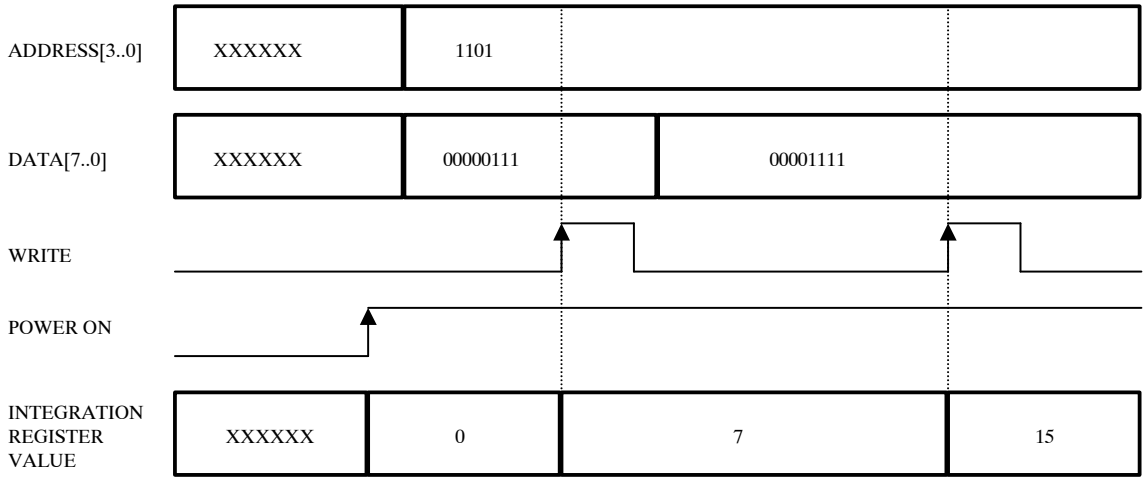

Figure 2. Internal Register Update Timing Example

MODES OF OPERATION

The system's operating mode is selected by setting the jumpers JMP[3..0] to the appropriate level.

Image Capture Mode

Continuous Capture Mode

To operate in Continuous Capture Mode, set JMP0 to the LOW position. In this mode the board will continuously repeat the sequence of integrating and then reading out the CCD.

Triggered Capture Mode

To operate in Triggered Capture Mode, set JMP0 to the HIGH position. In this mode, the board requires an externally generated trigger signal to begin the single frame capture sequence. Upon receiving the trigger the board will Flush the CCD of accumulated charge, integrate, and then readout a single frame. Upon completion of readout, the board will wait for another trigger to repeat the sequence.

Table 9. IMAGE CAPTURE MODES

JMP0	Image Capture Mode	Notes
0	Continuous Capture Mode	Default Mode
1	Triggered Capture Mode	

BINNING MODE

To operate without pixel binning, set JMP1 to the LOW position. In this mode the CCD is operated to reset the CCD's floating diffusion after each pixel has been sampled off chip. To operate in 2 X 2 pixel binning mode, set JMP1 to the HIGH position. In this mode the CCD is operated to bin a 2 x 2 pixel charge packet in the CCD's floating diffusion before sampling and resetting the CCD's floating diffusion.

Table 10. BINNING MODES

JMP1	Binning Mode Operation	Notes
0	No Binning	Default Mode
1	2 X 2 Binning Mode	

Integration Timing Control Modes

To operate in internally controlled integration mode, set JMP2 to the LOW position. When operating in internally controlled integration mode, the integration time is controlled by the INT MODE register and can be any one of the thirty−two different pre−defined integration times. Each of the pre−defined integration times is a multiple of the Unit integration time. (See Table 12) To operate in externally controlled integration mode, set JMP2 to the HIGH position. When operating in externally controlled integration mode, the integration time is controlled by an external timer. An external input via the digital input interface, DIO15, is used to end the integration time. In this way any number of custom integration times can be created. The rising edge of the external input ends the integration time (See Figure 6).

Table 11. INTEGRATION CONTROL MODES

JMP2	Binning Mode Operation	Notes
0	Internally controlled Integration times	Default Mode
1	Externally controlled Integration times	

Table 12. INTERNALLY SELECTABLE INTEGRATION TIMES

INT MODE Register Value	Integration Time (ms)	INT MODE Register Value	Integration Time (ms)
0	0	16	700
1	10	17	800
2	20	18	900
3	30	19	1000
4	40	20	2000
5	50	21	3000
6	60	22	4000
7	70	23	5000
8	80	24	6000
9	90	25	7000
10	100	26	8000
11	200	27	9000
12	300	28	10000
13	400	29	35000
14	500	30	50000
15	600	31	65000

Amplifier Disable Mode

To operate without ever disabling the CCD output amplifier, set JMP3 to the LOW position.

To reduce the CCD output amplifier's VDD bias voltage during integration time, set JMP3 to the HIGH position. In this mode, the CCD output amplifier supply (VDD) is switched to a lower voltage (ALT_VDD) during integration, thereby disabling the amplifier and reducing power consumption. This feature may be used to reduce thermal artifacts in the image.

Table 13. CCD AMPLIFIER OPERATING MODES

JMP3	CCD Amplifier Operating Mode Control	Notes
0	Internally controlled Integration times	Default Mode
1	Externally controlled Integration times	

TIMING GENERATOR STATE MACHINE DESCRIPTION

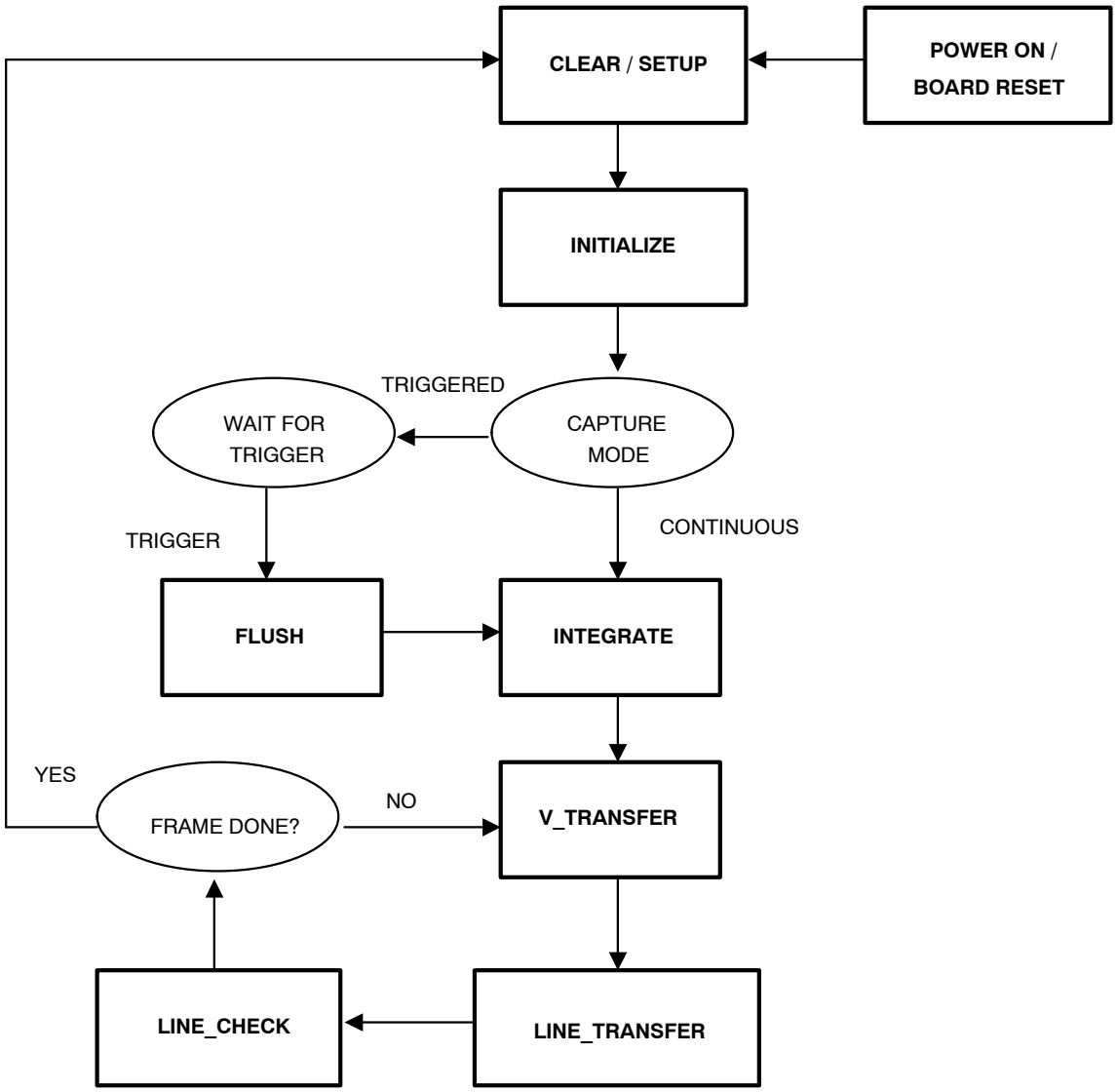

Figure 3. Timing Generator State Machine

Power−On/Board Reset

When the board is powered up or the Board Reset button is pressed, the Altera PLD is internally reset. When this occurs all internal counters are cleared, the state machine is reset, and all of the signal position and mode control registers are reset back to their default values. Upon completion of the board reset, the board will be ready to proceed according to the output mode selected.

CLEAR/SETUP and INITIALIZE States

The timing generator state machine is free running. It cycles through the states depending on the jumper settings and DIO inputs, and then returns back to the clear/setup state to begin the next frame. The clear/setup state is used to reset the internal PLD counters at the beginning of each frame.

The INITIALIZE state is used to determine the selected operating modes, and to synchronize with the INTEGRATE_CLK as needed.

In Continuous Capture mode, the state machine will wait in the INITIALIZE state for the next rising edge of INTEGRATE_CLK (See Figure 5). The reason for the delay before entering the INTEGRATE state is so that state machine is synchronized with the INT_CLK ensuring that consistent integration times are achieved when using the pre−defined internal integration modes.

FLUSH State

The FLUSH state will occur in the Triggered Capture Mode only. During the FLUSH state, the CCD is flushed of any accumulated charge by running the vertical clocks continuously for a number of lines. Upon flush completion, the state machine will wait in the flush state until the next rising edge of the INTEGRATE_CLK.

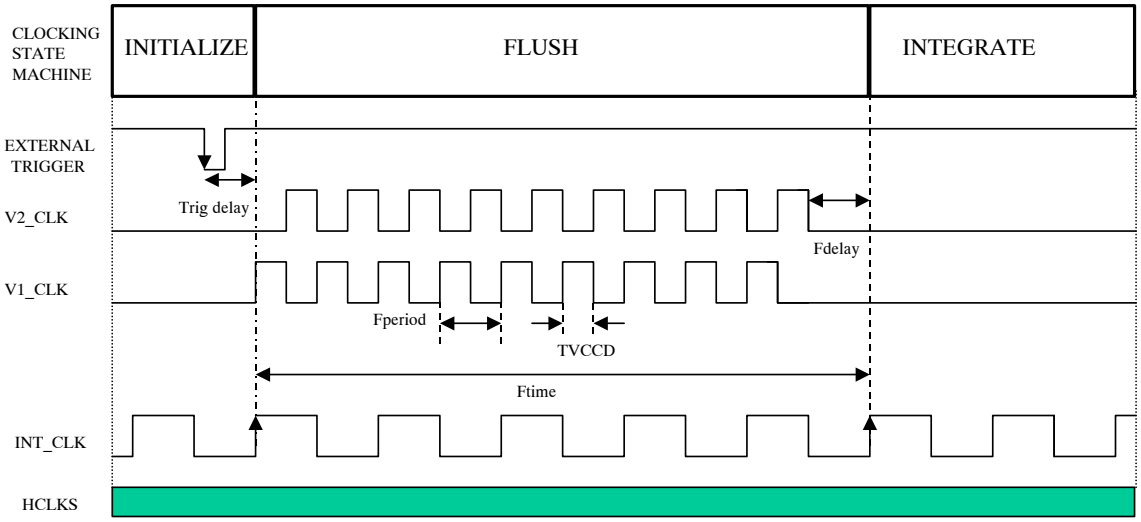

Figure 4. Flush Timing

INTEGRATE State

During the INTEGRATE state, the output signal INTEGRATE goes high and stays high until the integration time is over. When the board is configured for internally controlled integration mode operation, the integration time will depend on the value of the integration time register (See Table 12 and Figure 5). When the board is set up for externally controlled integration mode operation, the integration time will end when the external integration control signal (DIO15) is brought HIGH (See Figure 6).

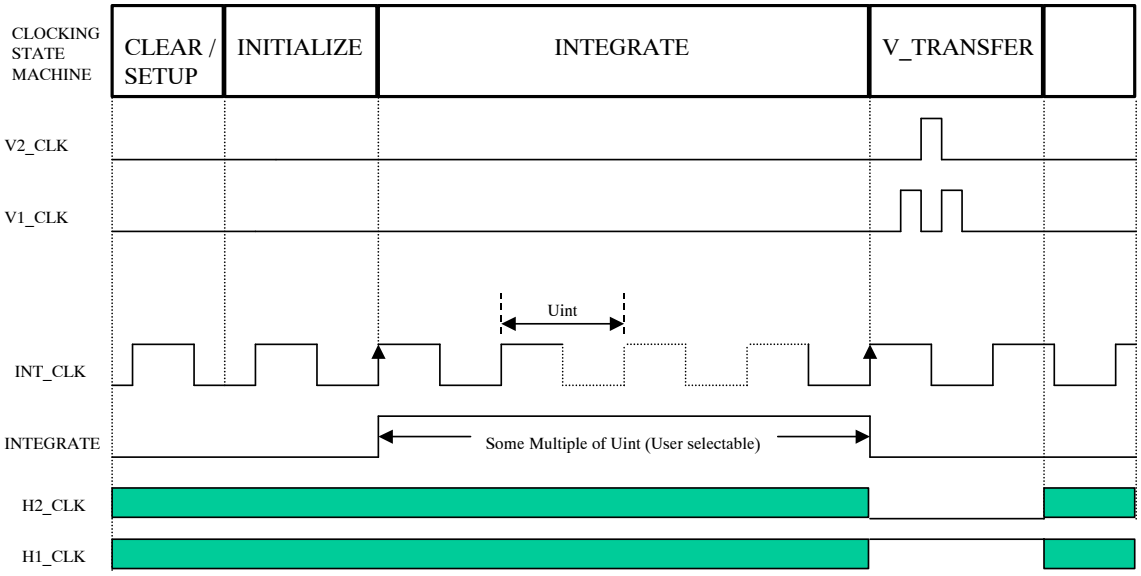

Figure 5. Integration Timing (Internal INT Mode)

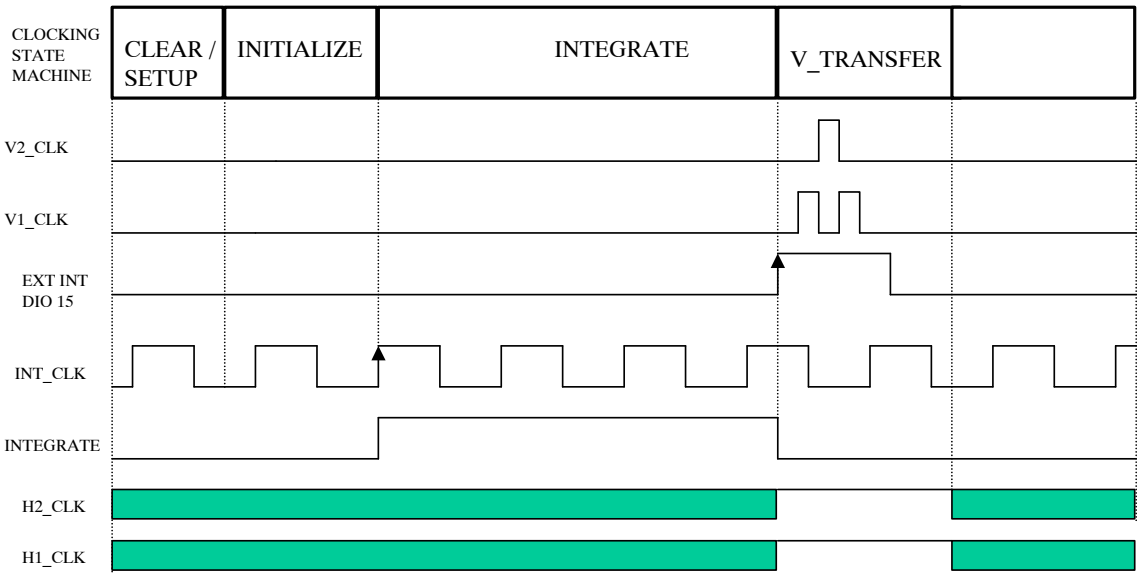

Figure 6. Integration Timing (External INT Mode)

V_TRANSFER State

During the V_TRANSFER state, each line (row) of charge is transported towards the horizontal CCD register using the Vertical clocks. A vertical transfer counter in the PLD is used to determine when the vertical clocks are forced high and low and when the vertical transfer time and horizontal delay time (Ths) are completed.

When operating in 2 X 2 Binning Mode, two lines of charge are transported towards the horizontal CCD register before the horizontal register is read out. The vertical clock timing is set in the timing generator PLD and is not adjustable.

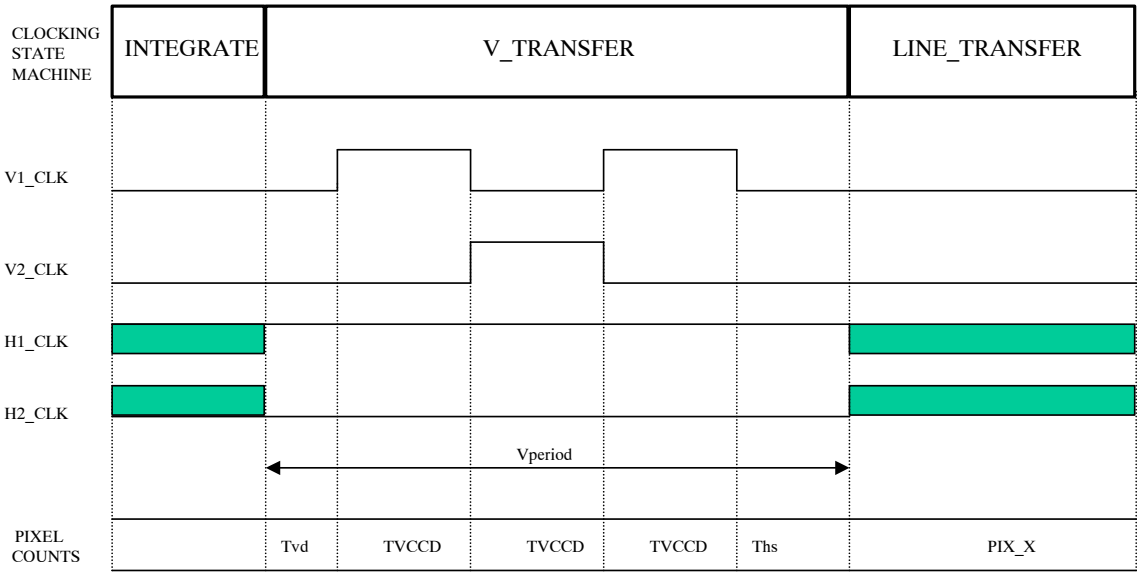

Figure 7. Vertical Transfer Timing

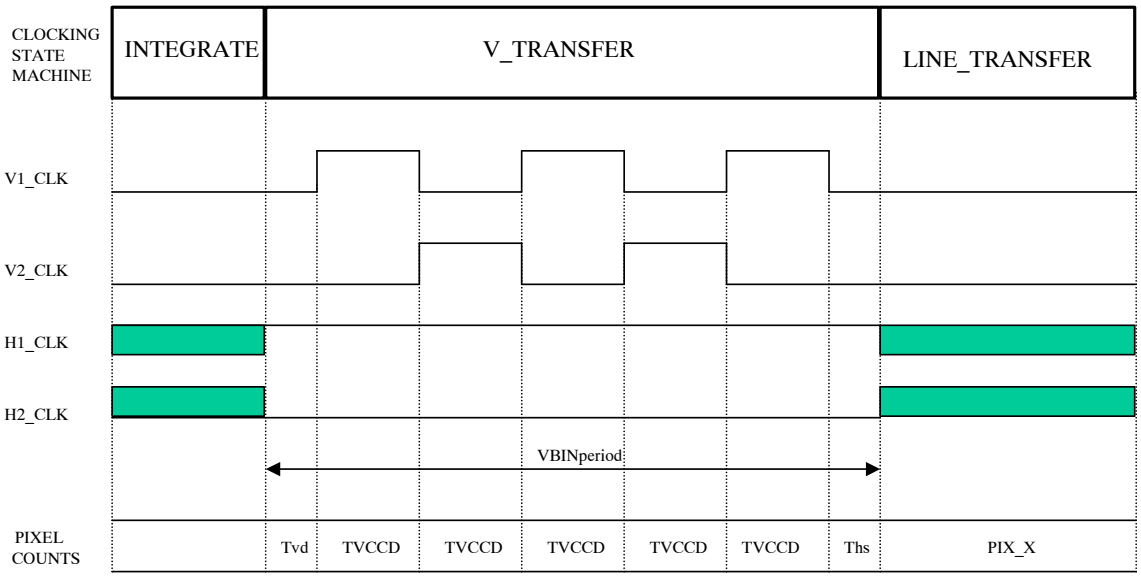

Figure 8. Vertical Transfer Timing (2 X 2 Binning)

LINE_TRANSFER and LINE_CHECK State

During the LINE_TRANSFER state, charge is transported to the CCD output structure pixel by pixel. A line transfer counter in the PLD is used to keep track of how many pixels have been transported, and to synchronize the PCI−1424 framegrabber synchronization signals.

When operating in 2 X 2 Binning Mode, two pixels of charge are transported towards the output structure and the charge is allowed to accumulate on the floating diffusion before being sensed off−chip and the floating diffusion is reset. In Binning Mode the RESET_CCD clock, the CDS CLAMP and SAMPLE clocks, and the framegrabber PIX clock are all gated off every other pixel.

At the end of each line transfer, the Line counter is incremented in the LINE_CHECK State. If all of the lines have been clocked out of the CCD, the state machine goes to the CLEAR/SETUP state; if not, the state machine returns to the V_TRANSFER state, and transfers another line of charge into the horizontal register.

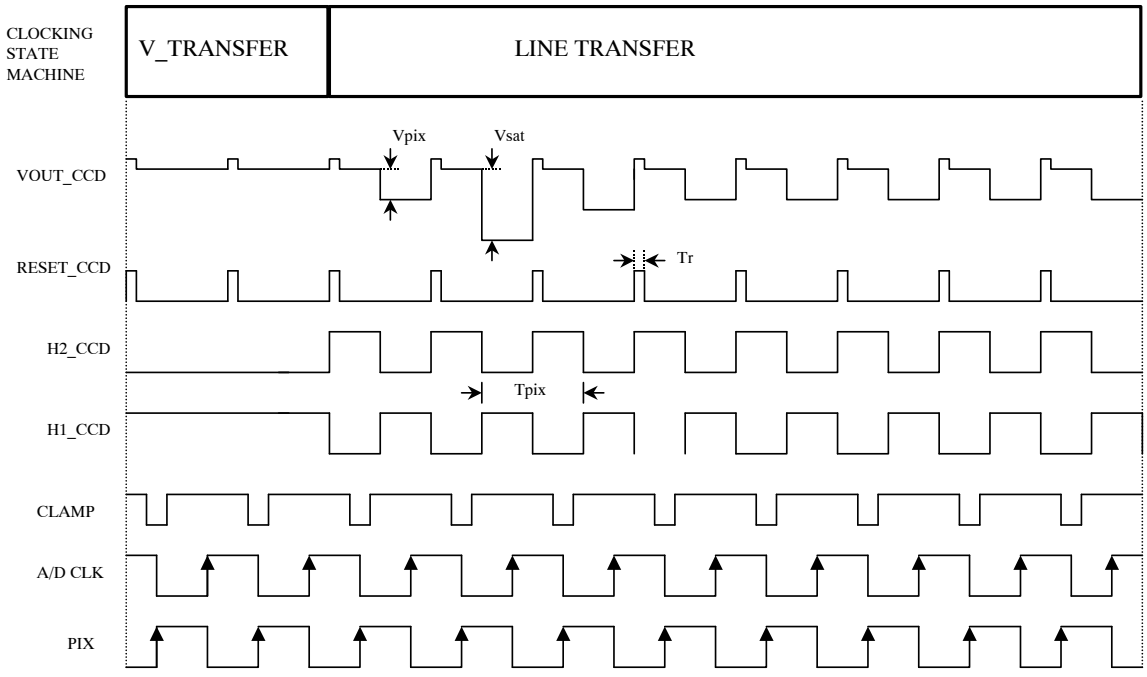

Figure 9. Horizontal Transfer Timing

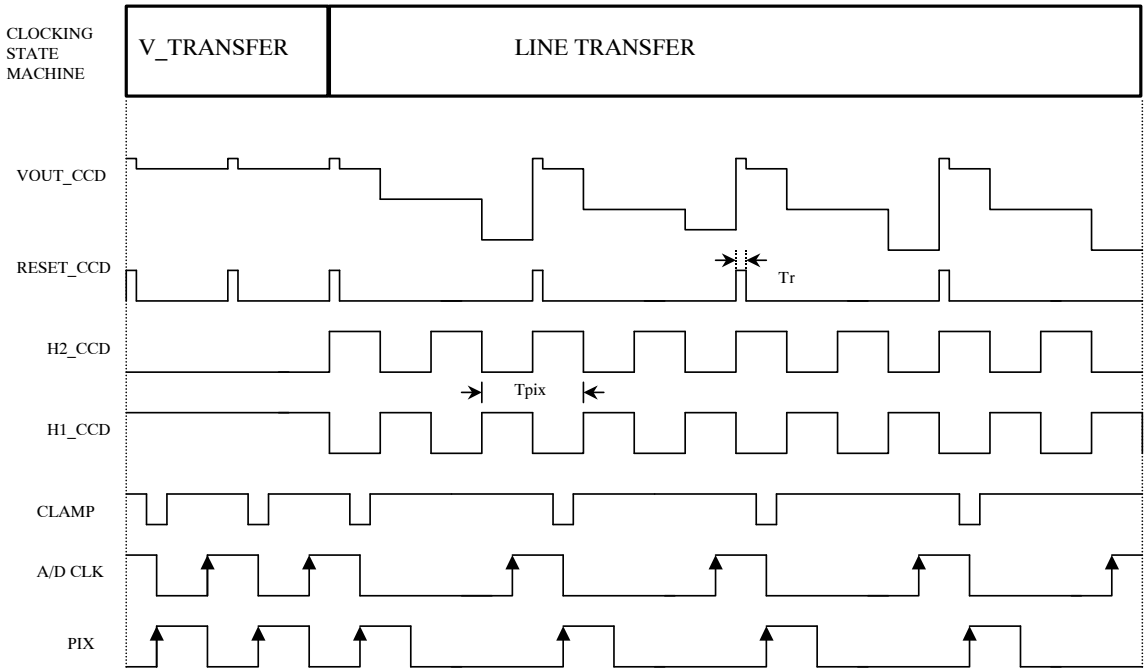

Figure 10. Horizontal Transfer Timing (2 X 2 Binning)

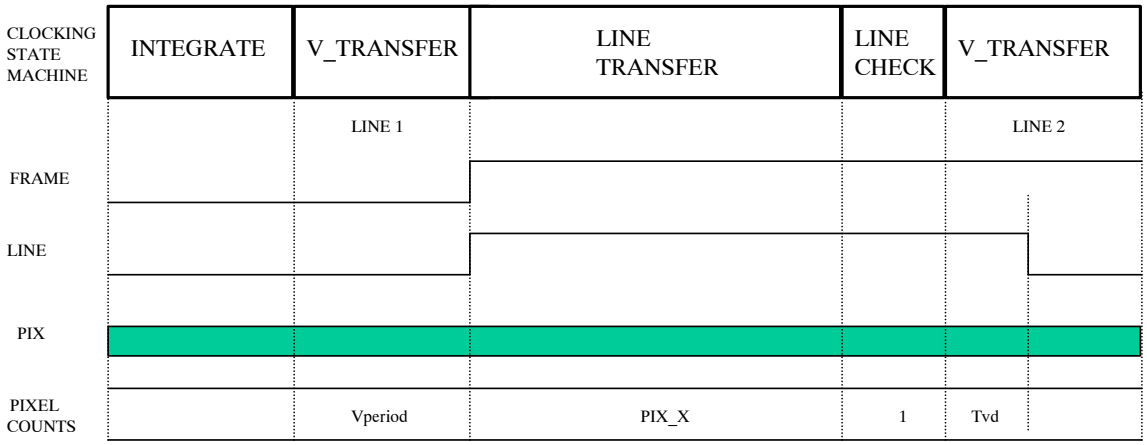

Figure 11. PCI−1424 Frame Grabber Timing

Warnings and Advisories

When programming the Timing Board, the Imager Board must be disconnected from the Timing Board before power is applied. If the Imager Board is connected to the Timing Board during the reprogramming of the Altera PLD, damage to the Imager Board will occur.

Purchasers of a an Evaluation Board Kit may, at their discretion, make changes to the Timing Generator Board firmware. ON Semiconductor can only support firmware developed by, and supplied by, ON Semiconductor. Changes to the firmware are at the risk of the customer.

Ordering Information

Please address all inquiries and purchase orders to:

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References

- KAF−4320 Device Specification
- KAF−4320 Imager Board User Manual
- KAF−4320 Imager Board Schematic
- ADS−93X Timing Generator Board User Manual
- ADS−93X Timing Generator Board Schematic
- Datel ADS−933 Product Data Sheet

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