Errata

The following are known problems with Rev. A of the AT89S2051/S4051 device:

1. JBC to TF0, TF1, IE0, IE1

JBC may cause a loss of interrupt information if used with any interrupt flag (see item #2 for SCON). Therefore JBC should not be used to poll for interrupt flags.

Problem Fix/Workaround:

```
POLL:  JBC FLAG, NEXT
       SJMP POLL
```

should be replaced by:

```
POLL:  JNB FLAG, POLL
       CLR FLAG
       SJMP NEXT
```

2. Read-Modify-Write to SCON (SETB, CLR, CPL, ANL, ORL, XRL, JBC)

Read-Modify-Write (RMW) instructions may cause a loss of UART interrupt information if used with any bit in SCON, i.e. the RMW instructions need to be treated as a direct move to SCON such as MOV SCON,#IMM. These instructions may be used when it is not possible for the interrupt to occur at the same time as the instruction is being executed, which means in the following circumstances::

A. The UART is not currently operating, **or**
B. Within a short period of time after TI or RI is set during half-duplex communications, **or**
C. Within a short period of time after both TI and RI are set during full-duplex communications, and before the next byte is transmitted.

3. Read-Modify-Write to ACSR (ANL, ORL, XRL)

Read-Modify-Write instructions may cause a loss of Comparator interrupt information if used with any bit in ACSR, i.e. the RMW instructions need to be treated as a direct move to ACSR such as MOV ACSR,#IMM. These instructions may be used when it is not possible for the interrupt to occur at the same time as the instruction is being executed, which means in the following circumstances:

A. The Comparator is not active, **or**
B. Within a short period of time after CF is set, **or**
C. The flag is level-sensitive and the input condition will last through the next instruction, **or**
D. Any time, if the application can afford to miss an edge event. The actual miss frequency will depend on the application code.

4. Interrupt Recovery from Power-down Mode

When attempting interrupt recovery from power-down, the external interrupt pins $\overline{INT0}$ (P3.2) and $\overline{INT1}$ (P3.3) should not transition low until at least 10 µs after entry into power-down. If the pins are low immediately before entering power-down, or go low while attempting to enter power-down, the device can get stuck in a power-down-like state requiring a power cycling sequence to wake up.

AT89 Microcontrollers

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Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

Literature Requests
www.atmel.com/literature

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