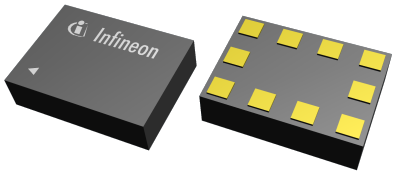
BGSA403ML10

Four throws low resistance antenna tuning switch

Features

- Low R_{ON} resistance of 0.98 Ω at each port in ON state
- Low C_{OFF} capacitance of 205 fF at each port in OFF state
- High RF operating peak voltage handling of typical 50 V in OFF state
- MIPI RFFE 2.1 compliant control interface
- Extremely low current consumption of 22 µA
- 4 USID addresses enabled by external condition at USID_SEL pin
- Small form factor (MSL1, 260 °C per JEDEC J-STD-020)



RoHS
Halogen-Free
Lead-Free
Green

Potential applications

- Impedance, antenna and inductance tuning
- Tunable filters

Product validation

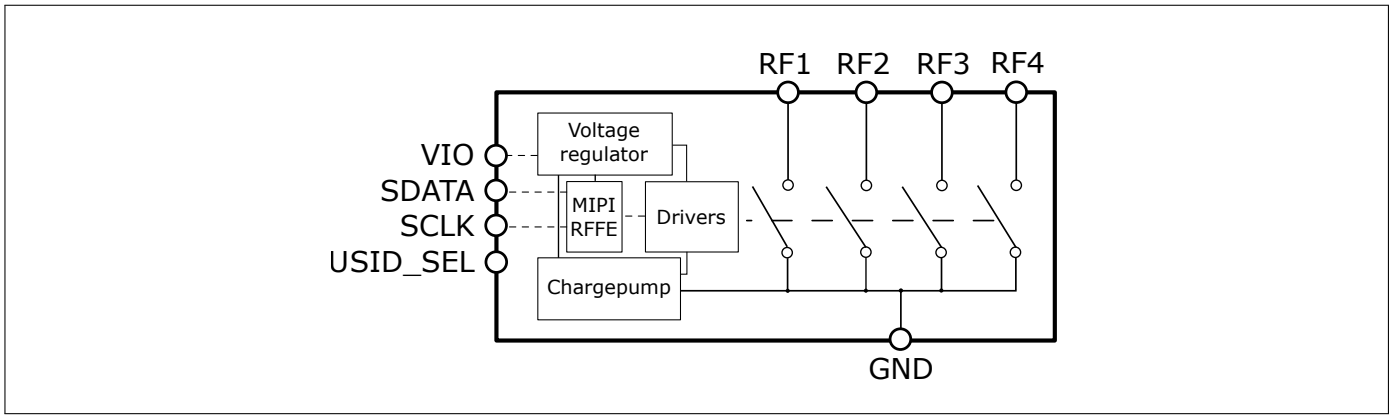
Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The BGSA403ML10 is a versatile shunt to ground 4xsingle-pole single-throw (4xSPST) RF antenna tuning switch. It is optimized for low C_{off} as well as low R_{on} enabling applications up to 7.125 GHz.

The BGSA403ML10 is ideal for antenna tuning application. This chip integrates on-chip CMOS logic and power supply regulation. Its digital control interface is compliant with MIPI2.1 RFFE specification and each switch throw can be programmed individually or all together in the same RFFE command frame. Up to 4 instantiations of the same device can be controlled using the same RFFE bus thanks to its 4 states USID_SEL pin unique feature.

Block diagram



Type	Marking	Package	Ordering information
BGSA403ML10	3T	TSLP-10-3	BGSA 403ML10 E6327

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1 Maximum ratings

Table 1: Maximum ratings table at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.4	–	7.125	GHz	[1]
RFFE supply voltage [2]	V_{IO}	-0.3	–	2.2	V	Only for infrequent and short duration time periods
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF peak voltage	V_{RF_max}	–	–	55	V	Short term peaks (1μs in 0.1% duty cycle), exceeding typical linearity, Ron and Coff parameters, in Isolation mode, test condition schematic in Fig. 1
ESD robustness, CDM [3]	$V_{ESD_{CDM}}$	-1	–	+1	kV	
ESD robustness, HBM [4]	$V_{ESD_{HBM}}$	-2	–	+2	kV	
Junction temperature	T_j	–	–	125	°C	–
Thermal resistance junction - soldering point	R_{thJS}	–	–	50	K/W	–
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltage allowed on RF-Ports
RFFE control voltage levels	V_{SCLK}, V_{SDATA}, V_{USID_SEL}	-0.7	–	V_{IO}+0.7 (max. 2.2)	V	–

[1] Switch has a low-pass response. For higher frequencies, losses have to be considered for their impact on thermal heating. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{IO}. A high RF ripple at the V_{IO} can exceed the maximum ratings by $V_{IO} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001 (R=1.5 kΩ, C=100 pF).

Warning: Stresses above the max. values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and life time. Functionality of the device might not be given under these conditions.

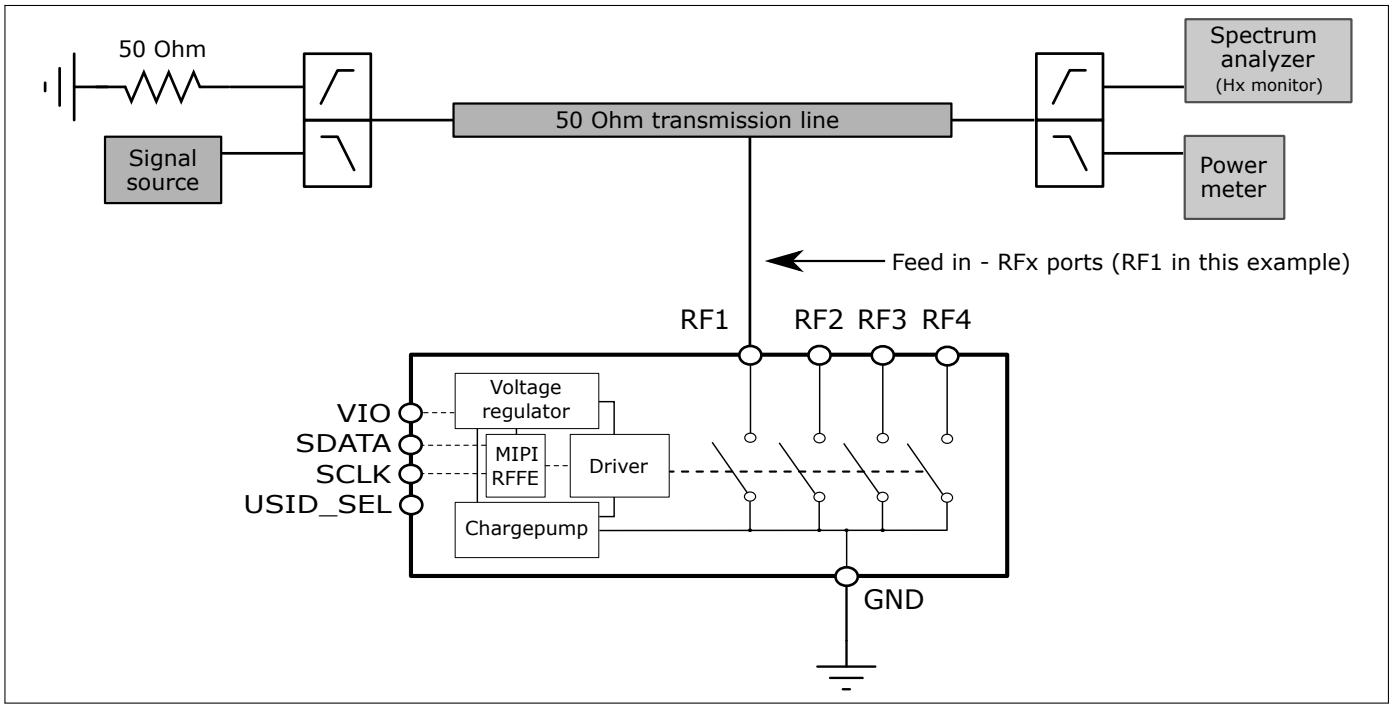

Figure 1: RF operating voltage and harmonic distortion measurement configuration

2 DC characteristics

Table 2: DC characteristics at T_A = −40 °C to 85 °C

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RFFE supply voltage	V_{IO}	1.65	1.8	1.95	V	–
RFFE input high voltage[1]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current [2]	I_{VIO}	–	22	40	µA	ACTIVE mode, ≤ 35 dBm RF power
		–	2 0.5 [3]	8 1 [3]	µA µA	SECONDARY_ACTIVE mode (LOW POWER) with analog circuitry powered OFF

[1] SCLK and SDATA
[2] No traffic on MIPI bus
[3] Supply current reduced after first MIPI RFFE command

3 RF small signal characteristics

Table 3: Parametric specifications for each SPST

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
RF1, RF2, RF3 or RF4 to GND DC ON resistance	$R_{ON_{SPST}}$	–	0.98	1.2	Ω	V_{IO} = 1.65 - 1.95 V, T_A = 25 °C, Z_0 = 50 Ω
RF1, RF2, RF3 or RF4 to GND OFF capacitance, 1 GHz [1]	$C_{OFF_{SPST}}$	–	205	220	fF	
RF1, RF2, RF3 or RF4 to GND DC OFF resistance	$R_{OFF_{SPST}}$	170	325	–	kΩ	

[1] Measurement accuracy limited by test setup

Table 4: RF electrical parameters

Frequency range	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
Isolation between adjacent RF ports (All OFF / Isolation Mode)[1]						
600 - 960 MHz	*ISO*	35	40	–	dB	State 0, V_{IO} = 1.65 … 1.95 V, Z_0 = 50 Ω, T_A = −40 °C... + 85 °C
1160 - 1300 MHz		32	36	–	dB	
1400 - 1700 MHz		30	34	–	dB	
1700 - 2200 MHz		28	32	–	dB	
2200 - 2700 MHz		26	30	–	dB	
3300 - 4200 MHz		24	28	–	dB	
4400 - 5000 MHz		24	28	–	dB	
5150 - 5925 MHz		24	28	–	dB	
5950 - 7125 MHz		24	28	–	dB	
Isolation between non-adjacent RF ports (All OFF / Isolation Mode) [1]						
600 - 960 MHz	*ISO*	54	64	–	dB	State 0, V_{IO} = 1.65 … 1.95 V, Z_0 = 50 Ω, T_A = −40 °C... + 85 °C
1160 - 1300 MHz		51	60	–	dB	
1400 - 1700 MHz		49	58	–	dB	
1700 - 2200 MHz		47	56	–	dB	
2200 - 2700 MHz		46	55	–	dB	
3300 - 4200 MHz		45	55	–	dB	
4400 - 5000 MHz		45	58	–	dB	
5150 - 5925 MHz		45	58	–	dB	
5950 - 7125 MHz		38	53	–	dB	
Isolation between adjacent RF ports (RFx ON Mode)[1]						
600 - 960 MHz	*ISO*	34	49	–	dB	State 1, 2, 4, 8, V_{IO} = 1.65 … 1.95 V, Z_0 = 50 Ω, T_A = −40 °C... + 85 °C
1160 - 1300 MHz		32	43	–	dB	
1400 - 1700 MHz		29	40	–	dB	
1700 - 2200 MHz		27	37	–	dB	
2200 - 2700 MHz		25	35	–	dB	
3300 - 4200 MHz		23	30	–	dB	
4400 - 5000 MHz		21	28	–	dB	
5150 - 5925 MHz		19	27	–	dB	
5950 - 7125 MHz		16	26	–	dB	
Isolation between non-adjacent RF ports (RFx ON Mode)[1]						
600 - 960 MHz	*ISO*	54	68	–	dB	State 1, 2, 4, 8, V_{IO} = 1.65 … 1.95 V, Z_0 = 50 Ω, T_A = −40 °C... + 85 °C
1160 - 1300 MHz		51	62	–	dB	
1400 - 1700 MHz		49	59	–	dB	
1700 - 2200 MHz		47	57	–	dB	
2200 - 2700 MHz		44	54	–	dB	
3300 - 4200 MHz		36	52	–	dB	
4400 - 5000 MHz		33	49	–	dB	
5150 - 5925 MHz		31	46	–	dB	
5950 - 7125 MHz		27	42	–	dB	

[1] On application board without any matching components

4 RF large signal parameter

Table 5: RF large signal specifications at $T_A = -40\,°C...+85\,°C$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF operating voltage	V_{RF_opr}	–	–	48	V	In isolation mode, 900MHz test condition schematic in Fig. 1. $T_A = 25\,°C$
Harmonic distortion, off mode						
All RF Ports Second order harmonics	P_{H2}	–	-93	-82	dBm	26 dBm, 50 Ω, f_0 = 663 MHz
All RF Ports Third order harmonics	P_{H3}	–	-94	-87	dBm	26 dBm, 50 Ω, f_0 = 663 MHz
All RF Ports Second order harmonicss	P_{H2}	–	-77	-65	dBm	35 dBm, 50 Ω, f_0 = 920 MHz
All RF Ports Third order harmonics	P_{H3}	–	-80	-70	dBm	35 dBm, 50 Ω, f_0 = 920 MHz
All RF Ports Second order harmonics	P_{H2}	–	-77	-67	dBm	33 dBm, 50 Ω, f_0 = 1910 MHz
All RF Ports Third order harmonicss	P_{H3}	–	-76	-67	dBm	33 dBm, 50 Ω, f_0 = 1910 MHz
All RF Ports Second order harmonics	P_{H2}	–	-79	-70	dBm	29 dBm, 50 Ω, f_0 = 2690 MHz
All RF Ports Third order harmonics	P_{H3}	–	-84	-74	dBm	29 dBm, 50 Ω, f_0 = 2690 MHz
All RF Ports Second order harmonics	P_{H2}	–	-73	-64	dBm	29 dBm, 50 Ω, f_0 = 3550 MHz
All RF Ports Third order harmonics	P_{H3}	–	-80	-70	dBm	29 dBm, 50 Ω, f_0 = 3550 MHz
All RF Ports Second order harmonics	P_{H2}	–	-71	-61	dBm	29 dBm, 50 Ω, f_0 = 4200 MHz
All RF Ports Third order harmonics	P_{H3}	–	-81	-70	dBm	29 dBm, 50 Ω, f_0 = 4200 MHz
All RF Ports Second order harmonics	P_{H2}	–	-71	-61	dBm	29 dBm, 50 Ω, f_0 = 5000 MHz
All RF Ports Third order harmonics	P_{H3}	–	-75	-61	dBm	29 dBm, 50 Ω, f_0 = 5000 MHz
All RF Ports > Third order harmonics	P_{Hx}	–	–	-75	dBm	29 dBm, 50 Ω

Table 6: RF large signal specifications at $T_A = -40\,°C... +85\,°C$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Intermodulation distortion IIP2						
IIP2, low	IIP2,l	120	138	–	dBm	IIP2 conditions table 7
IIP2, high	IIP2,h	120	135	–	dBm	
Intermodulation distortion IIP3						
IIP3	IIP3	75	84	–	dBm	IIP3 conditions table 8

Table 7: IIP2 conditions table

Band	In-band frequency [MHz]	Blocker frequency 1 [MHz]	Blocker power 1 [dBm]	Blocker frequency 2 [MHz]	Blocker power 2 [dBm]
Band 1 Low	2140	1950	20	190	0
Band 1 High	2140	1950	20	4090	0
Band 5 Low	881.5	836.5	20	45	0
Band 5 High	881.5	836.5	20	1718	0
Band 7 Low	2655	2535	20	120	0
Band 7 High	2655	2535	20	5190	0

Table 8: IIP3 conditions table

Band	In-band frequency [MHz]	Blocker frequency 1 [MHz]	Blocker power 1 [dBm]	Blocker frequency 2 [MHz]	Blocker power 2 [dBm]
Band 1	2140	1950	20	1760	0
Band 5	881.5	836.5	20	791.5	0
Band 7	2655	2535	20	2415	0

5 MIPI RFFE specification

The MIPI RFFE interface is implemented according to the following specifications and documents:

- MIPI Alliance Specification for RF Front-End Control Interface version 2.1 - 18 December 2017
- MIPI Alliance Errata 01 for MIPI RFFE Specification Version v2.1 - 24 February 2019
- Qualcomm RFFE Vendor specification 80-N7876-1 Rev. Y (December 3, 2018)

Table 9: MIPI features

Feature	Supported	Comment
MIPI RFFE 2.1 standard	Yes	Backward compatible to MIPI 2.0 standard
Register 0 write command sequence	Yes	
Register read and write command sequence	Yes	
Extended register read and write command sequence	Yes	
Masked write command sequence	Yes	Indicated as MW in below register mapping tables
Support for standard frequency range operations for SCLK	Yes	Up to 26 MHz
Support for extended frequency range operations for SCLK	Yes	Up to 52 MHz
Longer reach RFFE bus length feature	Yes	
Programmable driver strength	Yes	Up to 80 pF
Programmable Group SID	Yes	
Programmable USID	Yes	
Trigger functionality	Yes	
Extended triggers and trigger masks	Yes	
Broadcast / GSID write to PM TRIG register	Yes	
Reset	Yes	Via VIO, PM TRIG or software register
Status / error sum register	Yes	
Extended product ID register	Yes	
Revision ID register	Yes	
Group SID register	Yes	
USID select pin	Yes	See table 16

Table 10: Startup behavior

Feature	State	Comment
Power status	Low power	Device in SECONDARY_ACTIVE mode (LOW POWER) after start-up
Trigger function	Enabled	Enabled after start-up. Programmable via behavior control register

Table 11: Device control timing at V_{IO} = 1.65 — 1.95 V, T_A = 25 °C, P_{IN} = 0 *dBm*

Parameter	Symbol	Values			Unit	STATE / Notes
		Min.	Typ.	Max.		
ON Switching Time	$t_{ST,ON}$	–	–	16	µs	50% last SCLK rising edge of the register write command to 10% of RF amplitude, see Fig. 2
OFF Switching Time	$t_{ST,OFF}$	–	–	5	µs	50% last SCLK rising edge of the register write command to 90% of RF amplitude, see Fig. 2

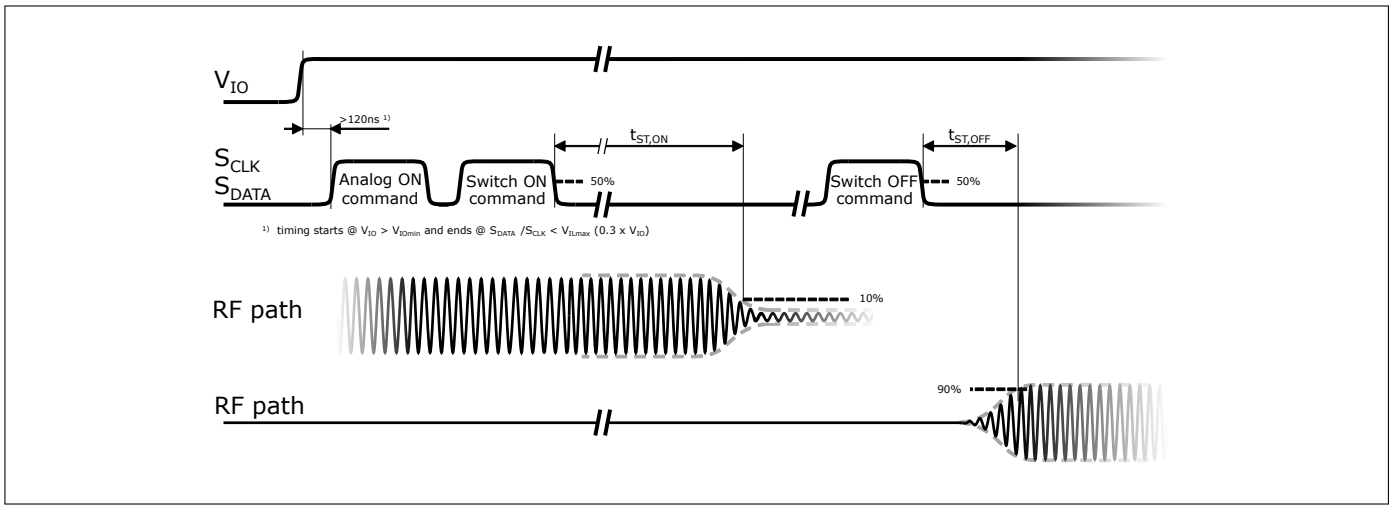

Figure 2: BGSA403ML10 Switching time behavior

Table 12: Register mapping, table I

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x00	REGISTER_0	7:0	MODE_CTRL	RF Switch Control	00000000	No	Yes Trigger 0-10	R/W MW
0x01	REGISTER_1	7:0	MODE_CTRL	RF Switch Control	00000000	No	Yes Trigger 0-10	R/W MW
0x1C	PM_TRIG	7	PWR_MODE(1) Operation Mode	0: Normal operation (ACTIVE) 1: Low Power Mode (LOW POWER)	1	Yes	No	R/W MW
		6	PWR_MODE(0) State Bit Vector	0: No action (ACTIVE) 1: Powered Reset (STARTUP to ACTIVE to LOW POWER)	0			
		5	TRIGGER_MASK_2	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0	No		
		4	TRIGGER_MASK_1	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		3	TRIGGER_MASK_0	0: Data masked (held in shadow REG) 1: Data not masked (ready for transfer to active REG)	0			
		2	TRIGGER_2	0: No action (data held in shadow REG) 1: Data transferred to active REG	0	Yes		
		1	TRIGGER_1	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
		0	TRIGGER_0	0: No action (data held in shadow REG) 1: Data transferred to active REG	0			
0x1D	PRODUCT_ID	7:0	PRODUCT_ID	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	01111010	No	No	R
0x1E	MAN_ID	7:0	MANUFACTURER_ID [7:0]	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.	00011010	No	No	R
0x1F	MAN_USID	7:4	MANUFACTURER_ID [11:8]	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.	0001	No	No	R
		3:0	USID[3:0]	USID_Sel pin	See table 16	No	No	R/W

Table 13: Register mapping, table II

Register Address	Register Name	Data Bits	Function	Description	Default	Broadcast_ID Support	Trigger Support	R/W
0x20	EXT_PRODUCT_ID	7:0	EXT_PRODUCT_ID	Extension to PRODUCT_ID in register 0x1D. This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	00000000	No	No	R
0x21	REV_ID	7:4	MAIN_REVISION	Chip main revision	0000	No	No	R
		3:0	SUB_REVISION	Chip sub revision	0000			
0x22	GSID	7:4	GSID0[3:0]	Primary Group Slave ID.	0000	No	No	R/W
		3:0	GSID1[3:0]	Secondary Group Slave ID.	0000			
0x23	UDR_RST	7	UDR_RST	Reset all configurable non-RFFE Reserved registers to default values. 0: Normal operation 1: Software reset	0	Yes	No	R/W
		6:0	RESERVED	Reserved for future use	0000000			
0x24	ERR_SUM	7	RESERVED	Reserved for future use	0	No	No	R
		6	COMMAND_FRAME_PARITY_ERR	Command Sequence received with parity error — discard command.	0			
		5	COMMAND_LENGTH_ERR	Command length error.	0			
		4	ADDRESS_FRAME_PARITY_ERR	Address frame with parity error.	0			
		3	DATA_FRAME_PARITY_ERR	Data frame with parity error.	0			
		2	READ_UNUSED_REG	Read command to an invalid address.	0			
		1	WRITE_UNUSED_REG	Write command to an invalid address.	0			
		0	BID_GID_ERR	Read command with a BROADCAST_ID or GROUP_ID.	0			
0x2B	BUS_LD	7:3	RESERVED	Reserved for future use	0x0	No	No	R/W
		2:0	BUS_LD[2:0]	Program the drive strength of the SDATA driver in readback modes. 0x0: 10 pF 0x1: 20 pF 0x2: 30 pF 0x3: 40 pF 0x4: 50 pF 0x5: 60 pF 0x6: 80 pF 0x7: 80 pF 0x8-0xF: reserved	0x4			

Table 14: Register mapping, table III

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID Support	Trigger support	R/W
0x2D	EXT_TRIG_MASK	7	TRIGGER_MASK_10	0: Data writes to registers tied to EXT_TRIGGER_10 are masked. Data is held in shadow registers until the EXT_TRIGGER_10 bit is set to 1.	1	No	No	R/W
				1: Data writes to registers tied to EXT_TRIGGER_10 are not masked. Data writes go directly to the active registers.				MW
		6	TRIGGER_MASK_9	0: Data writes to registers tied to EXT_TRIGGER_9 are masked. Data is held in shadow registers until the EXT_TRIGGER_9 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_9 are not masked. Data writes go directly to the active registers.				
		5	TRIGGER_MASK_8	0: Data writes to registers tied to EXT_TRIGGER_8 are masked. Data is held in shadow registers until the EXT_TRIGGER_8 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_8 are not masked. Data writes go directly to the active registers.				
		4	TRIGGER_MASK_7	0: Data writes to registers tied to EXT_TRIGGER_7 are masked. Data is held in shadow registers until the EXT_TRIGGER_7 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_7 are not masked. Data writes go directly to the active registers.				
		3	TRIGGER_MASK_6	0: Data writes to registers tied to EXT_TRIGGER_6 are masked. Data is held in shadow registers until the EXT_TRIGGER_6 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_6 are not masked. Data writes go directly to the active registers.				
		2	TRIGGER_MASK_5	0: Data writes to registers tied to EXT_TRIGGER_5 are masked. Data is held in shadow registers until the EXT_TRIGGER_5 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_5 are not masked. Data writes go directly to the active registers.				
		1	TRIGGER_MASK_4	0: Data writes to registers tied to EXT_TRIGGER_4 are masked. Data is held in shadow registers until the EXT_TRIGGER_4 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_4 are not masked. Data writes go directly to the active registers.				
		0	TRIGGER_MASK_3	0: Data writes to registers tied to EXT_TRIGGER_3 are masked. Data is held in shadow registers until the EXT_TRIGGER_3 bit is set to 1.	1			
				1: Data writes to registers tied to EXT_TRIGGER_3 are not masked. Data writes go directly to the active registers.				

Table 15: Register mapping, table IV

Register address	Register name	Data bits	Function	Description	Default	Broadcast_ID support	Trigger support	R/W
0x2E	EXT_TRIG	7	TRIGGER_10	0: No action. Data is held in shadow registers.	0	Yes	No	R/W
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_10				MW
		6	TRIGGER_9	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_9				
		5	TRIGGER_8	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_8				
		4	TRIGGER_7	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_7				
		3	TRIGGER_6	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_6				
		2	TRIGGER_5	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_5				
		1	TRIGGER_4	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_4				
		0	TRIGGER_3	0: No action. Data is held in shadow registers.	0			
				1: Data is transferred from shadow registers to active registers for refisters tied to EXT_TRIGGER_3				

Table 16: Default MIPI USID selection

Address	Symbol	External conditon at USID_SEL pin
USID=0110	Addr6	Ground
USID=0111	Addr7	to VIO
USID=1000	Addr8	Floating[1)]
USID=1001	Addr9	220 kΩ to VIO[1)]

[1)] Total capacitance on the USID_SEL pin must be <5 pF.

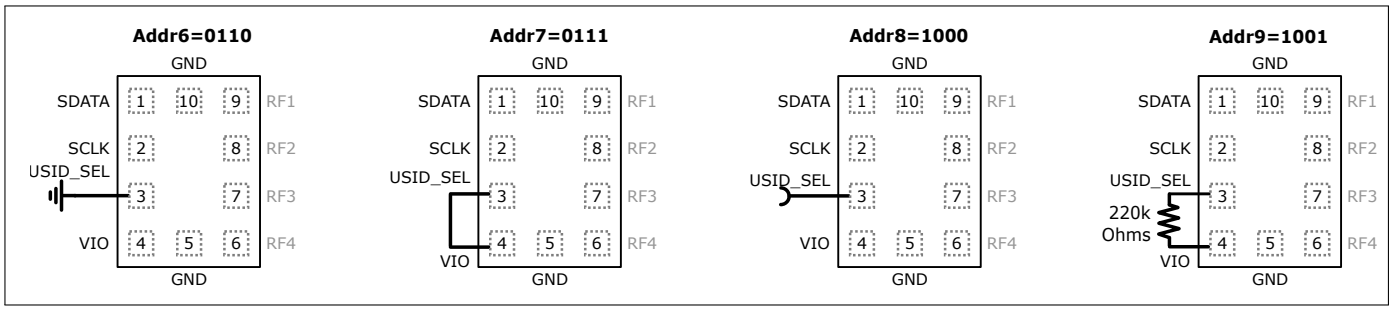

Figure 3: BGSA403ML10 USID_SEL pin configuration

Warning: Register_0 and Register_1 RF switch control bits are identical. Writing both registers Register_0 and Register_1 simultaneously will lead to undefined behavior. The unused register (Register_0 or Register_1) must remain 0x00.

Table 17: Modes of operation (Truth table, Register_0)

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL OFF (Isolation)	x	x	x	x	0	0	0	0
1	RF1 ON	x	x	x	x	0	0	0	1
2	RF2 ON	x	x	x	x	0	0	1	0
3	RF1+RF2 ON	x	x	x	x	0	0	1	1
4	RF3 ON	x	x	x	x	0	1	0	0
5	RF1+RF3 ON	x	x	x	x	0	1	0	1
6	RF2+RF3 ON	x	x	x	x	0	1	1	0
7	RF1+RF2+RF3 ON	x	x	x	x	0	1	1	1
8	RF4 ON	x	x	x	x	1	0	0	0
9	RF1+RF4 ON	x	x	x	x	1	0	0	1
10	RF2+RF4 ON	x	x	x	x	1	0	1	0
11	RF1+RF2+RF4 ON	x	x	x	x	1	0	1	1
12	RF3+RF4 ON	x	x	x	x	1	1	0	0
13	RF1+RF3+RF4 ON	x	x	x	x	1	1	0	1
14	RF2+RF3+RF4 ON	x	x	x	x	1	1	1	0
15	RF1+RF2+RF3+RF4 ON	x	x	x	x	1	1	1	1

[1] Do not care, x = 0 or 1

Table 18: Modes of operation (Truth table, Register_1)

State	Mode	D7	D6	D5	D4	D3	D2	D1	D0
0	ALL OFF (Isolation)	x	x	x	x	0	0	0	0
1	RF1 ON	x	x	x	x	0	0	0	1
2	RF2 ON	x	x	x	x	0	0	1	0
3	RF1+RF2 ON	x	x	x	x	0	0	1	1
4	RF3 ON	x	x	x	x	0	1	0	0
5	RF1+RF3 ON	x	x	x	x	0	1	0	1
6	RF2+RF3 ON	x	x	x	x	0	1	1	0
7	RF1+RF2+RF3 ON	x	x	x	x	0	1	1	1
8	RF4 ON	x	x	x	x	1	0	0	0
9	RF1+RF4 ON	x	x	x	x	1	0	0	1
10	RF2+RF4 ON	x	x	x	x	1	0	1	0
11	RF1+RF2+RF4 ON	x	x	x	x	1	0	1	1
12	RF3+RF4 ON	x	x	x	x	1	1	0	0
13	RF1+RF3+RF4 ON	x	x	x	x	1	1	0	1
14	RF2+RF3+RF4 ON	x	x	x	x	1	1	1	0
15	RF1+RF2+RF3+RF4 ON	x	x	x	x	1	1	1	1

[1] Do not care, x = 0 or 1

6 Application information

Pin configuration and function

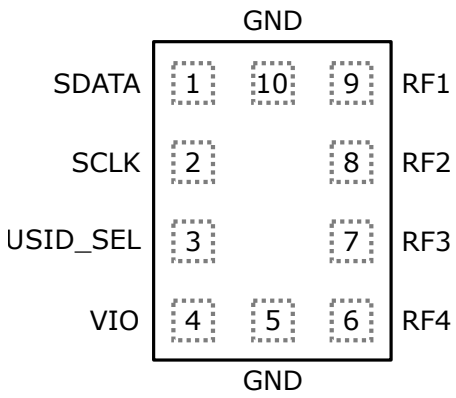

Figure 4: BGSA403ML10 pin configuration (top view)

Table 19: Pin definition and function

Pin No.	Name	Function
1	SDATA	MIPI RFFE data Input / Output
2	SCLK	MIPI RFFE clock Input
3	USID_SEL	USID default address selection pin (see table 16)
4	VIO	Voltage supply compatible with MIPI RFFE specification
5	GND	Ground
6	RF4	RF4 port
7	RF3	RF3 port
8	RF2	RF2 port
9	RF1	RF1 port
10	GND	Ground

Evaluation board description

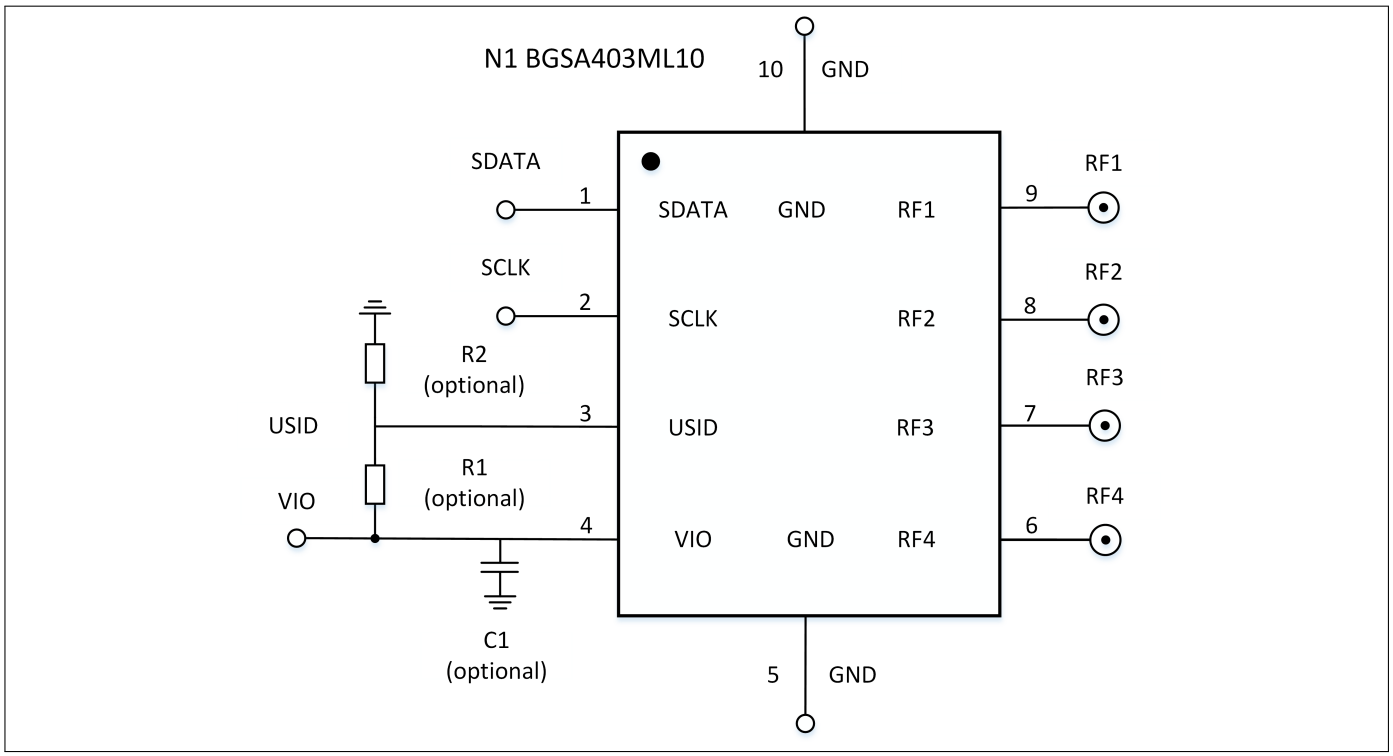

Figure 5: BGSA403ML10 application schematic

Table 20: Bill of materials table

Name	Part type	Package	Manufacturer	Function
C1 (1nF optional)[1)]	Capacitor	0402	Various	De-coupling capacitor
N1	BGSA403ML10	TSLP-10-3	Infineon	Antenna tuner
R1 (do not place) R2 (0 Ohm)	Resistor	0402	Various	Set USID default address to 6 (GND)
R1 (0 Ohm) R2 (do not place)	Resistor	0402	Various	Set USID default address to 7 (VIO)
R1 (do not place) R2 (do not place)	Resistor	0402	Various	Set USID default address to 8 (Floating)
R1 (220 kOhm) R2 (do not place)	Resistor	0402	Various	Set USID default address to 9 (220 kOhm to VIO)

[1)] This capacitor is optional and value is only indicative. Decoupling capacitor value has to be chosen in order VIO ramp-up time is within MIPI RFFE version v2.1 specification

7 Package information

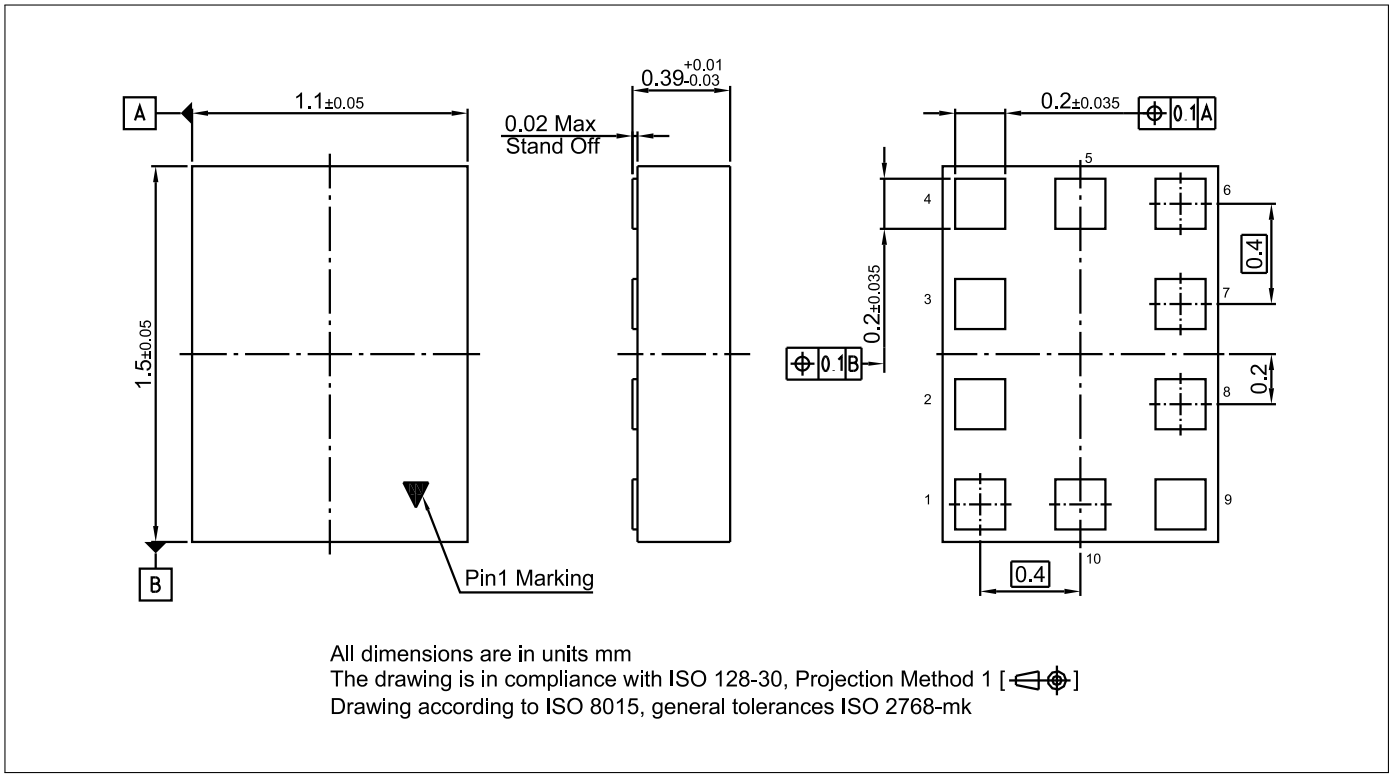

Figure 6: TSLP-10-3 package outline (top, side and bottom views)

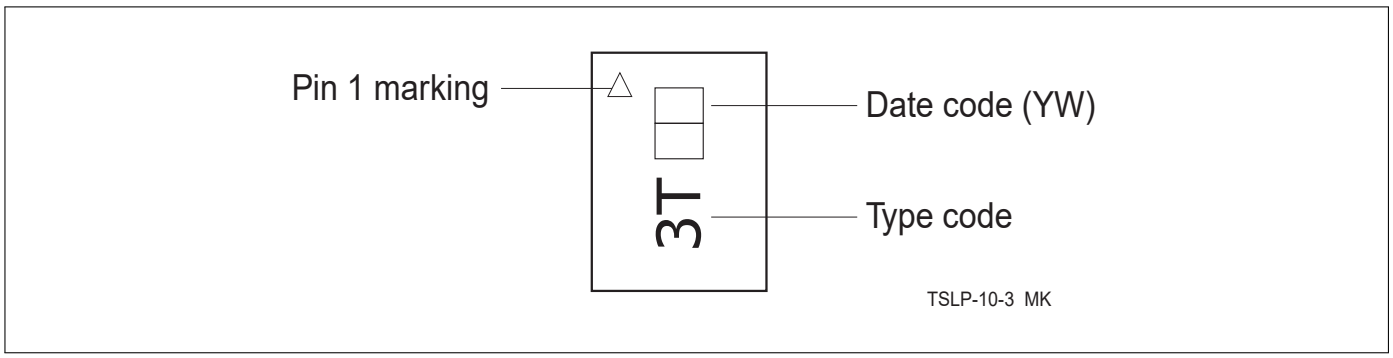

Figure 7: Marking specification (top view): date code digits Y and W defined in table 21/22

Table 21: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2010	0	2020	0	2030	0
2011	1	2021	1	2031	1
2012	2	2022	2	2032	2
2013	3	2023	3	2033	3
2014	4	2024	4	2034	4
2015	5	2025	5	2035	5
2016	6	2026	6	2036	6
2017	7	2027	7	2037	7
2018	8	2028	8	2038	8
2019	9	2029	9	2039	9

Table 22: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s	53	M
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

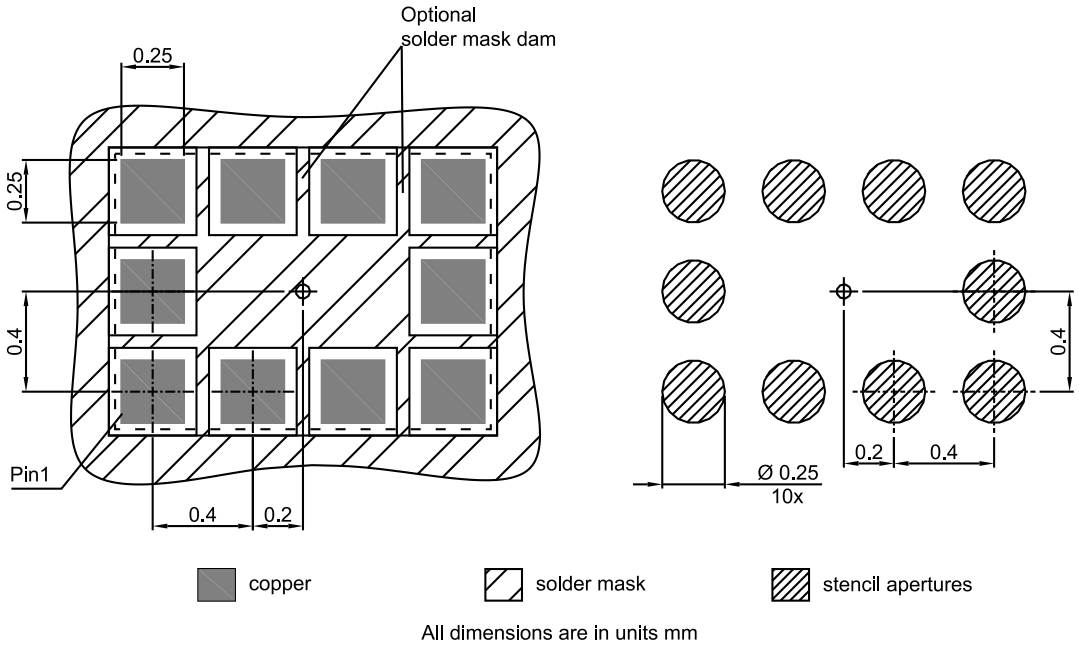

Figure 8: Footprint recommendation

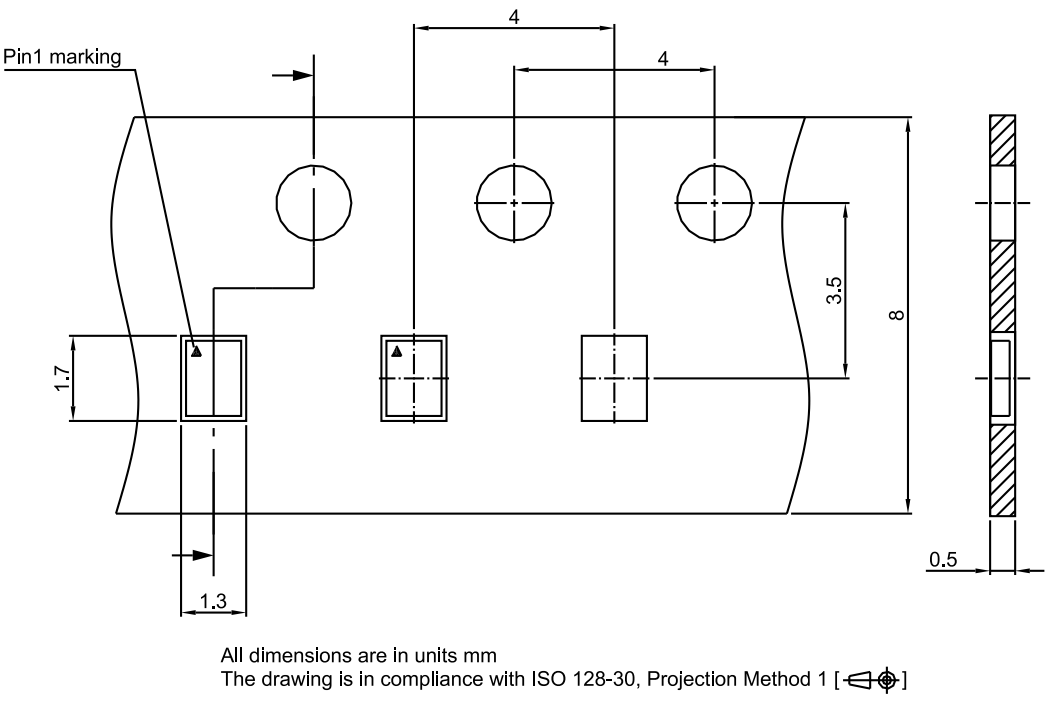

Figure 9: TSLP-10-3 carrier tape

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.1, 2022-02-08	
Title page	Package drawing added

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