



# BUK9M31-60EL

Single N-channel 60 V, 21 mOhm logic level MOSFET in LFPAK33 using Enhanced SOA technology

9 May 2022

Product data sheet

## 1. General description

Single, logic level, N-channel MOSFET in LFPAK33 using Application specific (ASFET) Enhanced SOA technology. This product has been designed and qualified to AEC-Q101 for use in linear mode in airbag applications.

## 2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Enhanced SOA technology for improved linear mode performance
- LFPAK copper clip package technology:
  - High robustness and current handling capability
  - Gull wing leads for easy AOI inspection and exceptional board level reliability

## 3. Applications

- 12 V automotive systems
- Airbag squib voltage regulator MOSFET

## 4. Quick reference data

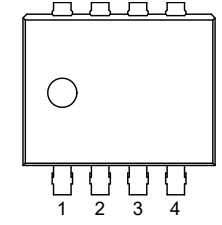
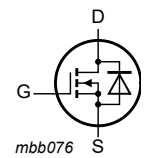
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	60	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	-	35	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	62	W
<b>Static characteristics</b>							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 12</a>		11.6	16.5	20.6	mΩ
<b>Dynamic characteristics</b>							
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	6	12	nC

[1] 35 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	Mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9M31-60EL	LFAK33	Plastic, single ended surface mounted package (LFAK33); 8 leads; 0.65 mm pitch	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9M31-60EL	9316EL

## 8. Limiting values

Table 5. Limiting values

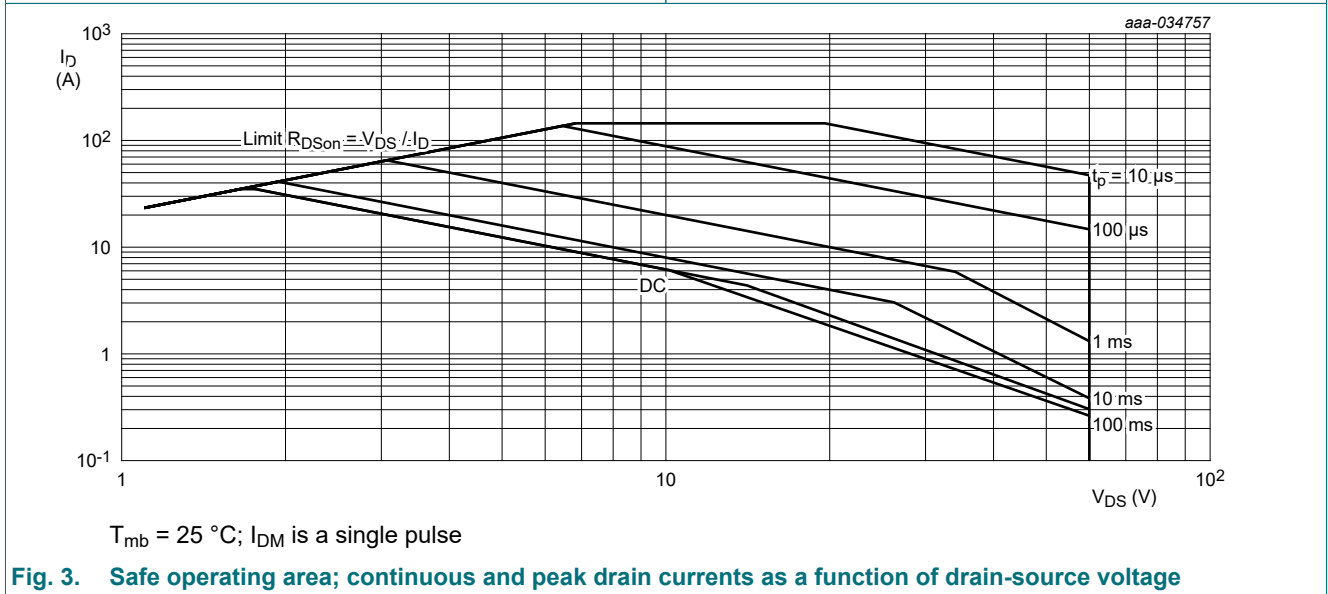
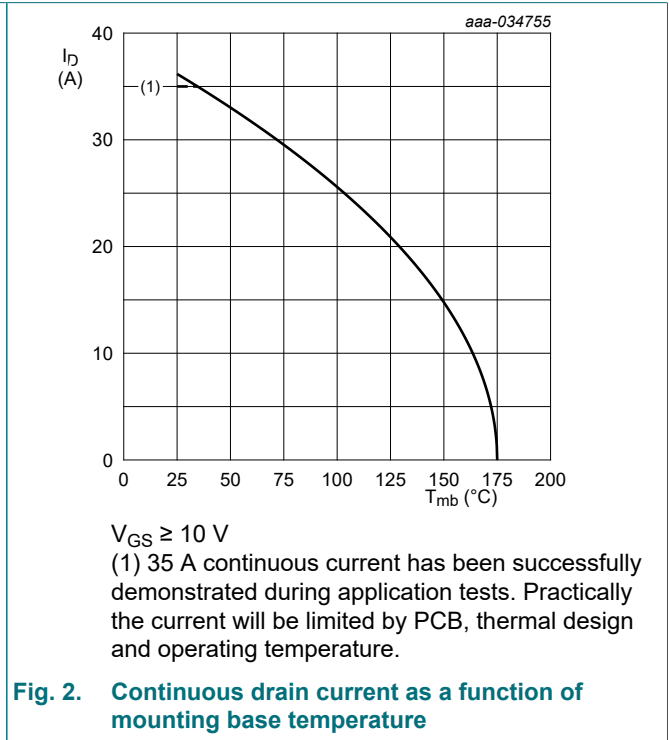
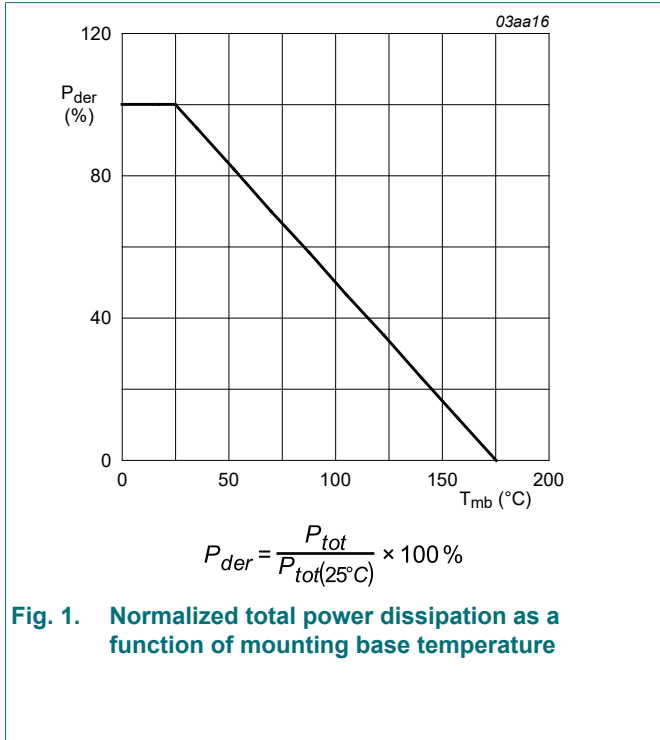
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ °C}$  unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	60	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ °C}$		-10	10	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1		-	62	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	[1]	-	35	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2		-	25.6	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3; Fig. 4		-	145	A
$T_{stg}$	storage temperature			-55	175	°C
$T_j$	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	35	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	145	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 27.3\text{ A}$ ; $V_{sup} \leq 60\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 36\text{ }\mu\text{s}$ ; Fig. 5	[2] [3]	-	40.4	mJ

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Symbol	Parameter	Conditions		Min	Max	Unit
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 60\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $R_{GS} = 50\text{ }\Omega$ ; Fig. 5	[2] [3] [4]	-	27.3	A

- [1] 35 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test.



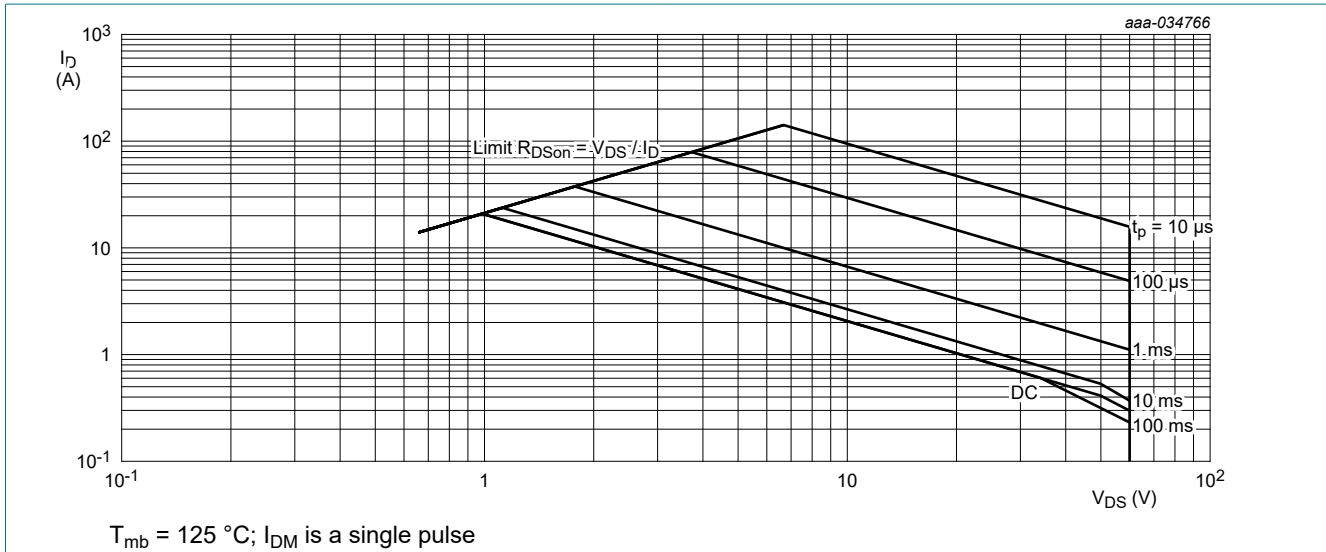


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

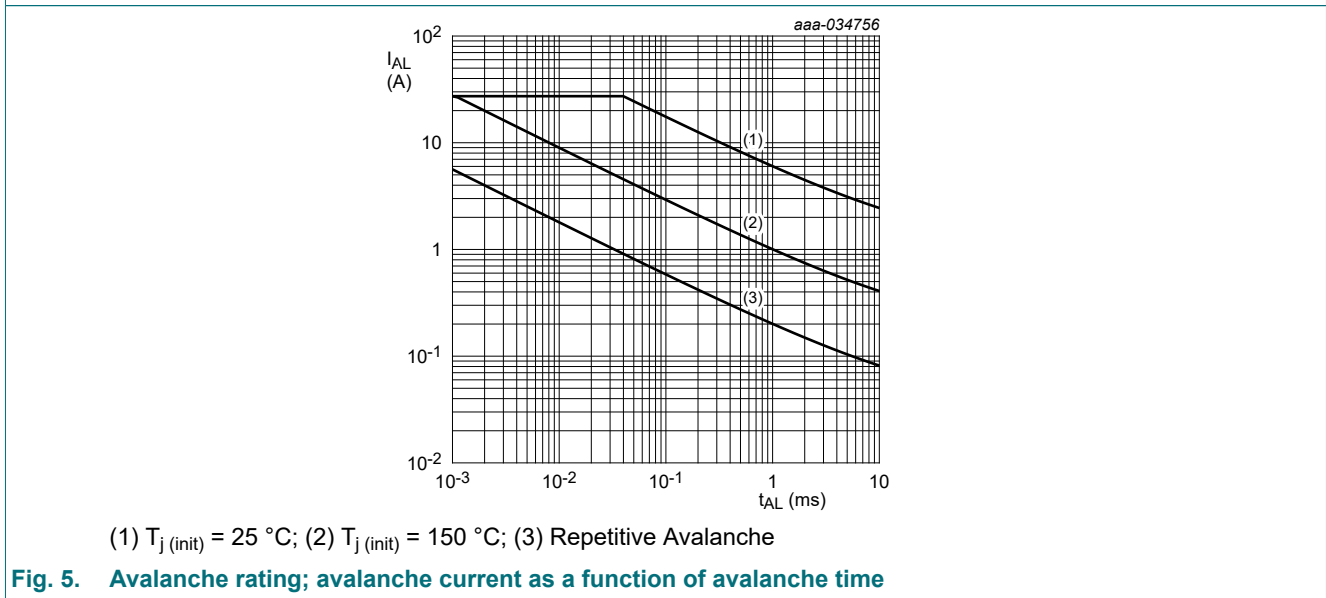


Fig. 5. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 6</a>	-	2.01	2.43	K/W

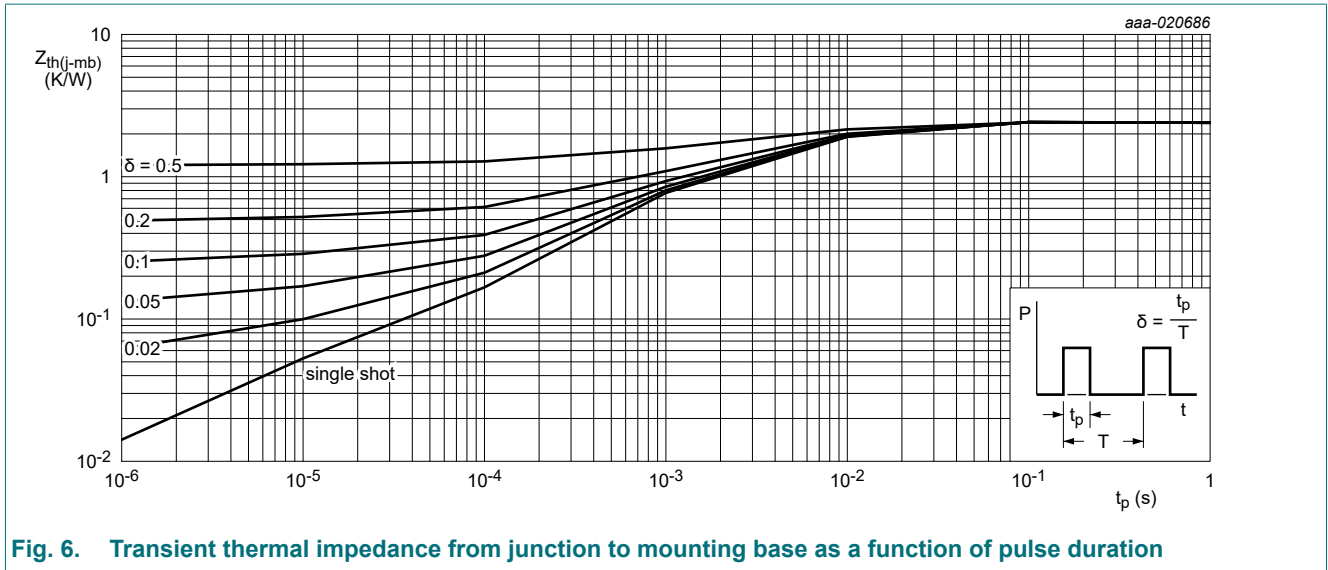


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

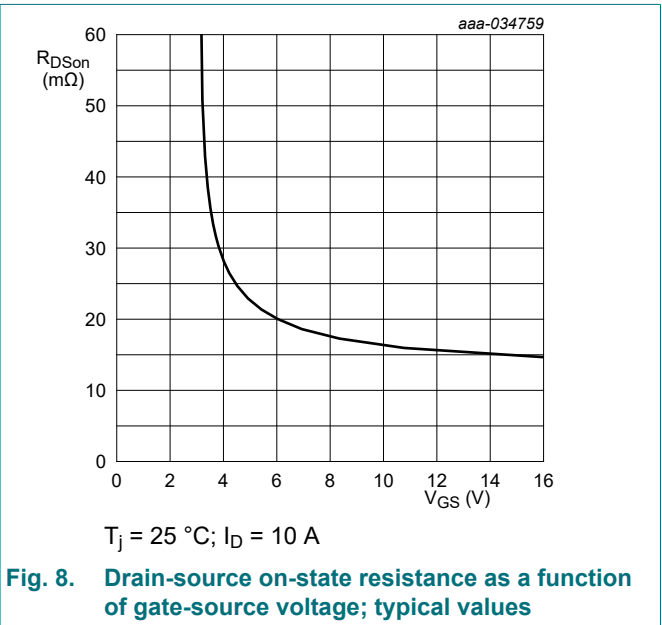
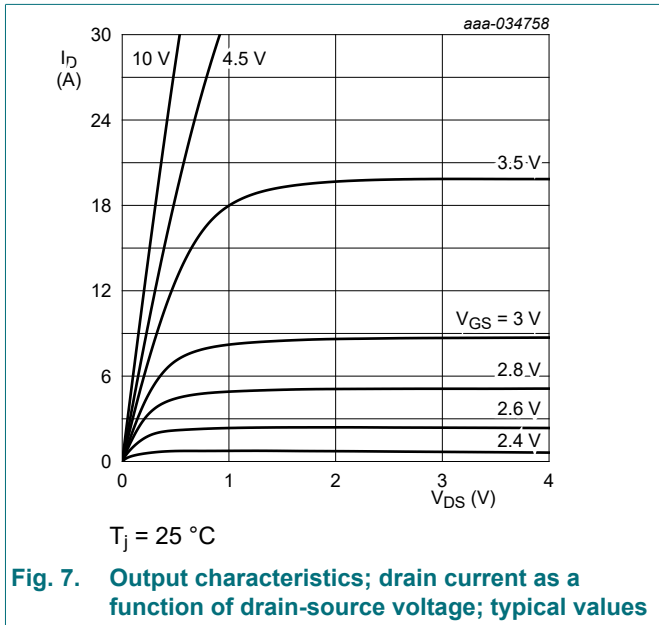
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	66	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	62	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	61	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 10}; \text{ Fig. 11}$	1.4	1.82	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 11}$	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 11}$	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	21	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 12}$	11.6	16.5	20.6	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 105 \text{ }^\circ C; \text{ Fig. 13}$	17.6	26	33.5	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 125 \text{ }^\circ C; \text{ Fig. 13}$	19.3	28.7	37.2	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 13}$	23.8	36	47.3	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 12}$	17.3	24.7	33	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 105 \text{ }^\circ C; \text{ Fig. 13}$	26	38	53	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 125 \text{ }^\circ C; \text{ Fig. 13}$	28	42	58	m $\Omega$
		$V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 13}$	34	52	73	m $\Omega$

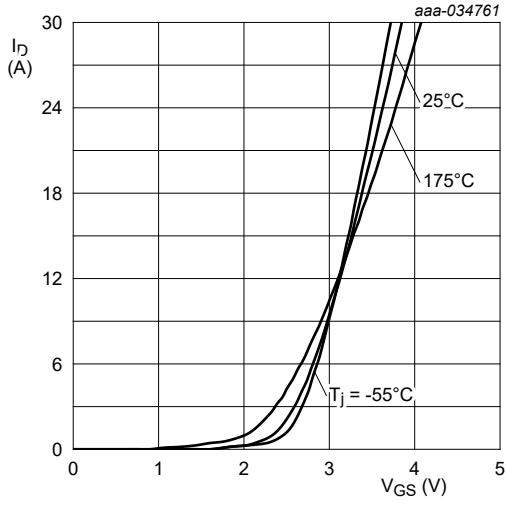
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	1.85	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 14}; \text{Fig. 15}$	-	13	18	nC
		$I_D = 10 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 14}; \text{Fig. 15}$	-	26	37	nC
$Q_{GS}$	gate-source charge	$I_D = 10 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 14}; \text{Fig. 15}$	-	3.7	5.5	nC
$Q_{GD}$	gate-drain charge		-	6	12	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 16}$	-	1334	1867	pF
$C_{oss}$	output capacitance		-	135	162	pF
$C_{rss}$	reverse transfer capacitance		-	79	108	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 48 \text{ V}; R_L = 5 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(\text{ext})} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	8	-	ns
$t_r$	rise time		-	18	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	17	-	ns
$t_f$	fall time		-	13	-	ns
$g_{fs}$	transfer conductance	$V_{DS} = 8 \text{ V}; I_D = 10 \text{ A}; \text{Fig. 17}$	-	24	-	S
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 18}$	-	0.83	1	V
$t_{rr}$	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 19}$	-	26	-	ns
$Q_r$	recovered charge		[1]	28.5	-	nC

[1] includes capacitive recovery

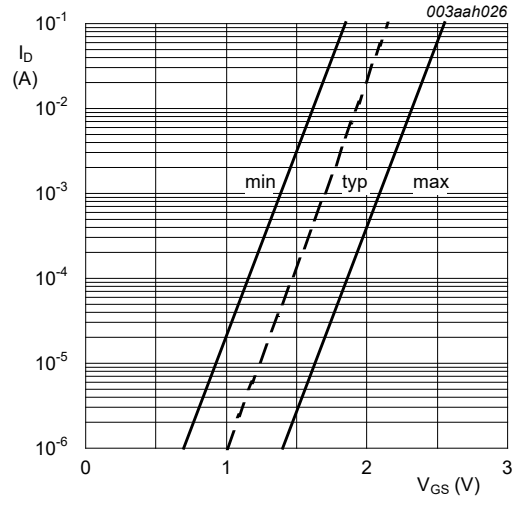


Single N-channel 60 V, 21 mOhm logic level MOSFET in LPAK33 using Enhanced SOA technology



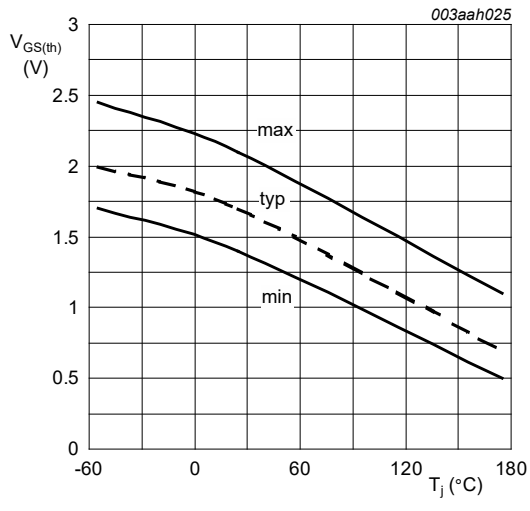
$V_{DS} = 8 \text{ V}$

**Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



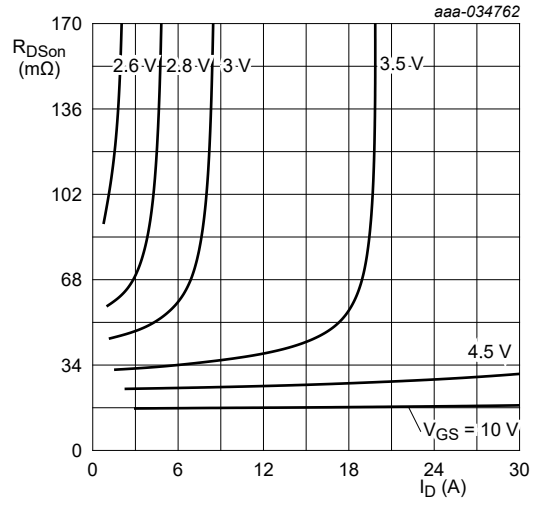
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**



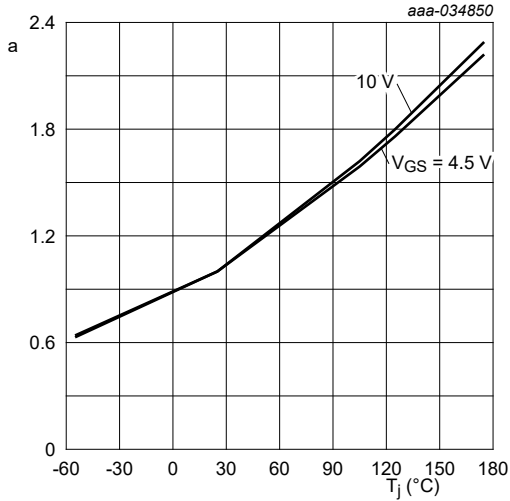
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig. 11. Gate-source threshold voltage as a function of junction temperature**



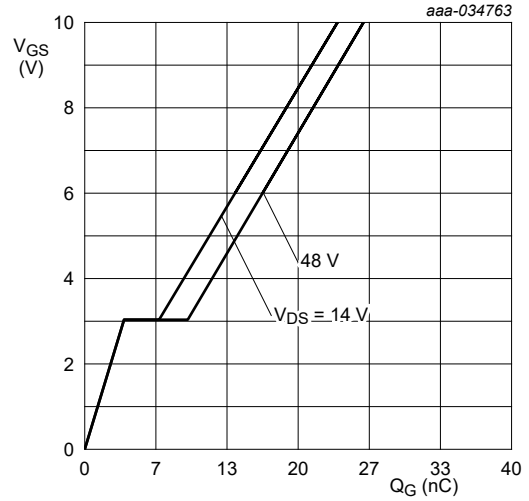
$T_j = 25 \text{ }^\circ\text{C}$

**Fig. 12. Drain-source on-state resistance as a function of drain current; typical values**



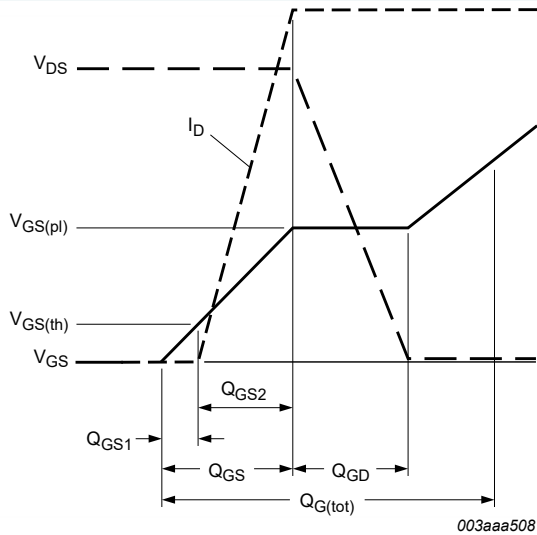
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

**Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

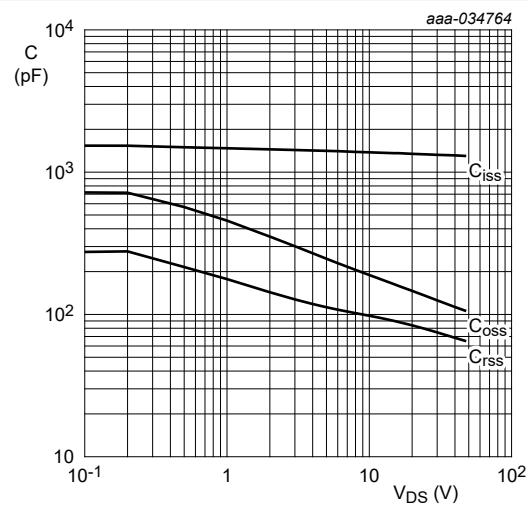


$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**



**Fig. 15. Gate charge waveform definitions**

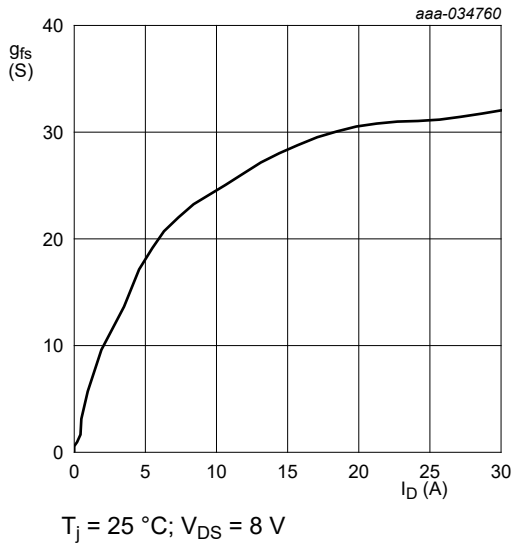


$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

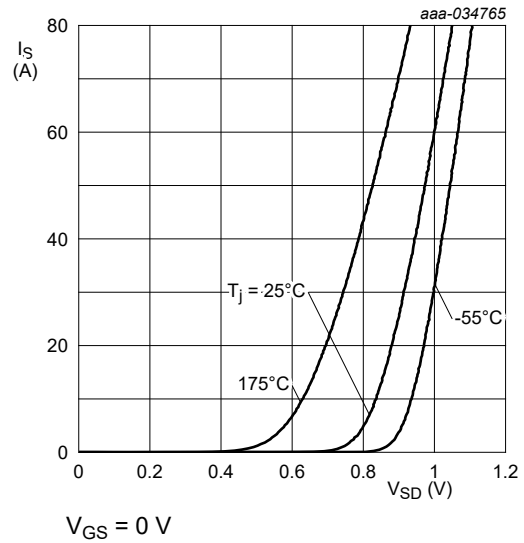
**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



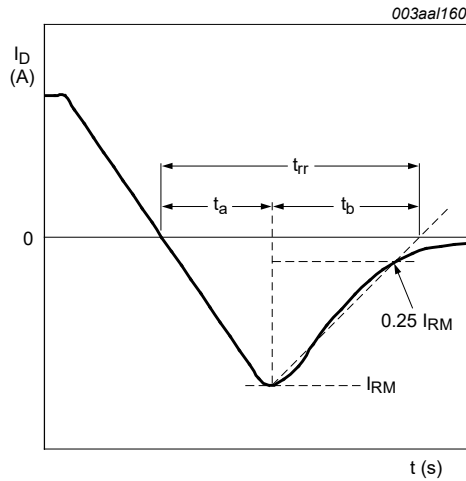
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**Fig. 17. Forward transconductance as a function of drain current; typical values**



**Fig. 18. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**



**Fig. 19. Reverse recovery timing definition**

### 11. Package outline

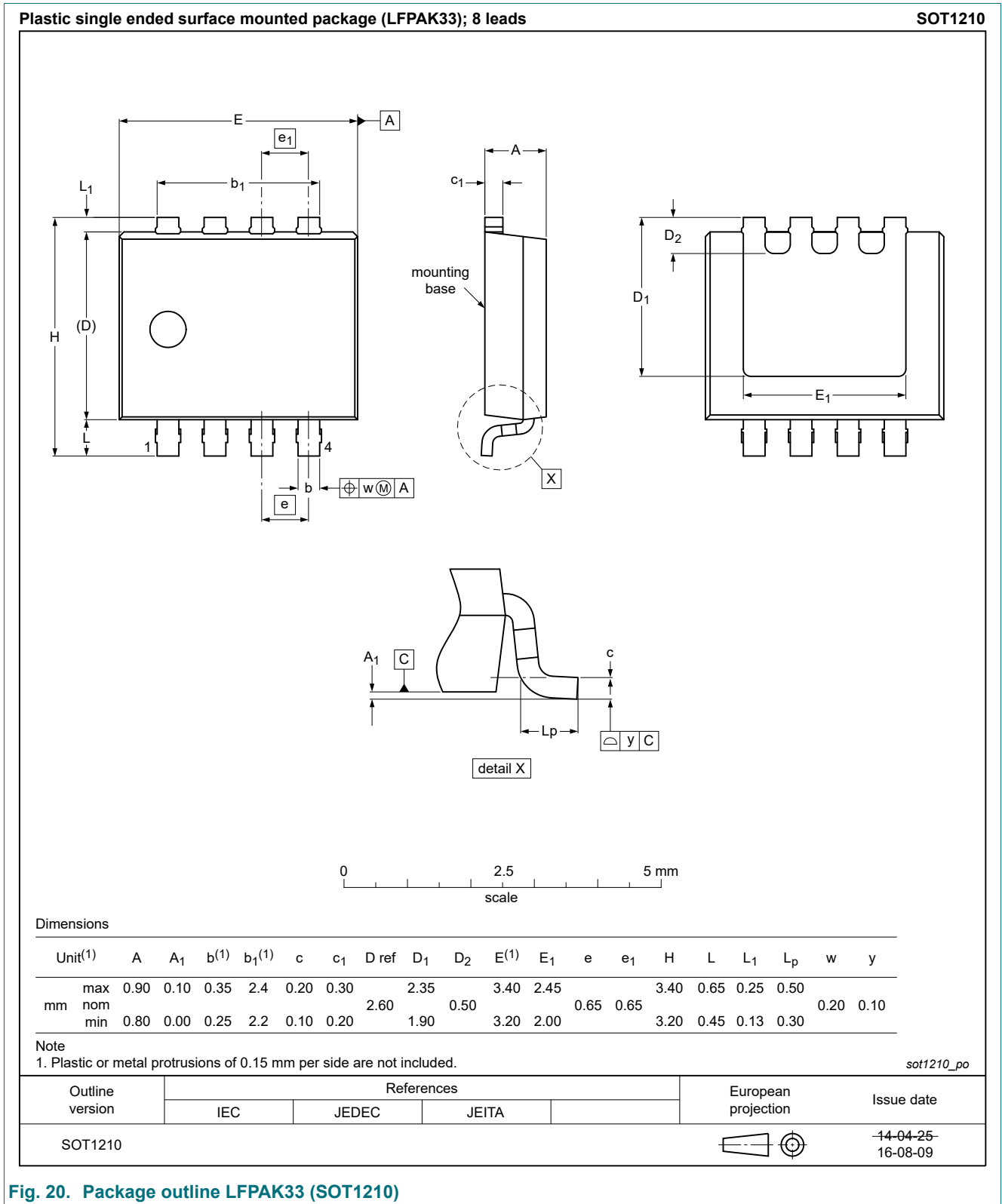


Fig. 20. Package outline LPAK33 (SOT1210)

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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