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U\_J2  
J2.SchDoc

U\_J3  
J3.SchDoc

U\_J4  
J4.SchDoc

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DDR4-TERM.SchDoc

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B64.SchDoc

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B65.SchDoc

U\_B66  
B66.SchDoc

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Clock.SchDoc

U\_CONFIG  
CONFIG.SchDoc

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DDR4-RAM\_2.SchDoc

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U\_DDR4-RAM\_4  
DDR4-RAM\_4.SchDoc

U\_DDR4-TERM  
DDR4-TERM.SchDoc

U\_ZU\_POWER  
ZU\_POWER.SchDoc

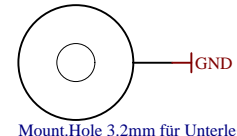
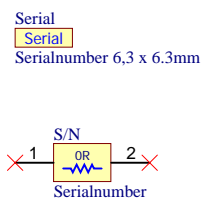
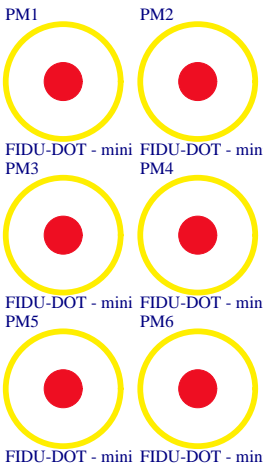
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ZU\_PS\_POWER.SchDoc

U\_POWER  
POWER.SchDoc

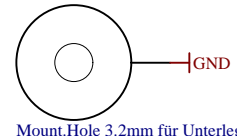
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POWER\_2.SchDoc

U\_POWER\_4  
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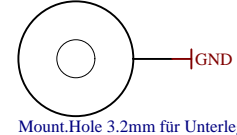
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Revision\_Changes.SchDoc



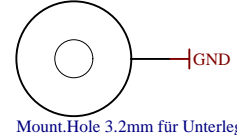
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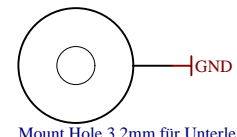
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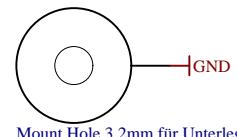
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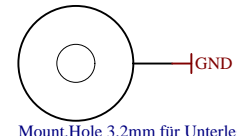
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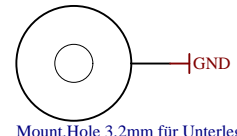
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Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



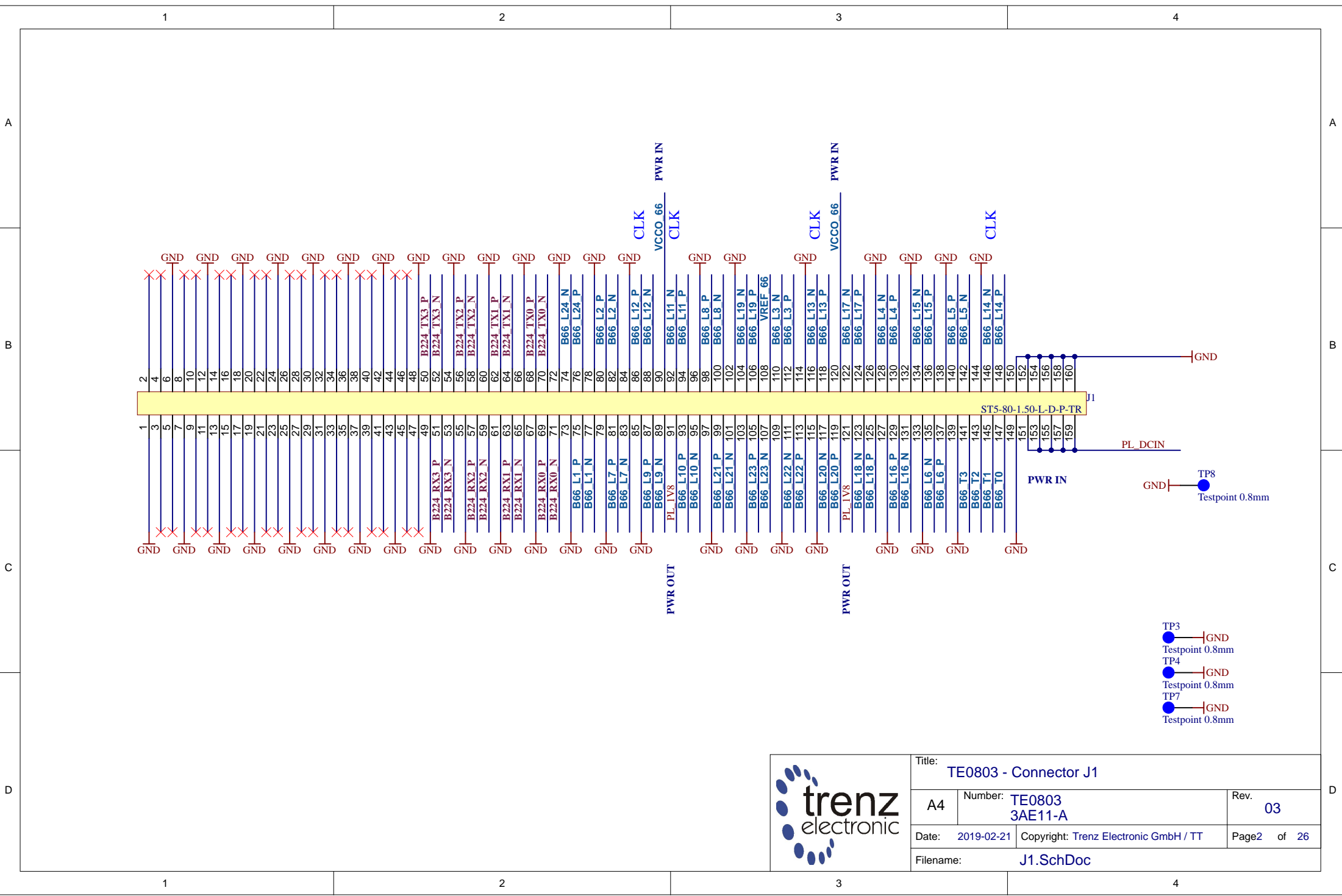
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A4	Number: <b>TE0803 3AE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page1 of 26
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Title: TE0803 - Connector J1		
A4	Number: TE0803 3AE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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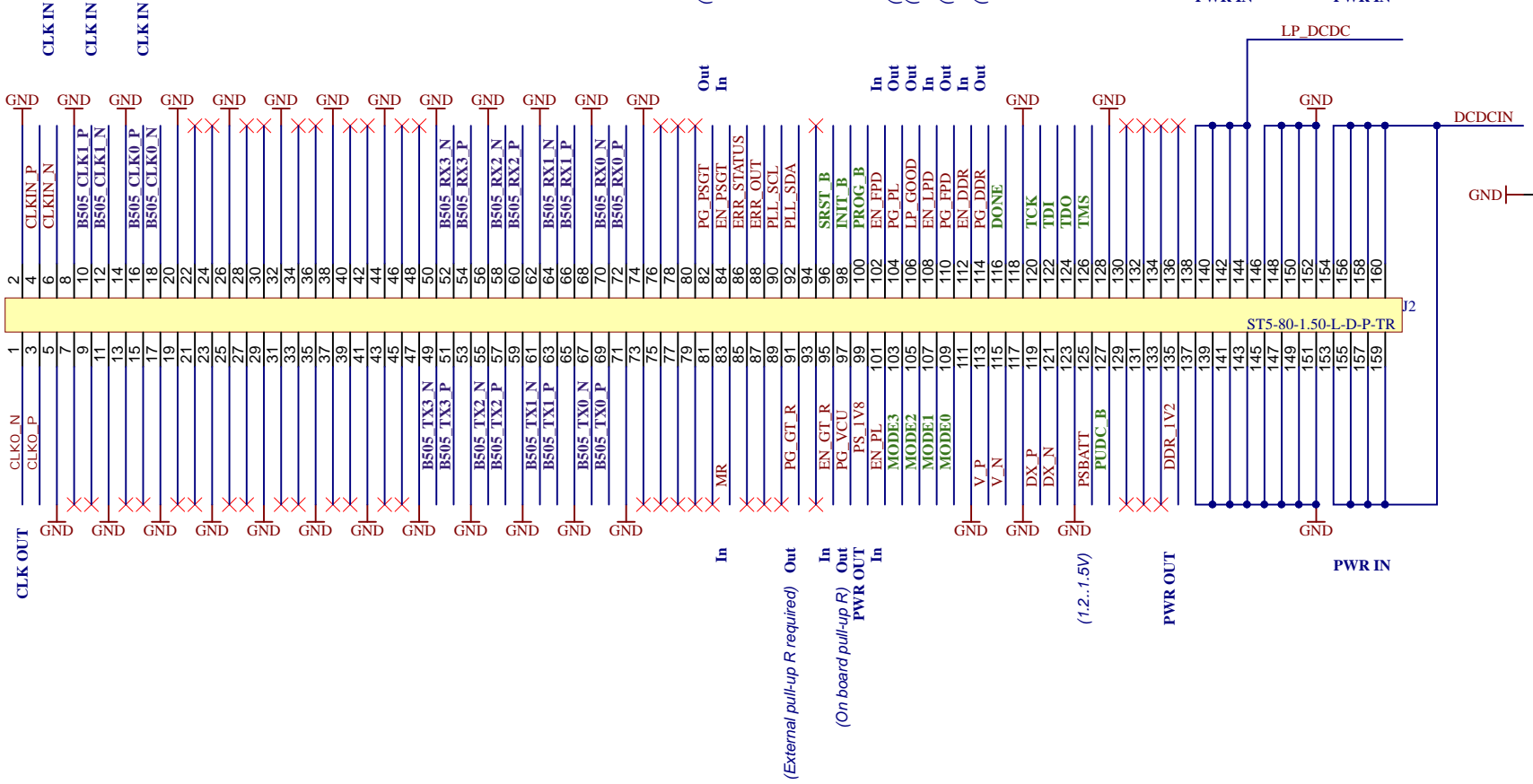

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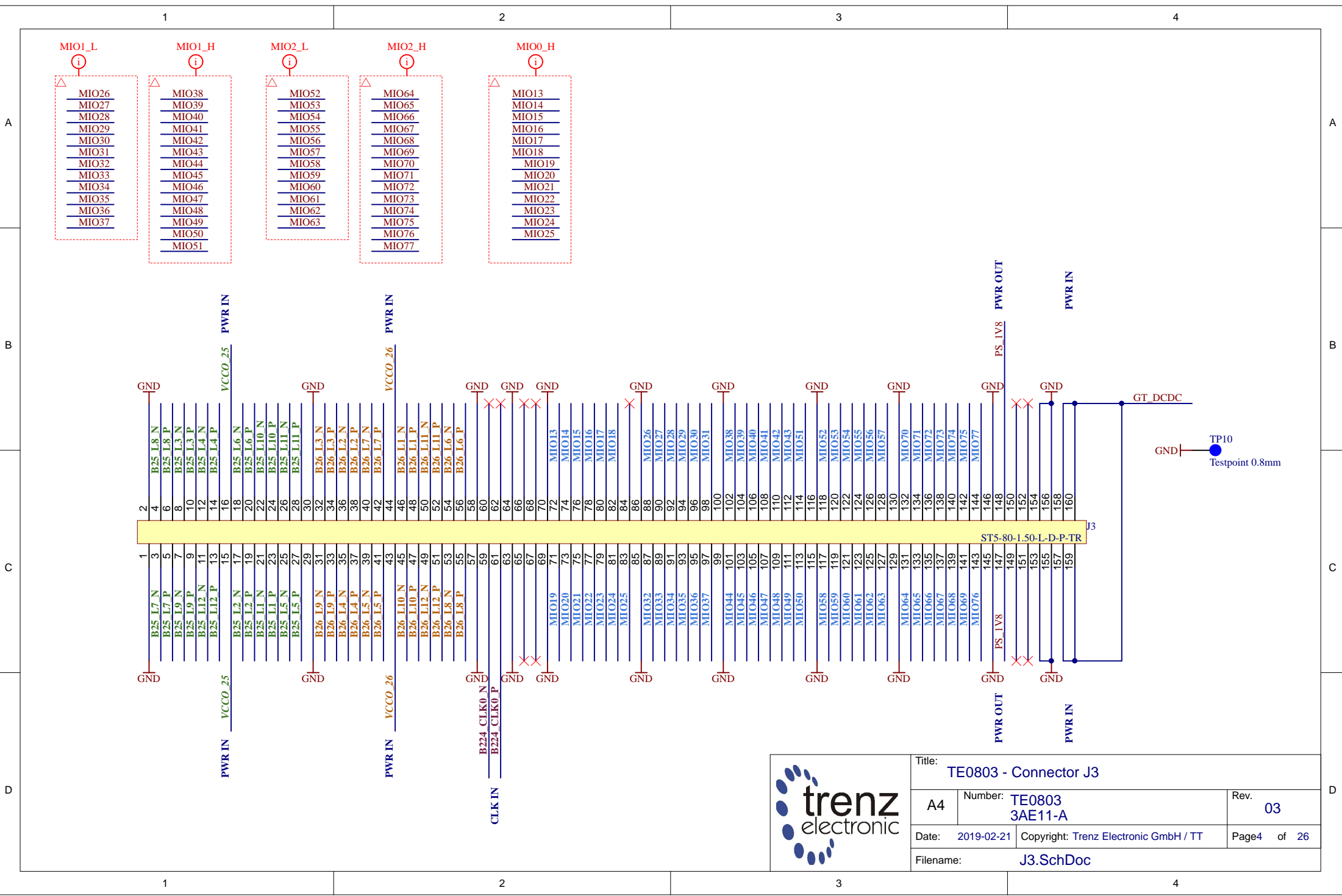
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page3 of 26
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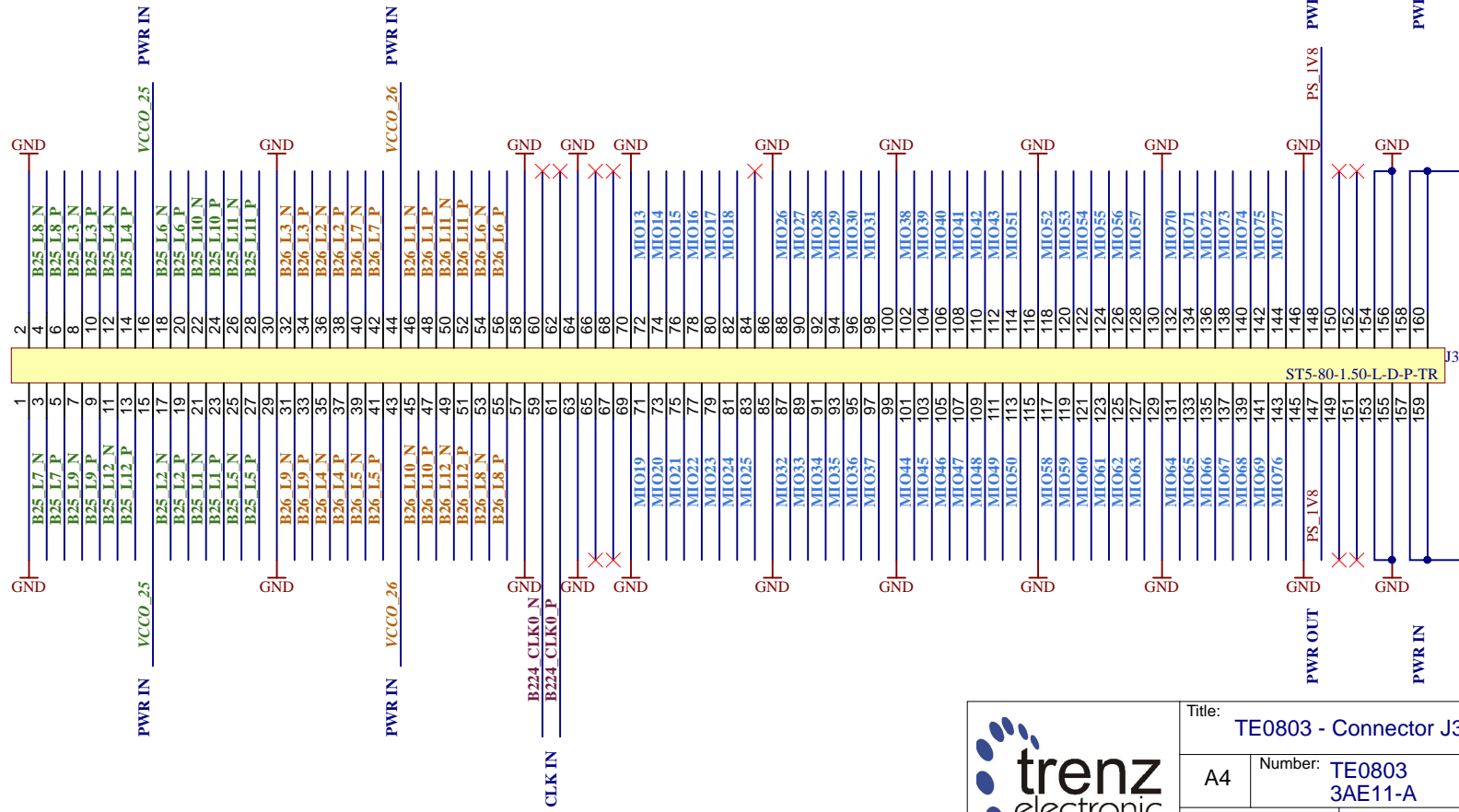
- MIO1\_L**
- MIO26
  - MIO27
  - MIO28
  - MIO29
  - MIO30
  - MIO31
  - MIO32
  - MIO33
  - MIO34
  - MIO35
  - MIO36
  - MIO37


- MIO1\_H**
- MIO38
  - MIO39
  - MIO40
  - MIO41
  - MIO42
  - MIO43
  - MIO44
  - MIO45
  - MIO46
  - MIO47
  - MIO48
  - MIO49
  - MIO50
  - MIO51

- MIO2\_L**
- MIO52
  - MIO53
  - MIO54
  - MIO55
  - MIO56
  - MIO57
  - MIO58
  - MIO59
  - MIO60
  - MIO61
  - MIO62
  - MIO63

- MIO2\_H**
- MIO64
  - MIO65
  - MIO66
  - MIO67
  - MIO68
  - MIO69
  - MIO70
  - MIO71
  - MIO72
  - MIO73
  - MIO74
  - MIO75
  - MIO76
  - MIO77

- MIO0\_H**
- MIO13
  - MIO14
  - MIO15
  - MIO16
  - MIO17
  - MIO18
  - MIO19
  - MIO20
  - MIO21
  - MIO22
  - MIO23
  - MIO24
  - MIO25



			Title: TE0803 - Connector J3	
			A4	Number: TE0803 3AE11-A
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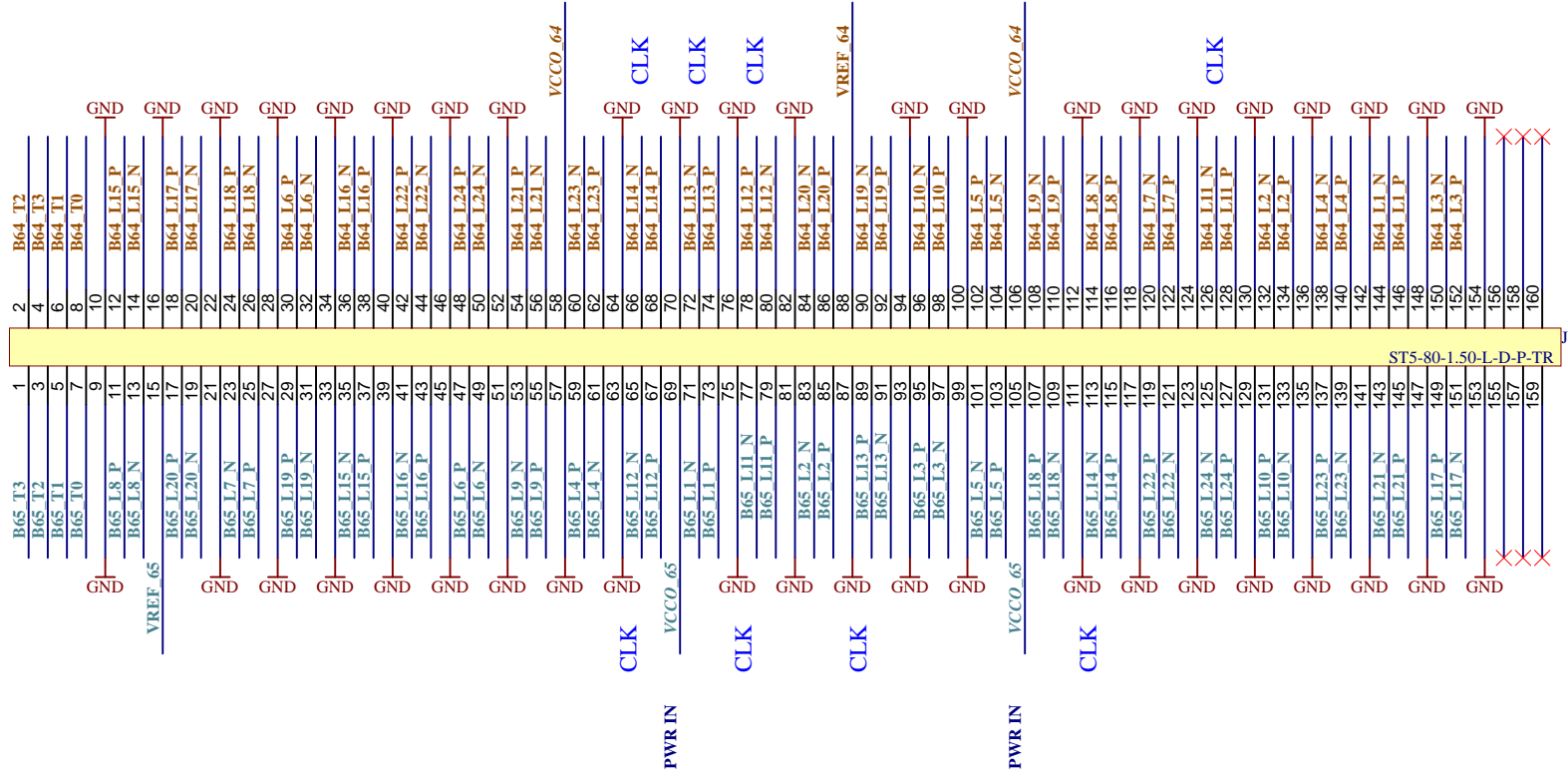
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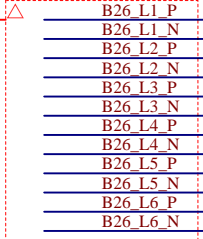
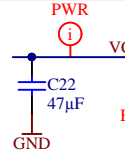
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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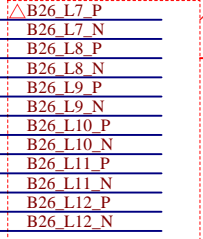
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**U1C XCZU3CG-1SFVC784E**

**BANK 26 HD (ZU4/5 BANK 46 HD)**

F14	VCCO_26		
C15	VCCO_26		
B15	IO_L1P_AD11P_26	IO_L7P_HDGC_AD5P_26	G13
A15	IO_L1N_AD11N_26	IO_L7N_HDGC_AD5N_26	F13
B14	IO_L2P_AD10P_26	IO_L8P_HDGC_AD4P_26	F15
A14	IO_L2N_AD10N_26	IO_L8N_HDGC_AD4N_26	E15
B13	IO_L3P_AD9P_26	IO_L9P_AD3P_26	G15
A13	IO_L3N_AD9N_26	IO_L9N_AD3N_26	G14
C14	IO_L4P_AD8P_26	IO_L10P_AD2P_26	H14
C13	IO_L4N_AD8N_26	IO_L10N_AD2N_26	H13
D15	IO_L5P_HDGC_AD7P_26	IO_L11P_AD1P_26	K14
D14	IO_L5N_HDGC_AD7N_26	IO_L11N_AD1N_26	J14
E14	IO_L6P_HDGC_AD6P_26	IO_L12P_AD0P_26	L14
E13	IO_L6N_HDGC_AD6N_26	IO_L12N_AD0N_26	L13



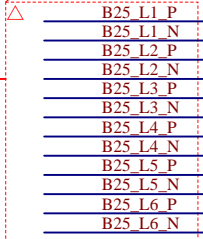
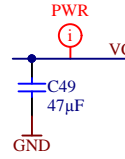
**BANK 44 HD (ZU4/5 BANK 43 HD)**

AC10	VCCO_44		
AG12	VCCO_44		
AG10	IO_L1P_AD11P_44	IO_L7P_HDGC_AD5P_44	AD11
AH10	IO_L1N_AD11N_44	IO_L7N_HDGC_AD5N_44	AD10
AF11	IO_L2P_AD10P_44	IO_L8P_HDGC_AD4P_44	AB11
AG11	IO_L2N_AD10N_44	IO_L8N_HDGC_AD4N_44	AC11
AH12	IO_L3P_AD9P_44	IO_L9P_AD3P_44	AA11
AH11	IO_L3N_AD9N_44	IO_L9N_AD3N_44	AA10
AE10	IO_L4P_AD8P_44	IO_L10P_AD2P_44	W10
AF10	IO_L4N_AD8N_44	IO_L10N_AD2N_44	Y10
AE12	IO_L5P_HDGC_AD7P_44	IO_L11P_AD1P_44	Y9
AF12	IO_L5N_HDGC_AD7N_44	IO_L11N_AD1N_44	AA8
AC13	IO_L6P_HDGC_AD6P_44	IO_L12P_AD0P_44	AB10
AD12	IO_L6N_HDGC_AD6N_44	IO_L12N_AD0N_44	AB9

**U1B**

**BANK 24 HD (ZU4/5 BANK 44 HD)**

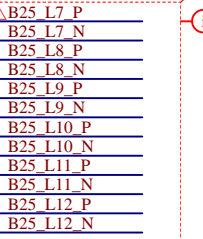
AA14	VCCO_24		
AD13	VCCO_24		
AE15	IO_L1P_AD15P_24	IO_L7P_HDGC_24	AA13
AE14	IO_L1N_AD15N_24	IO_L7N_HDGC_24	AB13
AG14	IO_L2P_AD14P_24	IO_L8P_HDGC_24	AB15
AH14	IO_L2N_AD14N_24	IO_L8N_HDGC_24	AB14
AG13	IO_L3P_AD13P_24	IO_L9P_AD11P_24	W14
AH13	IO_L3N_AD13N_24	IO_L9N_AD11N_24	W13
AE13	IO_L4P_AD12P_24	IO_L10P_AD10P_24	Y14
AF13	IO_L4N_AD12N_24	IO_L10N_AD10N_24	Y13
AD15	IO_L5P_HDGC_24	IO_L11P_AD9P_24	W12
AD14	IO_L5N_HDGC_24	IO_L11N_AD9N_24	W11
AC14	IO_L6P_HDGC_24	IO_L12P_AD8P_24	Y12
AC13	IO_L6N_HDGC_24	IO_L12N_AD8N_24	AA12



**XCZU3CG-1SFVC784E**

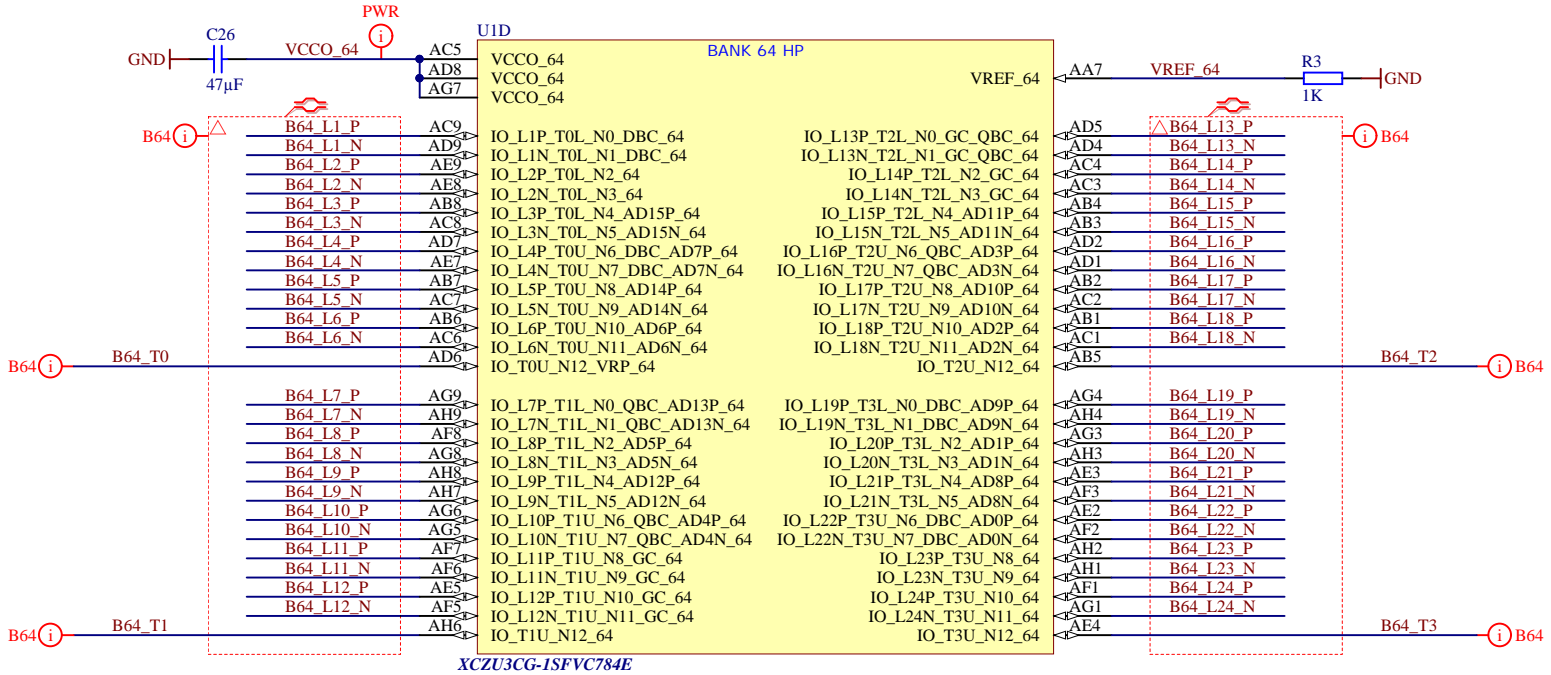
**BANK 25 HD (ZU4/5 BANK 45 HD)**

B12	VCCO_25		
E11	VCCO_25		
J11	IO_L1P_AD15P_25	IO_L7P_HDGC_25	E10
J10	IO_L1N_AD15N_25	IO_L7N_HDGC_25	D10
K13	IO_L2P_AD14P_25	IO_L8P_HDGC_25	E12
K12	IO_L2N_AD14N_25	IO_L8N_HDGC_25	D11
H11	IO_L3P_AD13P_25	IO_L9P_AD11P_25	C11
G10	IO_L3N_AD13N_25	IO_L9N_AD11N_25	B10
J12	IO_L4P_AD12P_25	IO_L10P_AD10P_25	B11
H12	IO_L4N_AD12N_25	IO_L10N_AD10N_25	A10
G11	IO_L5P_HDGC_25	IO_L11P_AD9P_25	A12
F11	IO_L5N_HDGC_25	IO_L11N_AD9N_25	A11
F12	IO_L6P_HDGC_25	IO_L12P_AD8P_25	D12
F11	IO_L6N_HDGC_25	IO_L12N_AD8N_25	C12

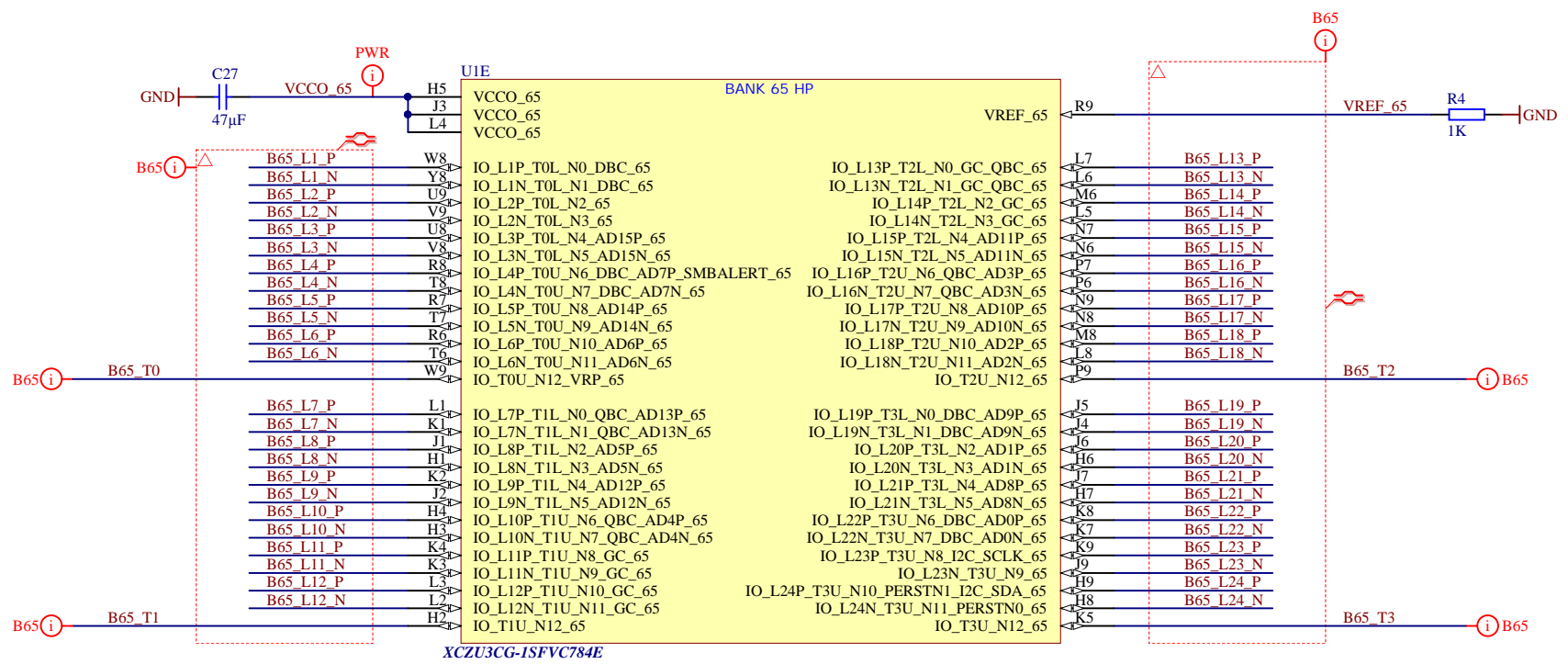


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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page6 of 26
Filename: B_HD.SchDoc		

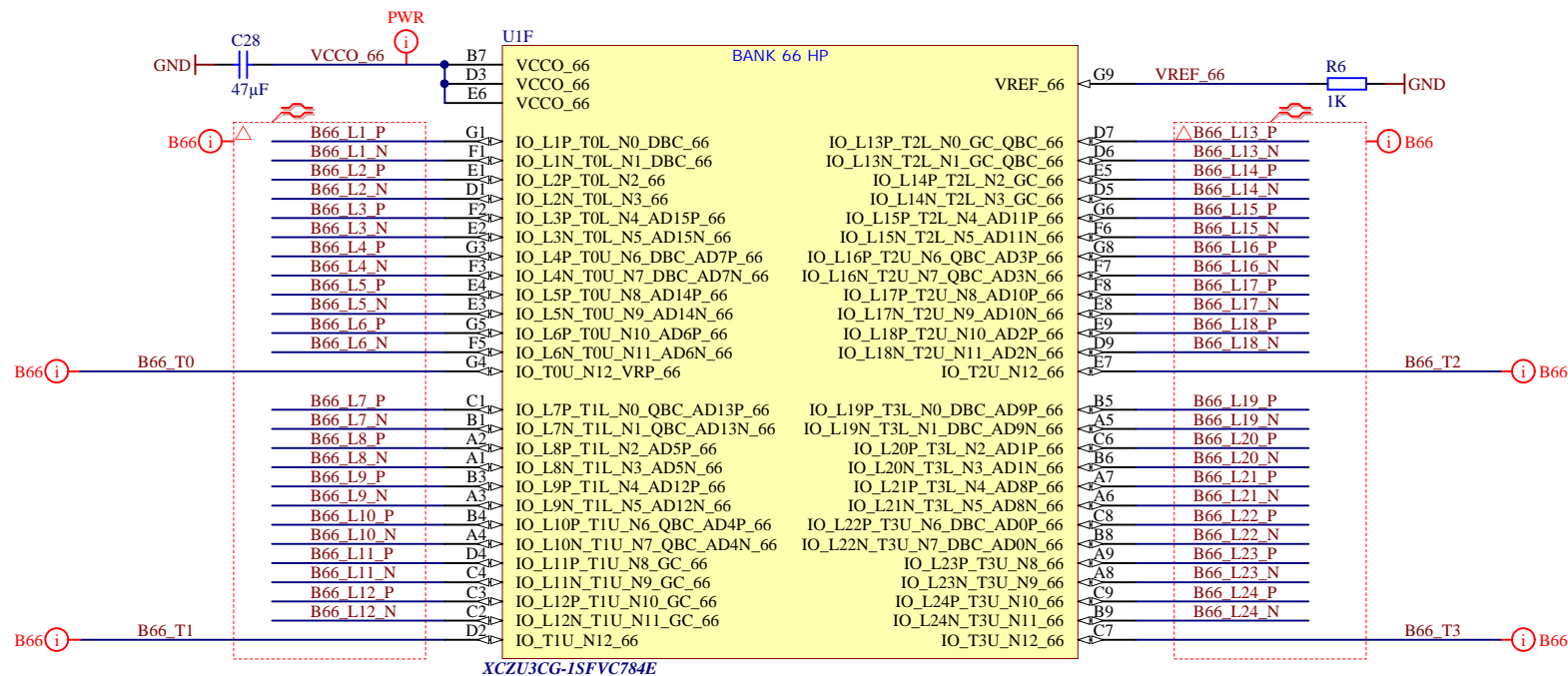




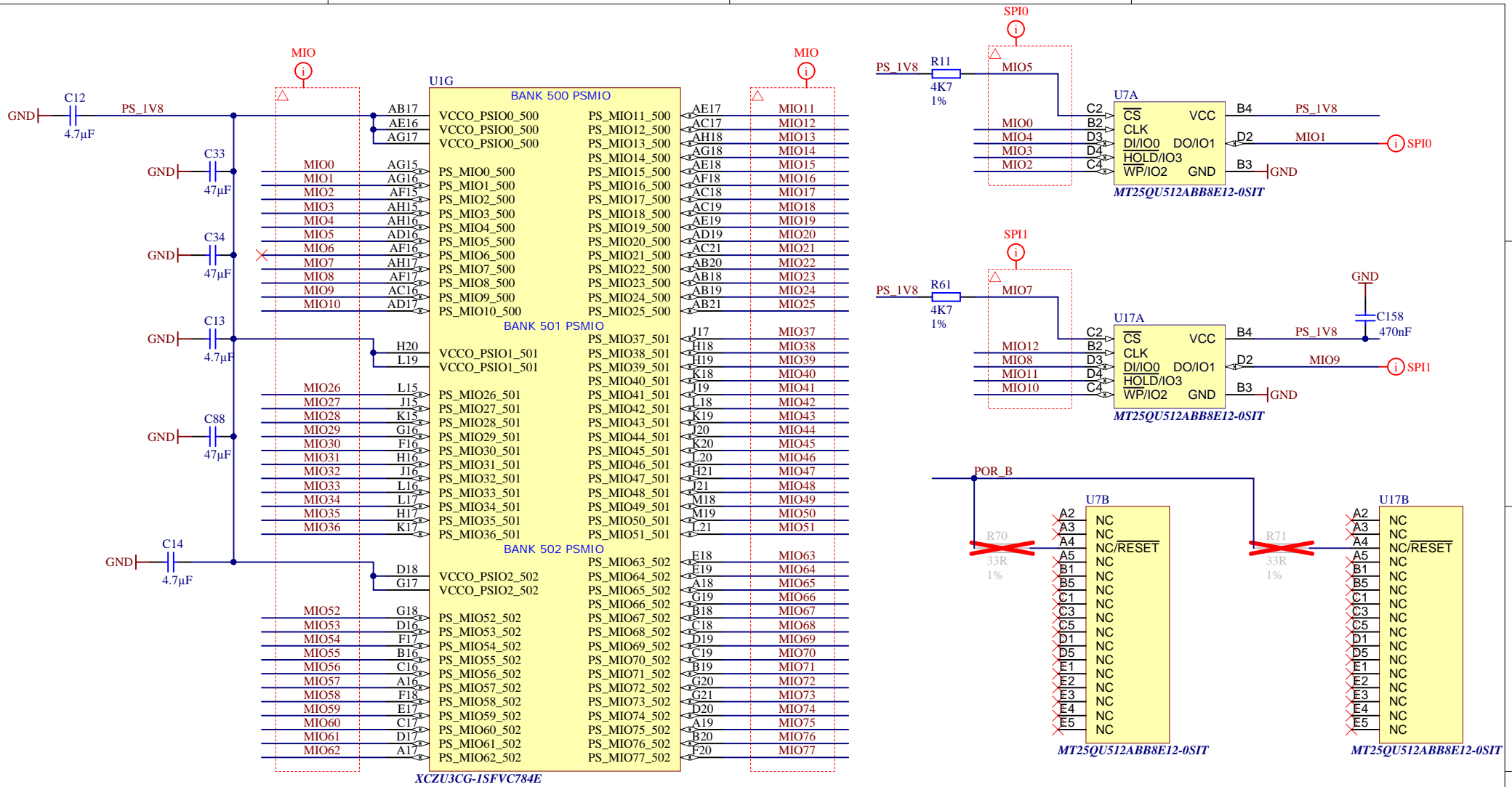
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Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>26</b>
Filename: <b>B64.SchDoc</b>		




Title: TE0803 - B65		
A4	Number: TE0803 3AE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page9 of 26
Filename: B65.SchDoc		



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	Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>26</b>
	Filename: <b>B66.SchDoc</b>		



			Title: <b>TE0803 - MIO Banks</b>	
			A4	Number: <b>TE0803 3AE11-A</b>
Date: <b>2019-02-21</b>		Copyright: Trenz Electronic GmbH / TT		Page11 of 26
Filename: <b>B_MIO.SchDoc</b>				



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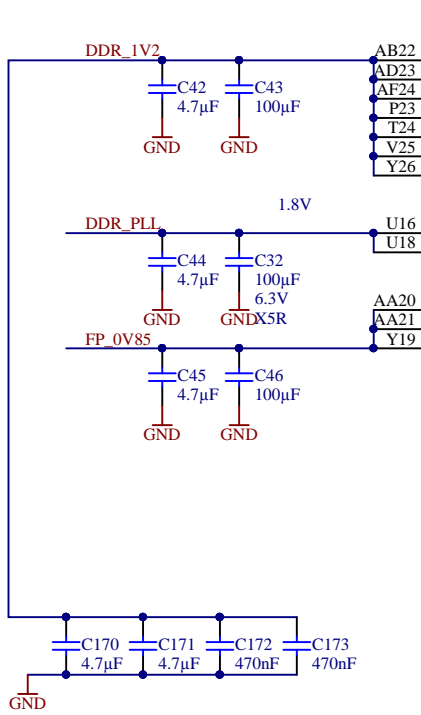
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U11		BANK 504 PSDDR			
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0 P	D80	
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0 N	D80	
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0		
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24			✗
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25			✗
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27			✗
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0		
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1		
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2		
	PS_DDR_A3_504	AA28	DDR4-A3		
	PS_DDR_A4_504	Y27	DDR4-A4		
	PS_DDR_A5_504	AA27	DDR4-A5		
	PS_DDR_A6_504	Y22	DDR4-A6		
	PS_DDR_A7_504	AA23	DDR4-A7		
	PS_DDR_A8_504	AA22	DDR4-A8		
	PS_DDR_A9_504	AB23	DDR4-A9		
	PS_DDR_A10_504	AA25	DDR4-A10		
	PS_DDR_A11_504	AA26	DDR4-A11		
	PS_DDR_A12_504	AB25	DDR4-A12		
	PS_DDR_A13_504	AB26	DDR4-A13		
	PS_DDR_A14_504	AB24	DDR4-A14		
	PS_DDR_A15_504	AC24	DDR4-A15		
	PS_DDR_A16_504	AC23	DDR4-A16		
	PS_DDR_A17_504	AC22	DDR4-A17		
	PS_DDR_CS_N0_504	W27	DDR4-CS		
	PS_DDR_CS_N1_504	V26			✗
	PS_DDR_BA0_504	V23	DDR4-BA0		
	PS_DDR_BA1_504	W22	DDR4-BA1		
	PS_DDR_BG0_504	W24	DDR4-BG0		
	PS_DDR_BG1_504	V22	DDR4-BG1		
	PS_DDR_PARITY_504	V24	DDR4-PAR		
	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET		
	PS_DDR_ACT_N_504	Y23	DDR4-ACT		
	PS_DDR_ALERT_N_504	U25	DDR4-ALERT		
	PS_DDR_ZQ_504	U24		R2 240R	GND
	PS_DDR_ODT0_504	U28	DDR4-ODT0		
	PS_DDR_ODT1_504	U26			✗

*XCZU3CG-1SFVC784E*

U1J		BANK 504 PSDDR			
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22	DQ32
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22	DQ33
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22	DQ34
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22	DQ35
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23	DQ36
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24	DQ37
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24	DQ38
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24	DQ39
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24	DQ40
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24	DQ41
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24	DQ42
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24	DQ43
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22	DQ44
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22	DQ45
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22	DQ46
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22	DQ47
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25	DQ48
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26	DQ49
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25	DQ50
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26	DQ51
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28	DQ52
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28	DQ53
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28	DQ54
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28	DQ55
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28	DQ56
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27	DQ57
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28	DQ58
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27	DQ59
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26	DQ60
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25	DQ61
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25	DQ62
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25	DQ63
		PS_DDR_DQ64_504	PS_DDR_DQ64_504	T28	
		PS_DDR_DQ65_504	PS_DDR_DQ65_504	R28	
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ66_504	P28	
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ67_504	P27	
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ68_504	P26	
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ69_504	R25	
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ70_504	P25	
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ71_504	T25	
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504			
DDR4-DQS3 N	AF27	PS_DDR_DQS_N3_504			
DDR4-DQS4 P	N23	PS_DDR_DQS_P4_504			
DDR4-DQS4 N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM0_504	AG20	DDR4-DM0
DDR4-DQS5 P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM1_504	AE23	DDR4-DM1
DDR4-DQS5 N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM2_504	AE25	DDR4-DM2
DDR4-DQS6 P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM3_504	AE28	DDR4-DM3
DDR4-DQS6 N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM4_504	R23	DDR4-DM4
DDR4-DQS7 P	J26	PS_DDR_DQS_P7_504	PS_DDR_DM5_504	H23	DDR4-DM5
DDR4-DQS7 N	J27	PS_DDR_DQS_N7_504	PS_DDR_DM6_504	L27	DDR4-DM6
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM7_504	H26	DDR4-DM7
	T27	PS_DDR_DQS_N8_504	PS_DDR_DM8_504	T26	

*XCZU3CG-1SFVC784E*



Title: <b>TE0803 - PS_DDR</b>		
A4	Number: <b>TE0803 3AE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>12</b> of <b>26</b>
Filename: <b>PS_DDR.SchDoc</b>		



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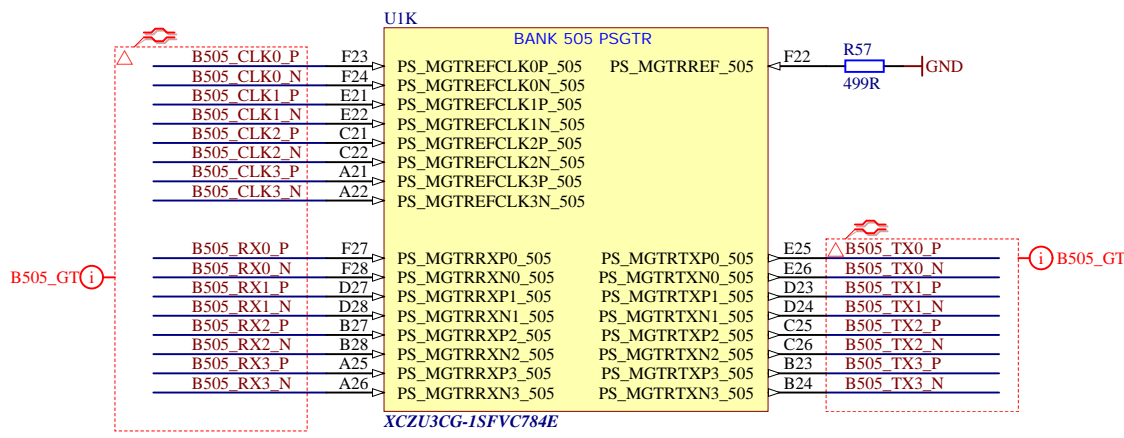
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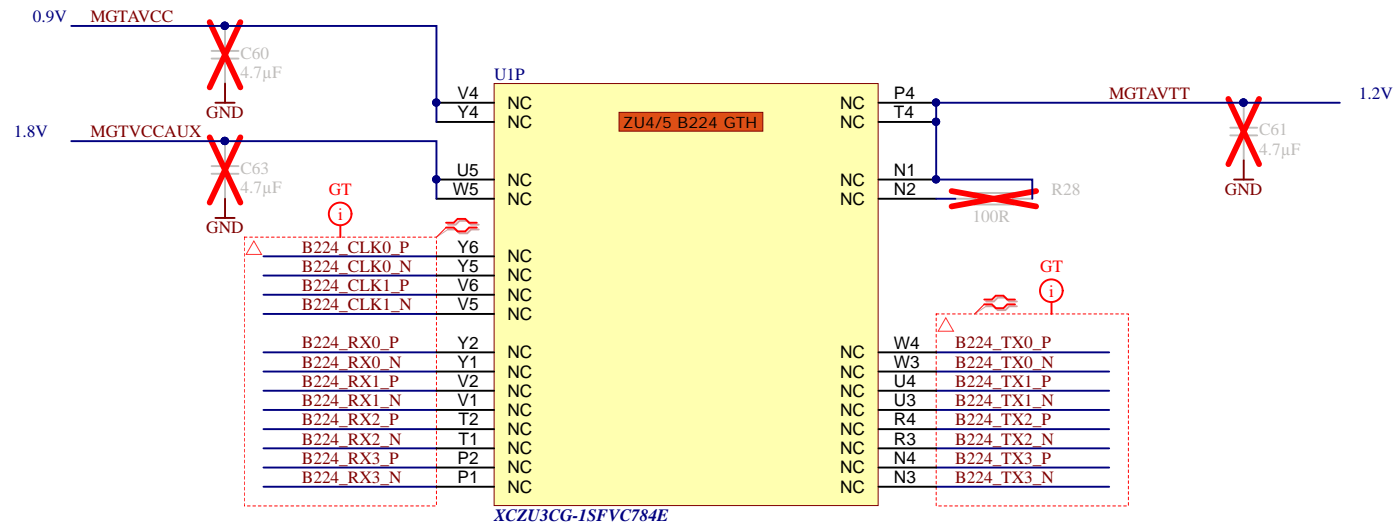
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	Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	
	Page <b>13</b> of <b>26</b>		
Filename: <b>B_PS_GT.SchDoc</b>			


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		Title: TE0803 - B224GTH	
		A4	Number: TE0803 3AE11-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: B_GT.SchDoc		Page 14 of 26	



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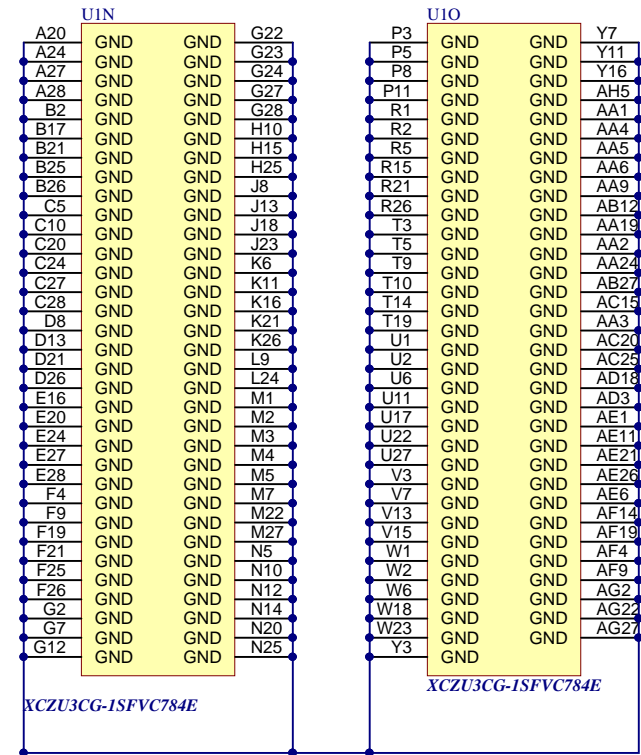
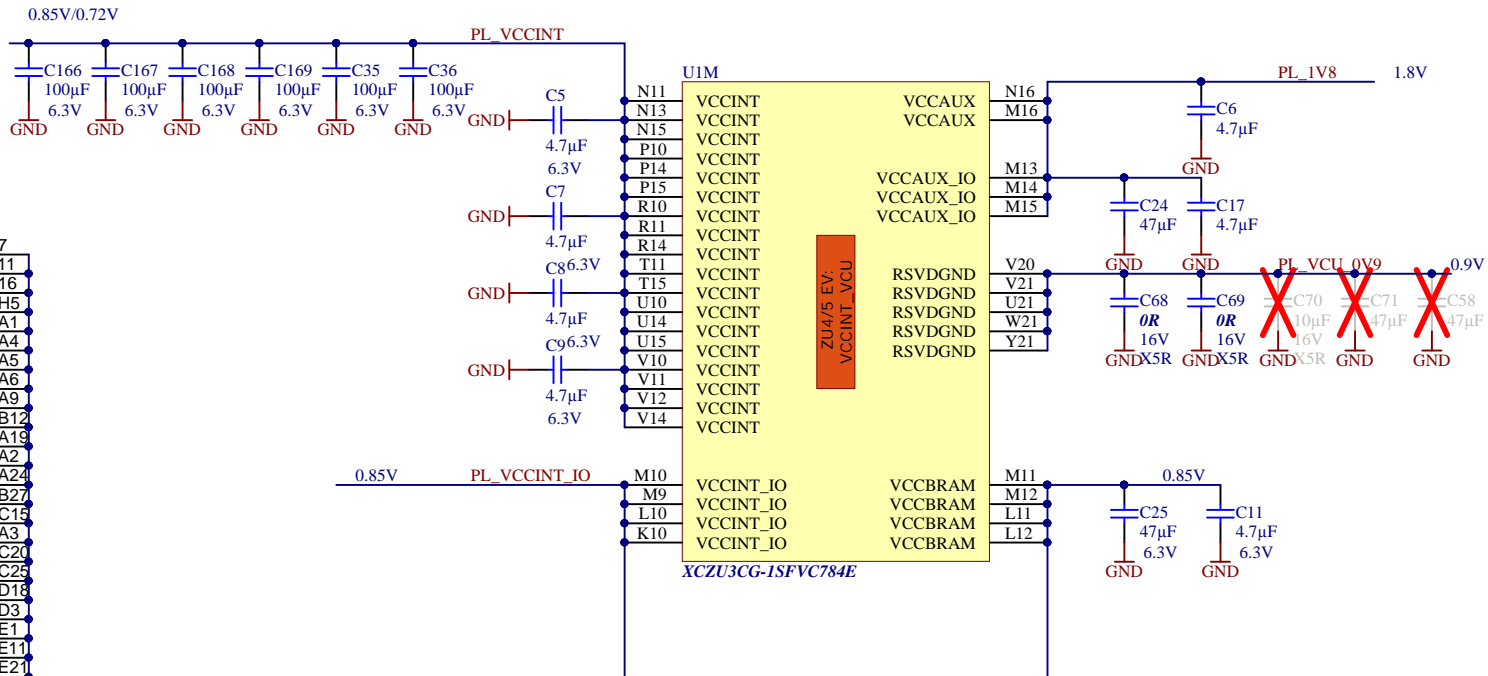
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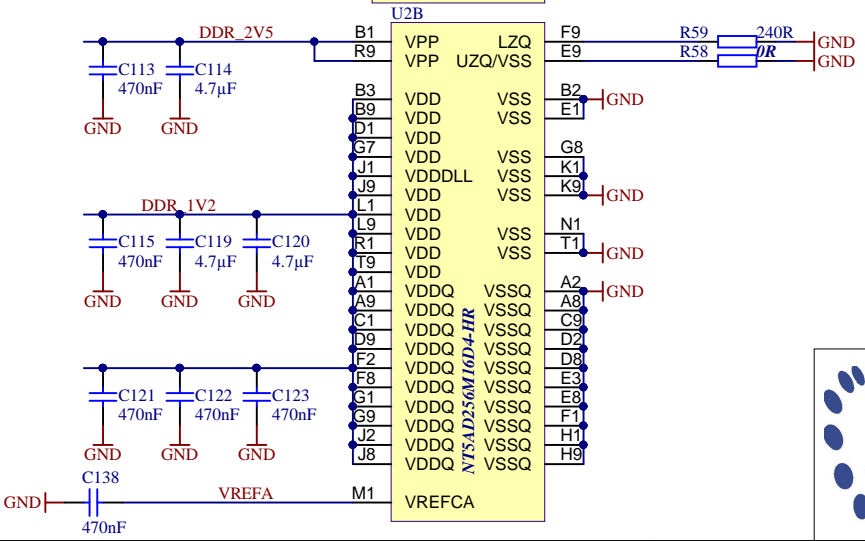
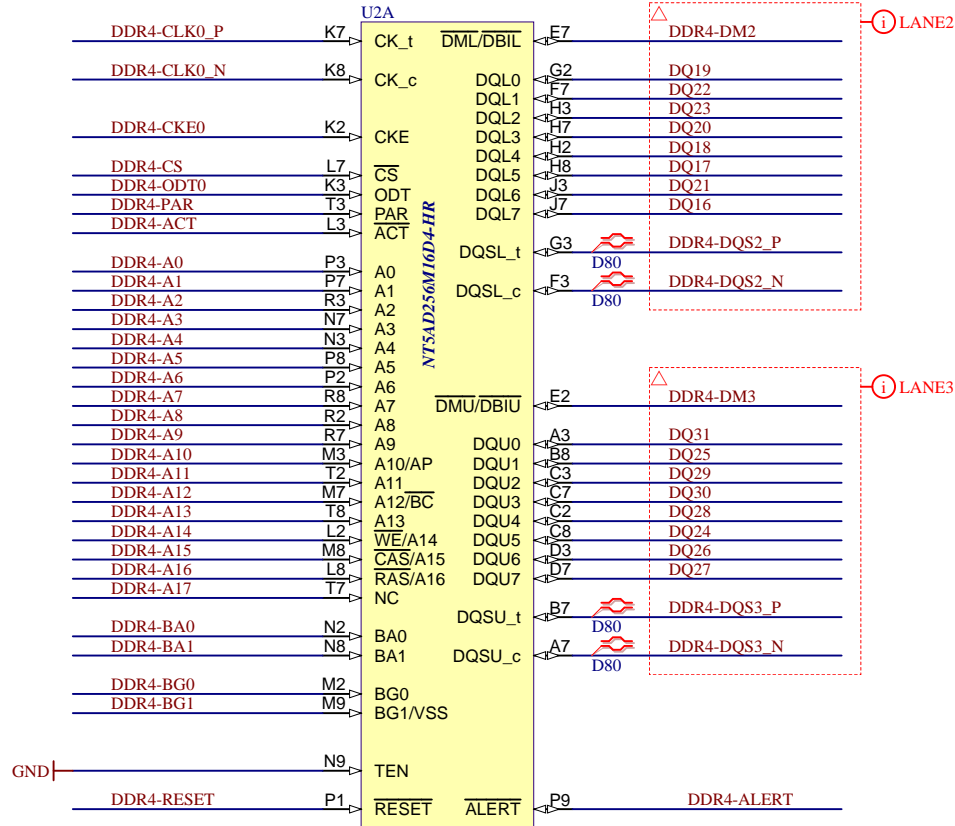
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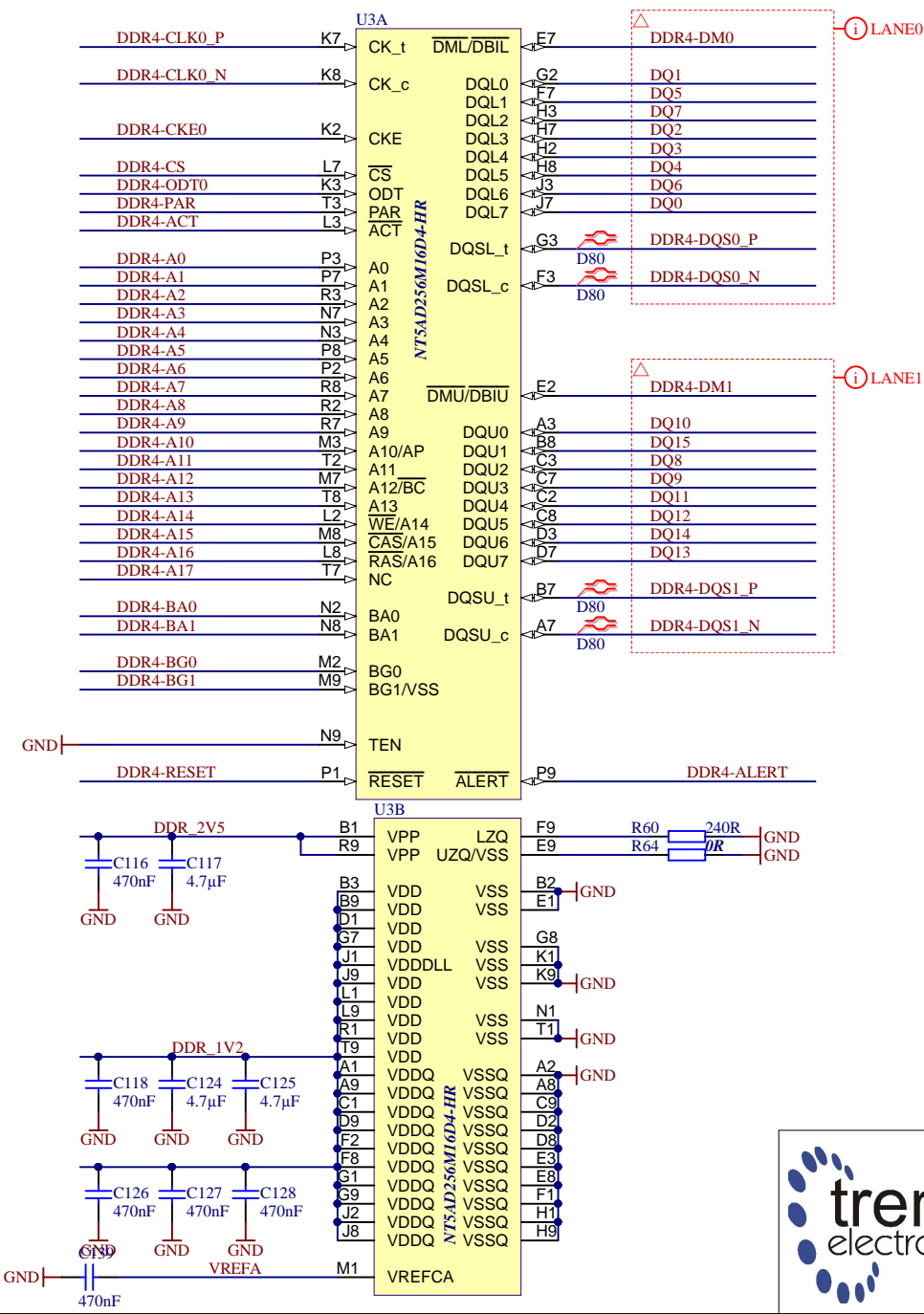
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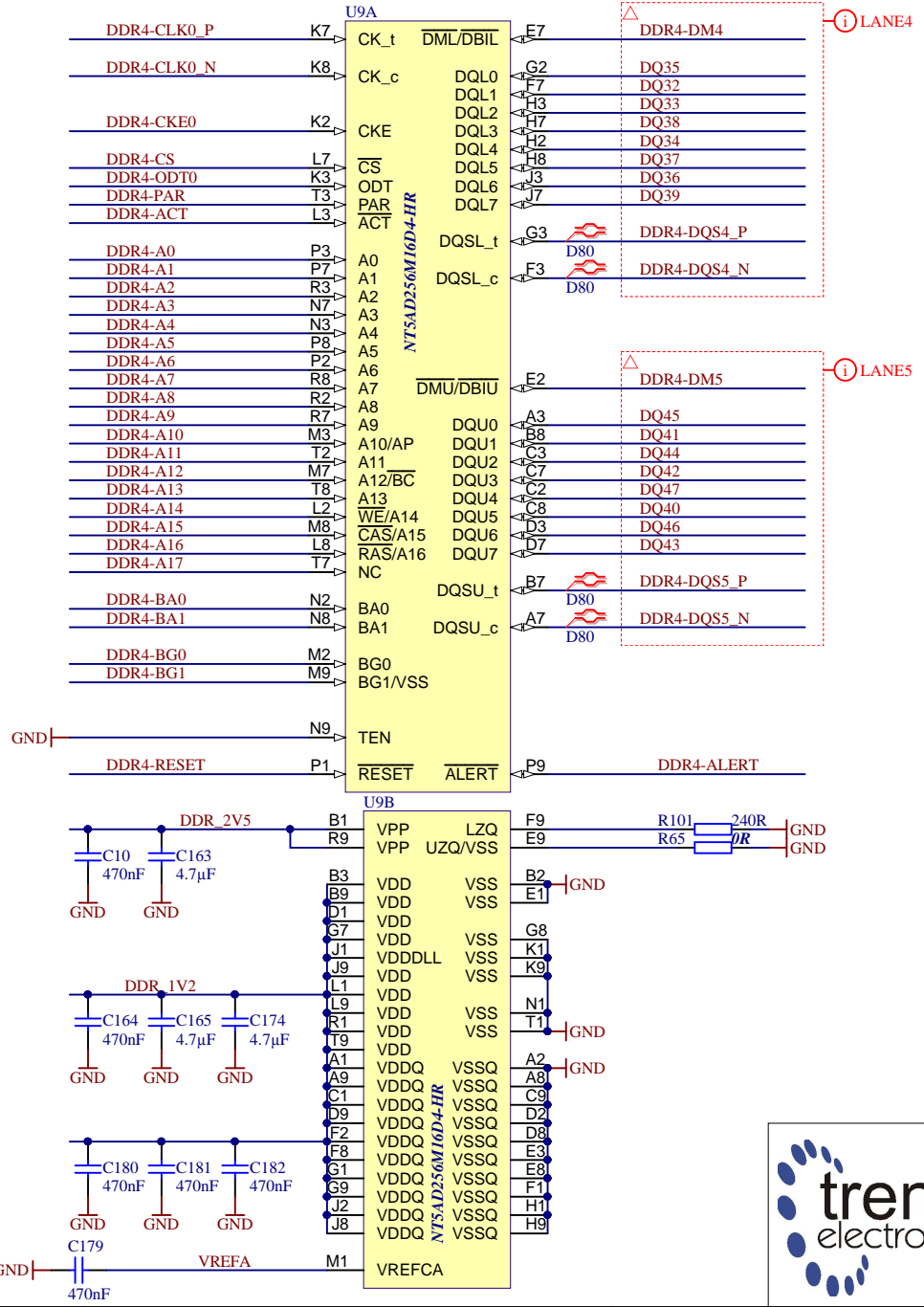
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	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 16 of 26
	Filename: ZU_POWER.SchDoc		



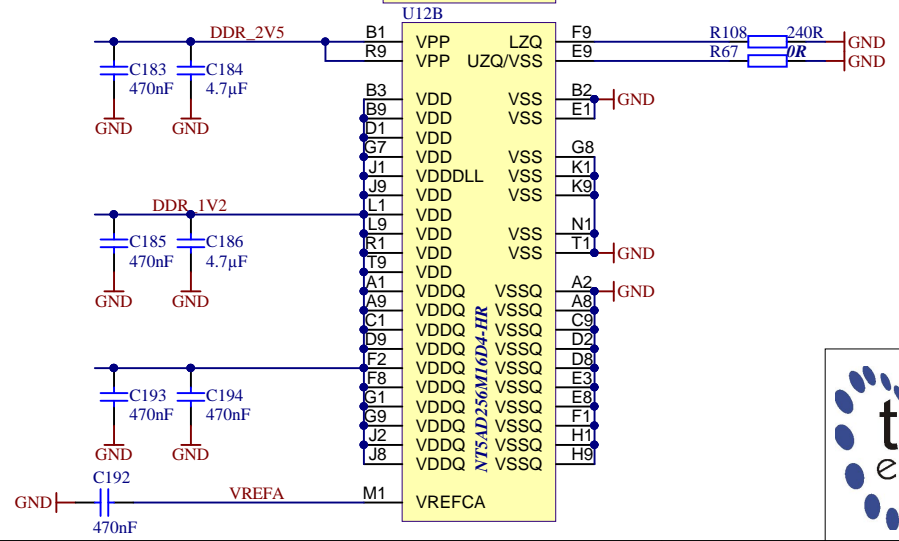
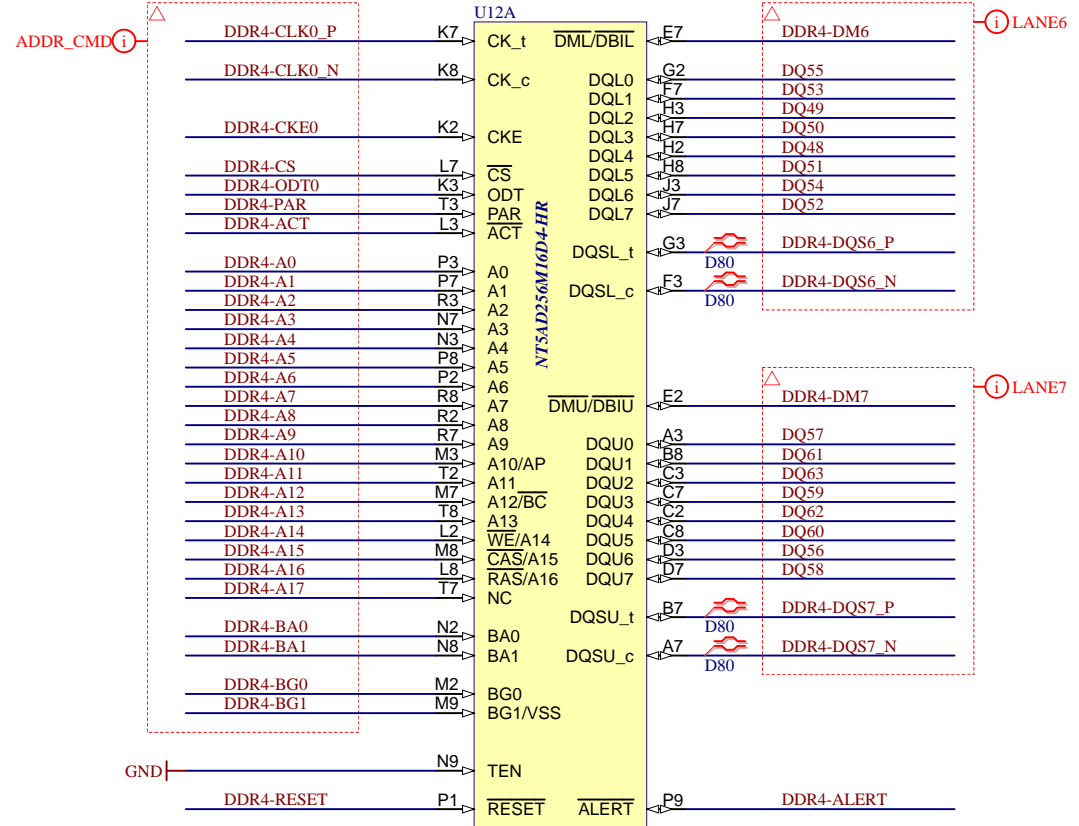
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		



Title: TE0803 - DDR4_2_RAM		
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page18 of 26
Filename: DDR4-RAM_2.SchDoc		

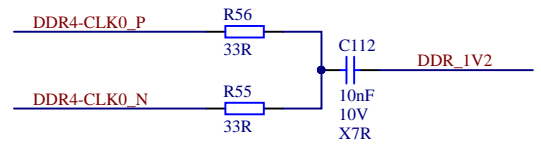
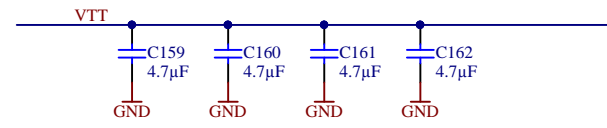
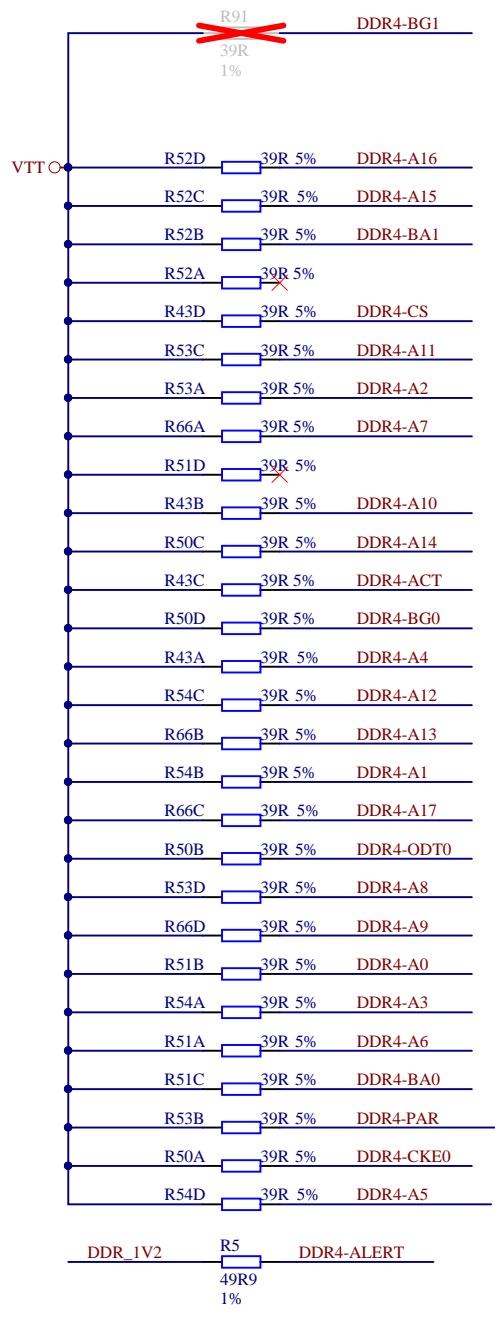


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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		

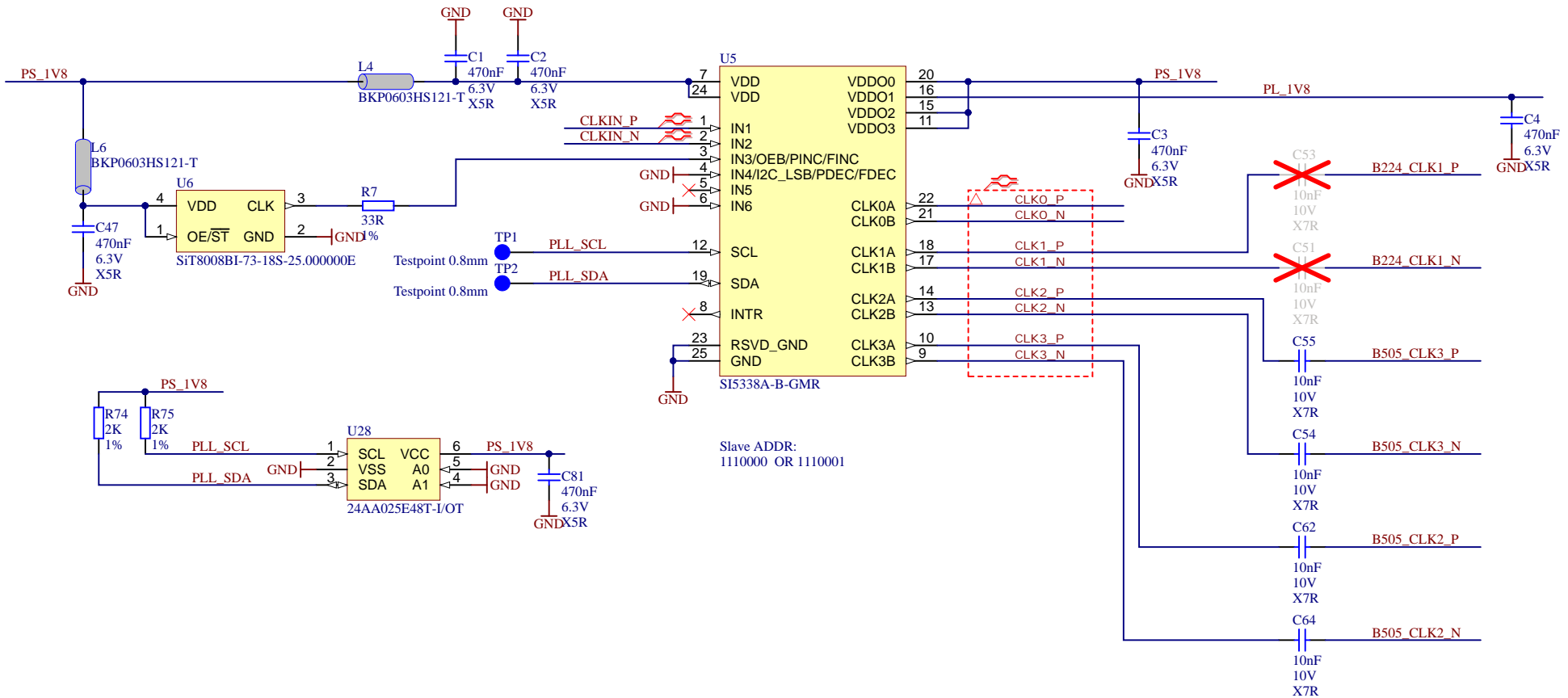


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Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>20</b> of <b>26</b>
Filename: <b>DDR4-RAM_4.SchDoc</b>		






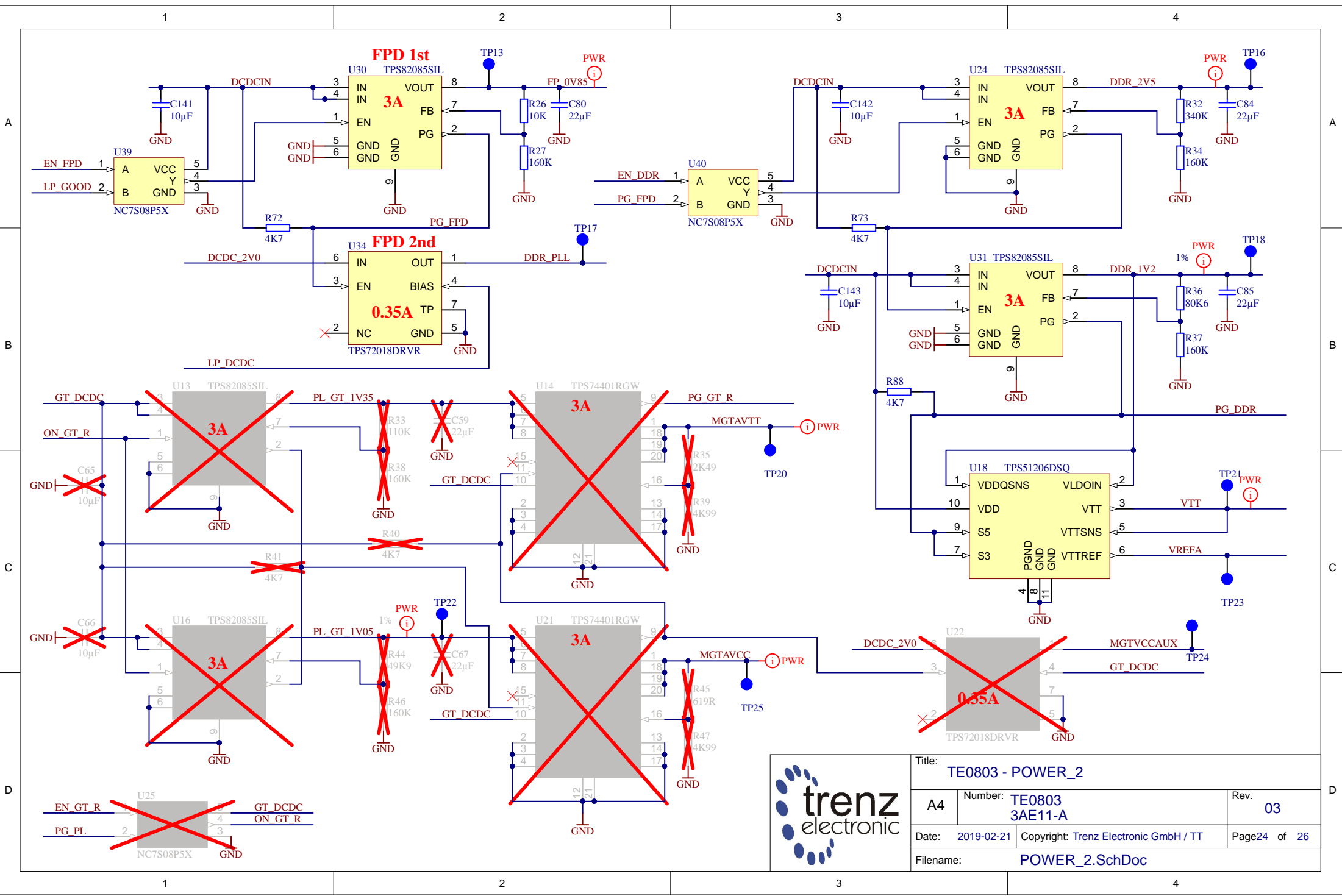
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 21 of 26
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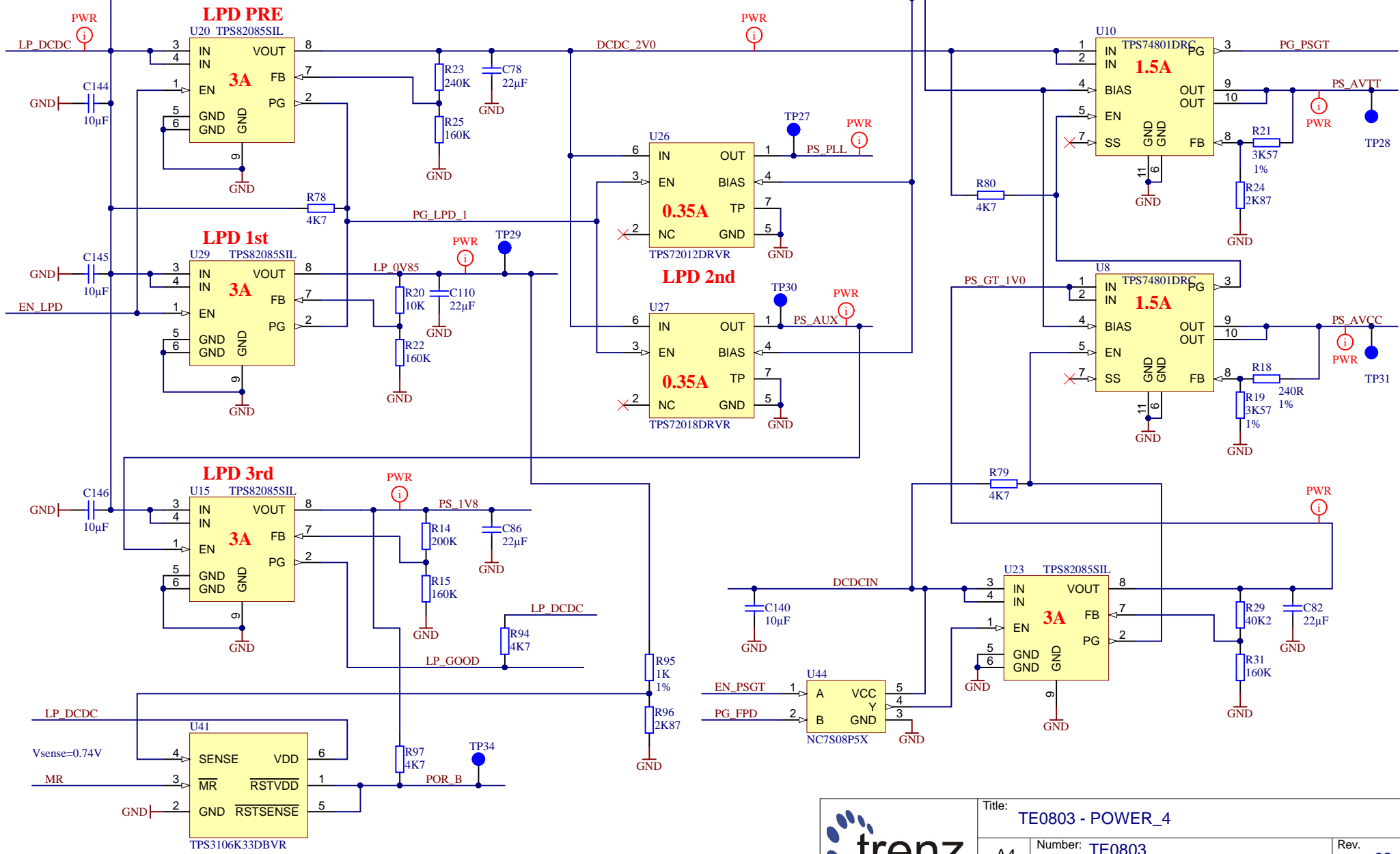
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1110000 OR 1110001

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			A4	Number: TE0803 3AE11-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page 22 of 26
Filename: Clock.SchDoc				





Title: <b>TE0803 - POWER_2</b>		
A4	Number: <b>TE0803 3AE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: Trenz Electronic GmbH / TT	
Page 24		of 26
Filename: <b>POWER_2.SchDoc</b>		



Title: TE0803 - POWER_4		
A4	Number: TE0803 3AE11-A	Rev. 03
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CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL\_VCU\_1V0 renamed to PL\_VCU\_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR\_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS\_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

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		Title: TE0803 - Changes list		
		A4	Number: TE0803 3AE11-A	Rev. 03
		Date: 2019-02-21	Copyright: Trenz Electronic GmbH	Page26 of 26
		Filename: Revision_Changes.SchDoc		

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