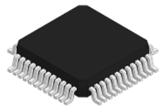
NuMicro® Family
M480
Product Brief

For additional information or questions, please contact: Nuvoton Technology Corporation.

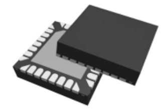
www.nuvoton.com

Features

- **Core**
  - Up to 192 MHz ARM® Cortex®-M4F delivering 1.25 DMIPS per MHz
  - DSP instruction set
  - Memory Protection Unit (MPU)
- **Memories**
  - 512/256 KB zero-wait state flash memory
  - 160/96 KB SRAM, including 32 KB external SPI Flash cache
  - 4 KB Secure Protection ROM
  - 2 KB One-Time-Programmable ROM
- **Cyclic Redundancy Calculation Unit**
- **16-channel Peripheral DMA Controller**
- **External Bus Interface**
  - LCD parallel interface, i80 mode
- **Clock**
  - 4 to 24 MHz crystal oscillator
  - 32 kHz crystal oscillator for RTC
  - Internal 12 MHz RC oscillator
  - Internal 10 kHz RC oscillator
  - Internal PLL up to 480 MHz
- **RTC**
  - 80 bytes of backup registers
- **Power Management**
  - Active: 175 µA/MHz at 25°C/3.3V (peripheral off)
  - Standby with 32 KB RAM: 45µA
  - Standby without 32 KB RAM: 40µA
- **Timer & PWM**
  - Four 32-bit timers, each supports up to 2 PWM (Total 8 PWM)
  - Twelve Enhanced PWM with twelve 16-bit timers
  - Twelve Basic PWM with two 16-bit timers
  - One 24-bit count-down SysTick timer
  - One watchdog timer
  - One window watchdog timer
- **Analog Peripheral**
  - One 12-bit, up to 16-ch 5MSPS SAR ADC
  - Two 12-bit, 1MSPS DAC
  - Two rail-to-rail comparators
  - Up to three operational amplifiers
- **Cryptography Accelerator**
  - ECC-192, 256
  - AES-128, 192, 256 / DES / 3DES
  - SHA-160, 224, 256, 384, 512 / HMAC
  - Random number generator



LQFP48 (7x7 mm)
LQFP64 (7x7 mm)
LQFP128 (14x14 mm)
LQFP144 (20x20 mm)



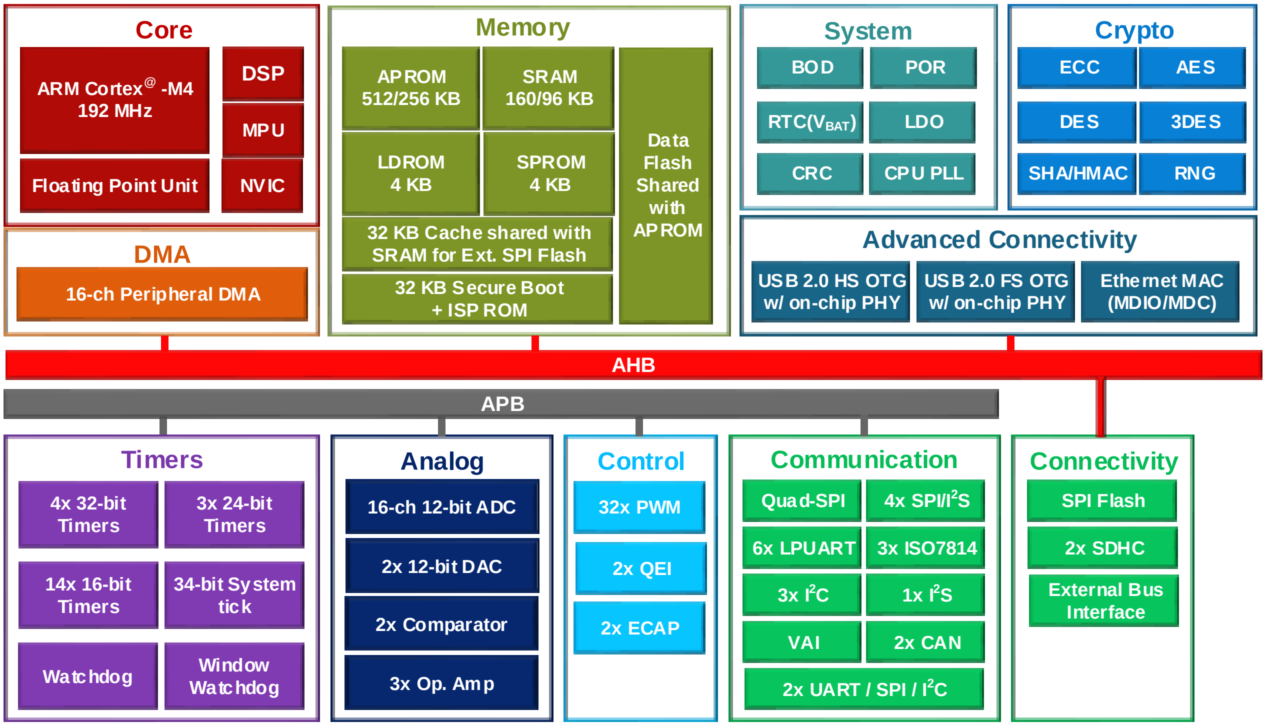
QFN33 (5x5 mm)

- **Communication Interface**
  - Up to 9 UART interfaces, including ISO-7816, LIN and IrDA interfaces
  - Three I^2C interfaces (Up to 3.4 Mbps)
  - One SPI Flash interface (Up to 96Mbps) supports quad mode
  - One Quad-SPI interface (Up to 48MB/s)
  - Up to 4 SPI/I^2S interfaces (SPI up to 96Mbps, I^2S up to 6Mbps)
  - One I^2S interface (Up to 12Mbps)
  - Two configurable USCI interfaces for UART / SPI / I^2C
  - Two CAN 2.0B interfaces (Up to 1Mbps)
  - Two Secure Digital Host Controllers (Up to 200Mbps)
- **Control Interface**
  - Up to two quadrature encoder interfaces
  - Two 24-bit, 3-ch input capture timer/counter units
- **Advanced Connectivity**
  - USB 2.0 high speed device/host/OTG controller with on-chip PHY
  - USB 2.0 full speed device/host/OTG controller with on-chip PHY
  - 10/100 Ethernet MAC with RMII
- **Operating Characteristic**
  - Voltage range: 1.8V to 3.6V
  - Temperature range: -40°C to +105°C
- **Voltage Adjustable Interface**
  - Up to six I/O ports support VAI with supply V_{DDIO} from 1.8V to 3.6V
- **Up to 115 I/O pins with interrupt capability**
  - Up to 84 5V-tolerant I/O pins
- **Up to six tamper detection pins**
- **96-bit Unique ID (UID)**
- **128-bit Unique Customer ID (UCID)**

Applications

- Consumer Electronic
- IoT / Industrial IoT / Payment
- Serial-to-Ethernet Converter

1 BLOCK DIAGRAM



Series	USB Full Speed	USB High Speed	CAN 2.0B	Cryptography	Ethernet
M481					
M482	√				
M483	√	√	√		
M484	√	√			
M485	√	√		√	
M487	√	√	√	√	√

2 FEATURE DESCRIPTION

Core and System	
ARM® Cortex®-M4	• ARM® Cortex® -M4 processor, running up to 192 MHz • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option. (3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V)
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level.
Security	• 96-bit Unique ID (UID). • 128-bit Unique Customer ID (UCID). • One built-in temperature sensor with 1℃ resolution.
Memories	
Boot Loader	• Factory pre-loaded 32 KB mask ROM for secure boot procedure • Uses SHA-256 and AES-256 to validate data in APROM, LDROM and external SPI Flash • Nuvoton ISP (In-System-Programming) tool for firmware upgrade via UART and high speed USB device • ISP/IAP libraries
Flash	• Dual bank 512/256 KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade • 192 MHz maximum frequency, with performance at zero wait cycle in continuous address read access • 4 KB on-chip Flash for user-defined loader (LDROM) • 8 KB non-readble Key Protection ROM (KPROM) for firmware programming protection • 4 KB non-readble Security Protection ROM (SPROM) for intelectual property protection • 2 KB One Time Programable (OTP) ROM for data security • All on-chip Flash support 4 KB page erase

	• Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 160 KB on-chip SRAM includes: – 32 KB SRAM located in bank 0 that supports hardware parity check and retenion mode; Exception (NMI) generated upon a parity check error – 96/32 KB SRAM located in bank 1 – 32 KB SRAM located in bank 2 that can be used as cache for external SPI Flash memory • Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one’s complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Sixteen independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise

	timing operation • 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 2% accuracy that can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 480 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain • The RTC clock source includes Low-speed external crystal oscillator (LXT) • The RTC block includes 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type

	• Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve 192 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger EADC or DAC to start conversion
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 192 MHz PWM output channels. • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion.
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset.
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-	• One 12-bit, 19-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is

Digital Converter (EADC)	guaranteed. • Three internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin or internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V. • Two power saving modes: Power-down mode and Standby mode • Supports calibration capability. • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or PWM trigger. • Configurable EADC sampling time. • Up to 19 sample modules. • Double data buffers for sample module 0~3. • PDMA operation.
Digital-to-Analog Converter (DAC)	• Two 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time. • Maximum output voltage AV_{DD} -0.2V at buffer mode • Digital-to-Analog conversion triggered by Timer0~3, EPWM0, EPWM1, external trigger pin to start DAC conversion or software. • Supports group mode for synchronized data update of two DACs. • PDMA operation
Analog Comparator (ACMP)	• Two rail-to-rail Analog Comparators. • Supports four multiplexed I/O pins at positive input. • Supports I/O pins, band-gap, DAC, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports four programmable propagation speeds for power saving • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode. • Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
Operational Amplifier (OPA)	• Three Operational Amplifiers with 0~AV_{DD} input voltage range. • OPA schmitt trigger buffer output used as the interrupt source of comparator.
Communication Interfaces	
Low-power UART	• Six sets of UARTs with up to 17.45 MHz baud rate. • Auto-Baud Rate measurement and baud rate compensation function. • Supports low power UART (LPUART): baud rate clock from LXT(32.768 KHz) with 9600bps in Power-down mode even system clock is stopped.

	• 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode. • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation.
Smart Card Interface	• Three sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function. • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal.
I^2C	• Three sets of I^2C devices with Master/Slave mode. • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) and High speed mode (3.4Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
SPI Master (SPI Flash)	• Maximum 32 MB external SPI Flash memory with standard (1-bit), dual (2-bit) and quad (4-bit) transfer mode. • 32 KB cache memory for enhancing program execution

	performance. • 64-bit key length for code protection. • DMA mode for code transfer between SPI Flash memory and SRAM. • SPI Master function with 8-, 16-, 24-, and 32-bit length of transaction and burst mode operation, which can transmit/receive data up to four successive transactions in one transfer.
Quad SPI	• One set of SPI Quad controller with Master/Slave mode, up to 96 MHz at 2.7V~3.6V stsyem voltage. • Supports Dual and Quad I/O Transfer mode • Supports one/two data channel half-duplex transfer • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation.
SPI/I²S	• Up to four sets of SPI/I²S controllers with Master/Slave mode. • SPI/I²S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers. **SPI** • Up to 96 MHz. • Configurable bit length of a transfer word from 8 to 32-bit. • MSB first or LSB first transfer sequence. • Byte reorder function. • Supports Byte or Word Suspend mode. • Supports one data channel half-duplex transfer. • Supports receive-only mode. **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes. • Supports PCM mode A, PCM mode B, I²S and MSB justified data format. • PDMA operation.
I²S	• One set of I²S interface with Master/Slave mode. • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes. • Two 16-level FIFO data buffers, one for transmitting and the other for receiving.

	• Supports I^2S protocols: Philips standard, MSB-justified, and LSB-justified data format. • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format. • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8. • PDMA operation.
Universal Serial Control Interface (USCI)	• Two sets of USCI,configured as UART, SPI or I^2C function. • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload. • Supports hardware auto flow control function and programmable flow control trigger level. • 9-bit Data Transfer. • Baud rate detection by built-in capture event of baud rate generator. • Supports wake-up function. • PDMA operation. **SPI** • Supports Master or Slave mode operation. • Supports one transmit buffer and two receive buffer for data payload. • Supports additional receive/transmit 16 entries FIFO for data payload. • Configurable bit length of a transfer word from 4 to 16-bit (SPI Quad transmission only supports 8 to 16-bit of word length). • Supports MSB first or LSB first transfer sequence. • Supports Word Suspend function. • Supports 3-wire, no slave select signal, bi-direction interface. • Supports wake-up function: input slave select transition. • PDMA operation. **I^2C** • Supports master and slave device capability. • Supports one transmit buffer and two receive buffer for data payload. • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps). • Supports 10-bit mode. • Supports 10-bit bus time out capability. • Supports bus monitor mode. • Supports power-down wake-up by data toggle or address match. • Supports multiple address recognition.

	• Supports device address flag. • Programmable setup/hold time.
Controller Area Network (CAN)	• Two sets of CAN 2.0B controllers. • Each supports 32 Message Objects; each Message Object has its own identifier mask. • Programmable FIFO mode (concatenation of Message Object). • Disabled Automatic Re-transmission mode for Time Triggered CAN applications. • Supports power-down wake-up function.
Secure Digital Host Controller (SDHC)	• Two sets of Secure Digital Host Controllers, compliant with SD Memory Card Specification Version 2.0. • Supports 50 MHz to achieve 200 Mbps at 3.3V operation. • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card.
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter. • Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space. • 8-/16-bit data width. • Supports byte write in 16-bit data width mode. • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R). • Supports Address/Data multiplexed mode. • Supports address bus and data bus separate mode. • Supports LCD interface i80 mode. • PDMA operation.
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode. • Selectable TTL/Schmitt trigger input. • Configured as interrupt source with edge/level trigger setting. • Supports independent pull-up/pull-down control. • Supports high driver and high sink current I/O. • Supports software selectable slew rate control. • Supports 5V-tolerance function except analog I/O.
Control Interfaces	
Quadrature Encoder Interface (QEI)	• Two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX). • Supports 2/4 times free-counting mode and 2/4 compare-counting

	mode. • Supports encoder pulse width measurement mode with ECAP.
Enhanced Capture (ECAP)	**Input Capture Timer/Counter** • Supports three input channels with independent capture counter hold register. • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter. • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports. • Supports compare-match function.
Advanced Connectivity	
USB 2.0 Full Speed with on-chip PHY	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG PHY. • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only or ID-dependent **USB 2.0 Full Speed Host Controller** • Compliant with USB Revision 1.1 Specification. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Supports Control, Bulk, Interrupt, Isochronous and Split transfers. • Integrated a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Supports port power control and port over current detection. • Built-in DMA. **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports suspend function when no bus activity existing for 3 ms. • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types. • 1024 bytes configurable RAM for endpoint buffer. • Remote wake-up capability. • Start of Frame (SOF) locked clock pulse generation for crystal-less feature.
USB 2.0 High Speed with on-chip PHY	**USB 2.0 High Speed OTG (On-The-Go)** • On-chip USB 2.0 high speed OTG PHY. • Compliant with USB OTG Supplement 2.0.

	• Configurable as host-only, device-only or ID-dependent. **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification. • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Integrated a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Built-in DMA. **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports one dedicate control endpoint and 12 configurable endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction. • 4096 bytes configurable RAM for endpoint buffer and up to 1024 bytes maximum packet size. • Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode. • Suspend, resume and remote wake-up capability. • Built-in DMA.
Ethernet MAC	• IEEE Std. 802.3 CSMA/CD protocol. • Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol. • Supports both half and full duplex for 10 Mbps or 100 Mbps operation. • RMII (Reduced Media Independent Interface) and serial management interface (MDC/MDIO). • Pause and remote pause function for flow control. • Long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception. • CAM function for Ethernet MAC address recognition. • Supports Magic Packet recognition to wake system up from Power-down mode. • Built-in DMA.
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator. • Supports 192-bit and 256-bit key length. • Supports both prime field GF(p) and binary field GF(2^m).

	• Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes. • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes. • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes. • Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m). • Supports modulus division, multiplication, addition and subtraction operations in GF(p).
Advanced Encryption Standard (AES)	• Hardware AES accelerator. • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197. • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum.
Data Encryption Standard (DES)	• Hardware DES accelerator. • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode. • Compliant with FIPS 46-3.
Triple Data Encryption Standard (3DES)	• Hardware Triple DES accelerator. • Supports two or three different keys in each round. • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode. • Implemented based on X9.52 standard and compliant with FIPS SP 800-67.
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator. • Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512. • Compliant with FIPS 180/180-2.
keyed-Hash Message Authentication Code (HMAC)	• Hardware HMAC accelerator. • Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512. • Compliant with FIPS 180/180-2.

3 PARTS INFORMATION

3.1 Package Type

Part No.	QFN33	LQFP48	LQFP64	LQFP128	LQFP144
M481	M481ZGAAE M481ZIDAE	M481LGAAE M481LIDAE	M481SGAAE M481SIDAE		
M482	M482ZIDAE	M482LGAAE M482LIDAE	M482SGAAE M482SIDAE	M482KGAAE M482KIDAE	
M483			M483SGAAE M483SIDAE	M483KIDAE	
M484			M484SGAAE M484SIDAE M484SGAAE2U M484SIDAE2U	M484KIDAE	
M485	M485ZIDAE	M485LIDAE	M485SIDAE	M485KIDAE	
M487			M487SIDAE	M487KIDAE	M487JIDAE

3.2 NuMicro® M481 Base Series

PART NUMBER		M481					
		ZGAAE	ZIDAE	LGAAE	LIDAE	SGAAE	SIDAE
Flash (KB)		256	512	256	512	256	512
SRAM (KB)		96	160	96	160	96	160
ISP Loader ROM (KB)		4					
I/O		26		41		52	
32-bit Timer		4					
Tamper		-		-		1	
Connectivity	LPUART	6					
	ISO-7816	3					
	SPI Master	1					
	Quad SPI	1					
	SPI/I²S	3		3		4	
	I²S	1					
	I²C	3					
	USCI	2					
	CAN	-					
	LIN	2					
	SDHC	1		2		2	
16-bit PWM		24					
QEI		1		2		2	
ECAP		-		1		1	
USB 2.0 FS OTG		-					
USB 2.0 HS OTG		-					
12-bit ADC		10		12		16	
12-bit DAC		2					
Analog Comparator		2					
Operational Amplifier		1		2		2	
Ethernet		-					
Cryptography		-					
LCD Parallel Data Bus (External Bus Interface)		-		8		16	
Package		QFN 33		LQFP 48		LQFP 64	

3.3 NuMicro® M482 USB FS OTG Series

PART NUMBER		M482						
		ZIDAE	LGAAE	LIDAE	SGAAE	SIDAE	KGAAE	KIDAE
Flash (KB)		512	256	512	256	512	256	512
SRAM (KB)		160	96	160	96	160	96	160
ISP Loader ROM (KB)		4						
I/O		26	41		52		100	
32-bit Timer		4						
Tamper		-	-		1		6	
Connectivity	LPUART	6						
	ISO-7816	3						
	SPI Master	1						
	Quad SPI	1						
	SPI/I²S	3	3		4		4	
	I²S	1						
	I²C	3						
	USCI	2						
	CAN	-						
	LIN	2						
	SDHC	2						
16-bit PWM		24						
QEI		1	2		2		2	
ECAP		-	1		1		2	
USB 2.0 FS OTG		√						
USB 2.0 HS OTG		-						
12-bit ADC		10	12		16		16	
12-bit DAC		2						
Analog Comparator		2						
Operational Amplifier		1	2		2		3	
Ethernet		-						
Cryptography		-						
LCD Parallel Data Bus (External Bus Interface)		-	8		16		16	
Package		QFN33	LQFP 48		LQFP 64		LQFP 128	

3.4 NuMicro® M483 CAN Series

PART NUMBER		M483		
		SGAAE	SIDAE	KIDAE
Flash (KB)		256	512	512
SRAM (KB)		96	160	160
ISP Loader ROM (KB)		4		
I/O		44		100
32-bit Timer		4		
Tamper		1		6
Connectivity	LPUART	6		
	ISO-7816	3		
	SPI Master	1		
	Quad SPI	1		
	SPI/I²S	4		
	I²S	1		
	I²C	3		
	USCI	2		
	CAN	2		
	LIN	2		
	SDHC	2		
16-bit PWM		24		
QEI		2		
ECAP		1		2
USB 2.0 FS OTG		-		√
USB 2.0 HS OTG		√		
12-bit ADC		16		
12-bit DAC		2		
Analog Comparator		2		
Operational Amplifier		2		3
Ethernet		-		
Cryptography		-		
LCD Parallel Data Bus (External Bus Interface)		8		16
Package		LQFP 64		LQFP 128

3.5 NuMicro® M484 USB HS OTG Series

PART NUMBER		M484				
		SGAAE	SIDAE	SGAAE2U	SIDAE2U	KIDAE
Flash (KB)		256	512	256	512	512
SRAM (KB)		96	160	96	160	160
ISP Loader ROM (KB)		4				
I/O		44		44		100
32-bit Timer		4				
Tamper		1		1		6
Connectivity	LPUART	6				
	ISO-7816	3				
	SPI Master	1				
	Quad SPI	1				
	SPI/I²S	4				
	I²S	1				
	I²C	3				
	USCI	2				
	CAN	-				
	LIN	2				
	SDHC	2				
16-bit PWM		24				
QEI		2				
ECAP		1		1		2
USB 2.0 FS OTG		-		√		√
USB 2.0 HS OTG		√				
12-bit ADC		16				
12-bit DAC		2				
Analog Comparator		2				
Operational Amplifier		2		2		3
Ethernet		-				
Cryptography		-				
LCD Parallel Data Bus (External Bus Interface)		8		8		16
Package		LQFP 64		LQFP 64		LQFP 128

3.6 NuMicro® M485 Crypto Series

PART NUMBER		M485			
		ZIDAE	LIDAE	SIDAE	KIDAE
Flash (KB)		512			
SRAM (KB)		160			
ISP Loader ROM (KB)		4			
I/O		26	41	44	100
32-bit Timer		4			
Tamper		-	-	1	6
Connectivity	LPUART	6			
	ISO-7816	3			
	SPI Master	1			
	Quad SPI	1			
	SPI/I²S	3	3	4	4
	I²S	1			
	I²C	3			
	USCI	2			
	CAN	-			
	LIN	2			
	SDHC	1	2	2	2
16-bit PWM		24			
QEI		1	2	2	2
ECAP		-	1	1	2
USB 2.0 FS OTG		√	√	-	√
USB 2.0 HS OTG		-	-	√	√
12-bit ADC		10	12	16	16
12-bit DAC		2			
Analog Comparator		2			
Operational Amplifier		1	2	2	3
Ethernet		-			
Cryptography		√			
LCD Parallel Data Bus (External Bus Interface)		-	8	8	16
Package		QFN33	LQFP 48	LQFP 64	LQFP 128

3.7 NuMicro® M487 Ethernet Series

PART NUMBER		M487		
		SIDAE	KIDAE	JIDAE
Flash (KB)		512		
SRAM (KB)		160		
ISP Loader ROM (KB)		4		
I/O		44	100	114
32-bit Timer		4		
Tamper		1	6	6
Connectivity	LPUART	6		
	ISO-7816	3		
	SPI Master	1		
	Quad SPI	1		
	SPI/I²S	4		
	I²S	1		
	I²C	3		
	USCI	2		
	CAN	2		
	LIN	2		
	SDHC	2		
16-bit PWM		24		
QEI		2		
ECAP		1	2	2
USB 2.0 FS OTG		-	√	√
USB 2.0 HS OTG		√		
12-bit ADC		16		
12-bit DAC		2		
Analog Comparator		2		
Operational Amplifier		2	3	3
Ethernet		√		
Cryptography		√		
LCD Parallel Data Bus (External Bus Interface)		8	16	16
Package		LQFP 64	LQFP 128	LQFP 144

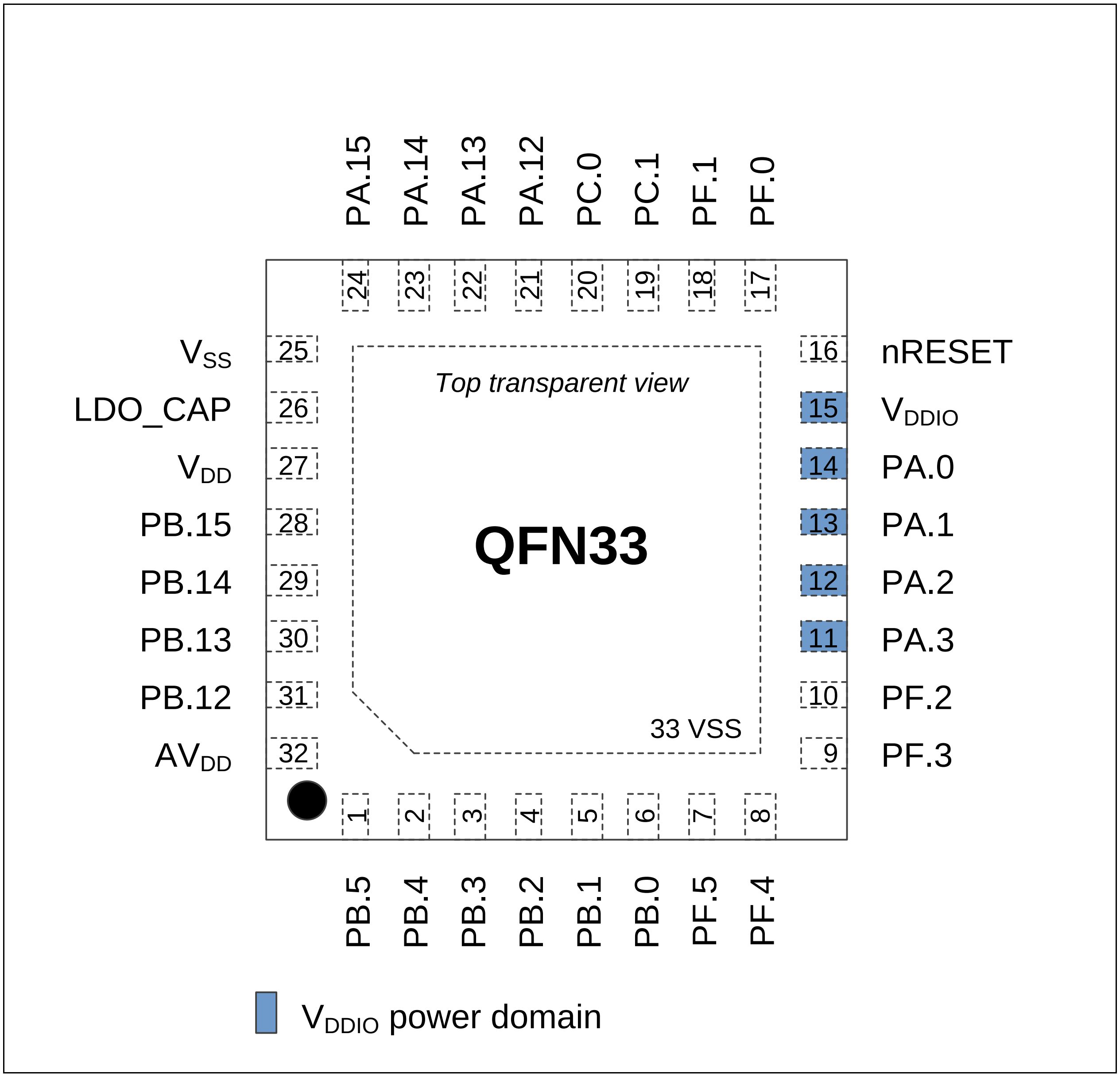
4 PART NUMBERING

M4	81	Z	G	D	A	E
Core	**Series**	**Package**	**Flash Size**	**SRAM Size**	**Revision**	**Temperature**
Cortex®-M4F	81: Base 82: USB FS 83: CAN 84: USB HS 85: Crypto 87: Ethernet	Z: QFN33 (5x5 mm) L: LQFP48 (7x7 mm) C: WLCSP S: LQFP64 (7x7 mm) O: QFN88 (10x10 mm) V: LQFP100 (14x14 mm) K: LQFP128 (14x14 mm) J: LQFP144 (20x20 mm)	A: 8 KB B: 16 KB C: 32 KB D: 64 KB E: 128 KB F: 192 KB G: 256 KB H: 384 KB I: 512 KB	1: 4 KB 2: 8 KB 3: 16 KB 4: 20 KB 5: 24 KB 6: 32 KB 7: 48 KB 8: 64 KB 9: 80 KB A: 96 KB B: 112 KB C: 128 KB D: 160 KB		E:-40°C ~ 105°C

5 PIN CONFIGURATION

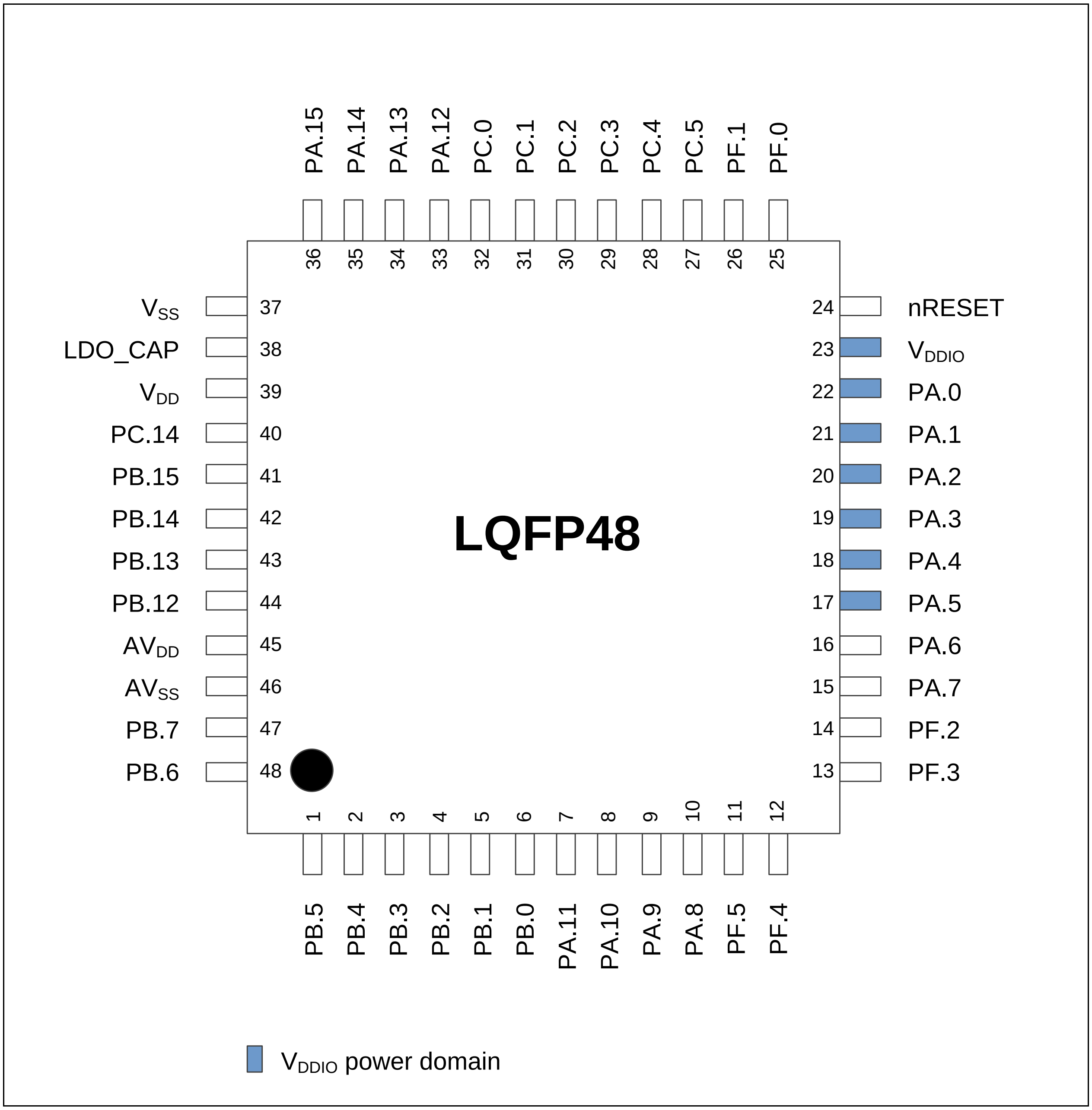
5.1 QFN 33 Pin Diagram

Corresponding Part Number: M481ZGAAE, M481ZIDAE, M482ZIDAE, M485ZIDAE



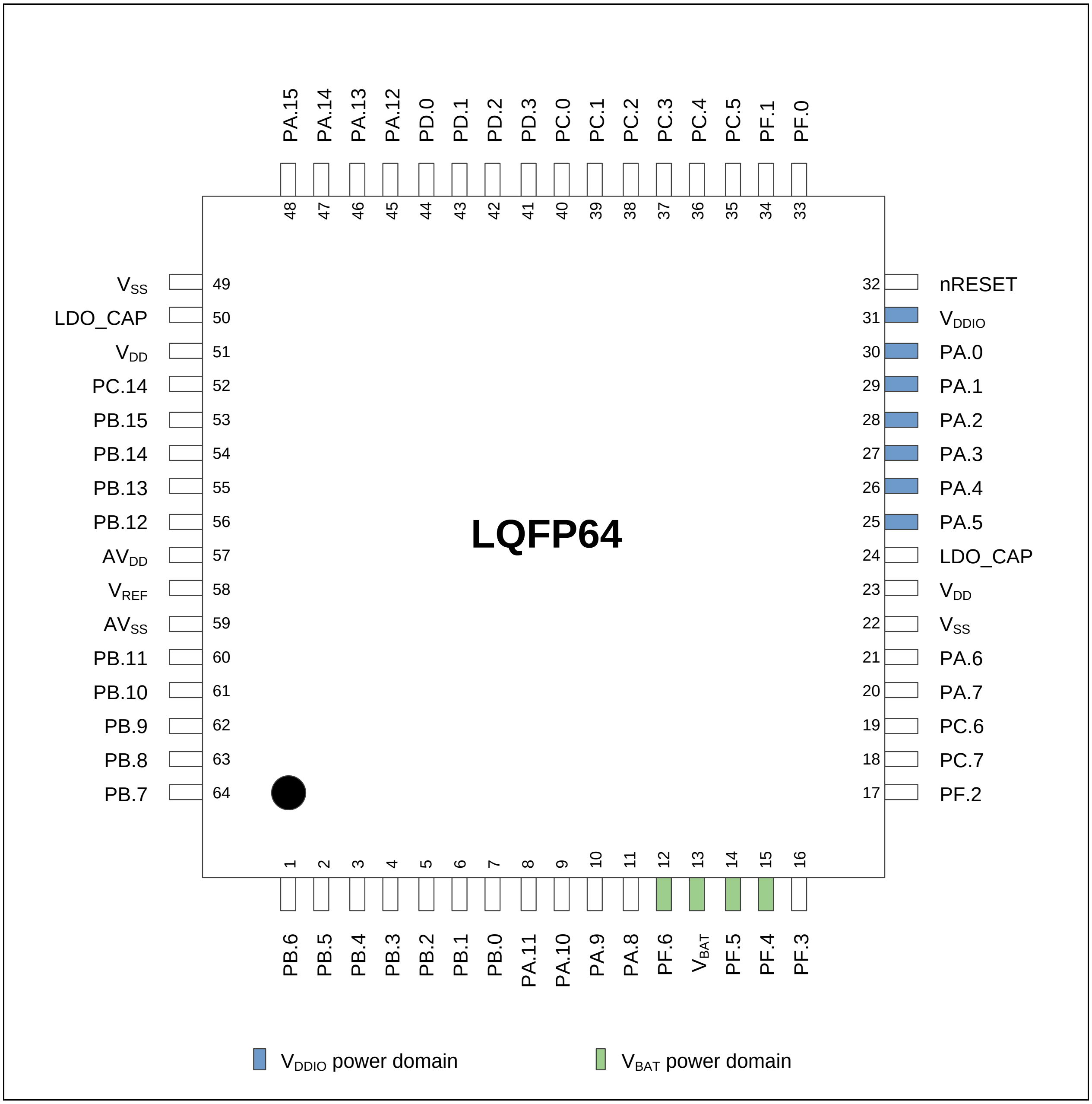
5.2 LQFP-48 Pin Diagram (0/1 USB FS)

Corresponding Part Number: M481LGAAE, M481LIDAE, M482LGAAE, M482LIDAE, M485LIDAE



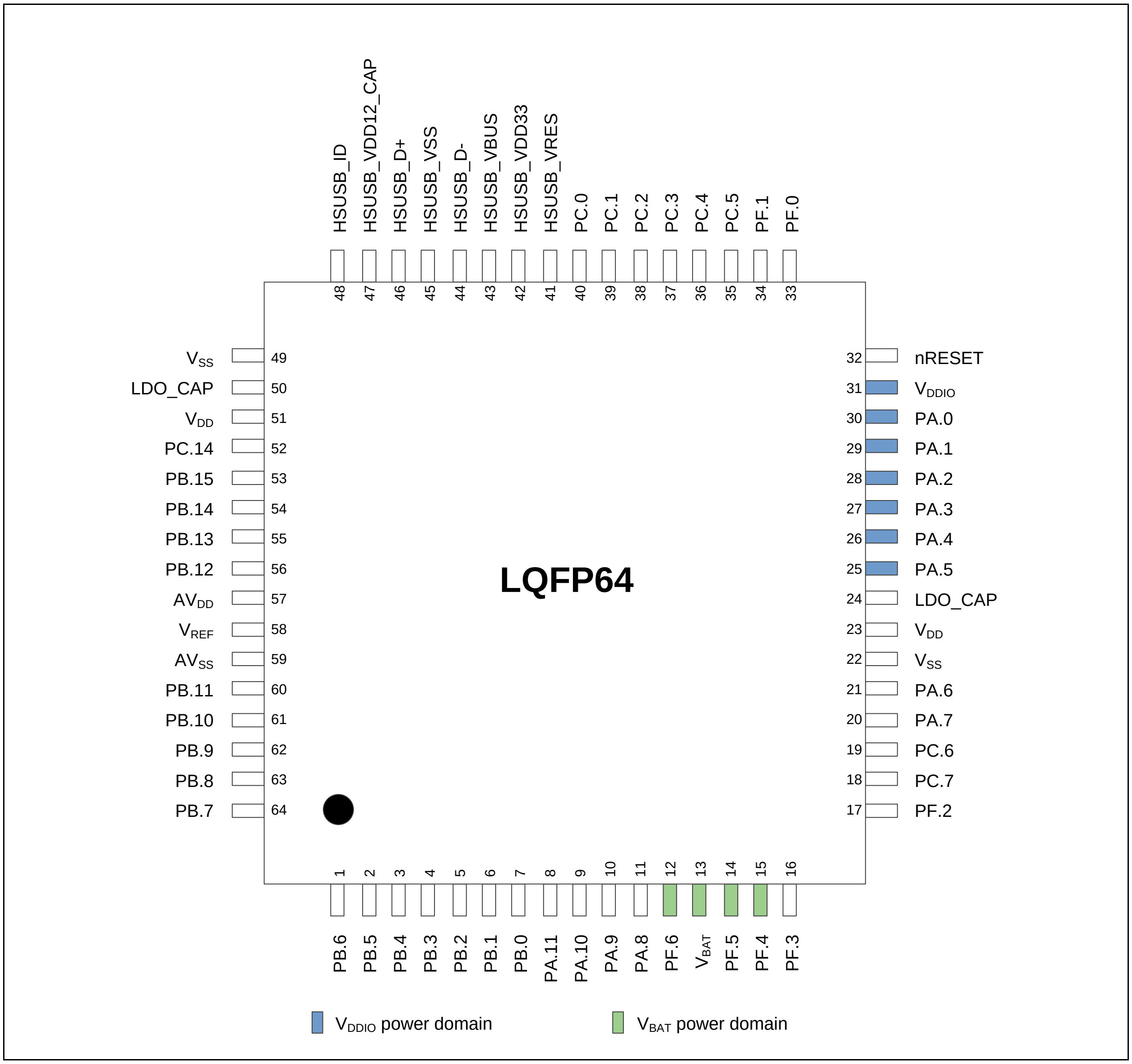
5.3 LQFP-64 Pin Diagram (0/1 USB FS)

Corresponding Part Number: M481SGAAE, M481SIDAE, M482SGAAE, M482SIDAE



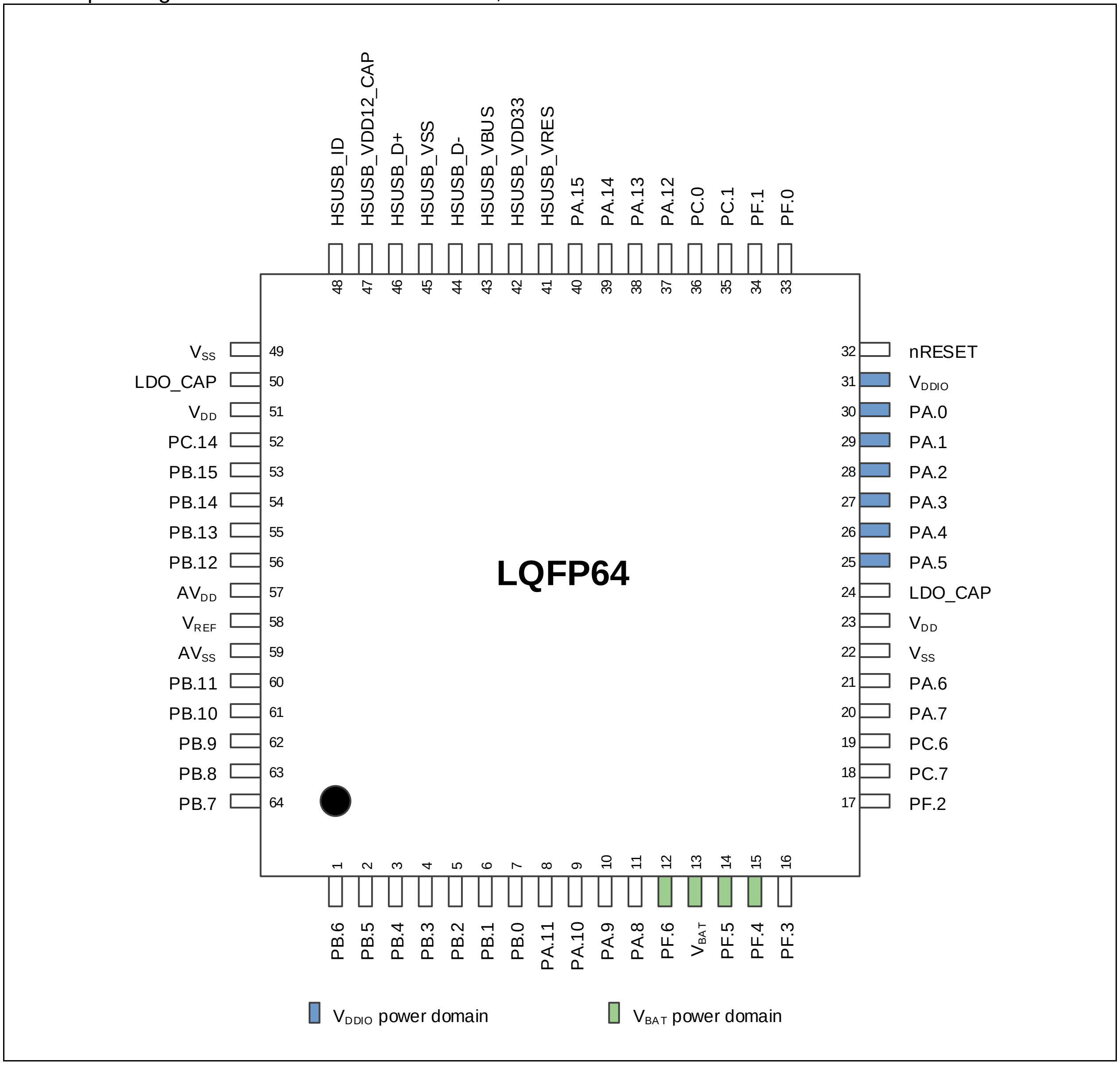
5.4 LQFP-64 Pin Diagram (1 USB HS)

Corresponding Part Number: M483SGAAE, M483SIDAE, M484SGAAE, M484SIDAE, M485SIDAE, M487SIDAE



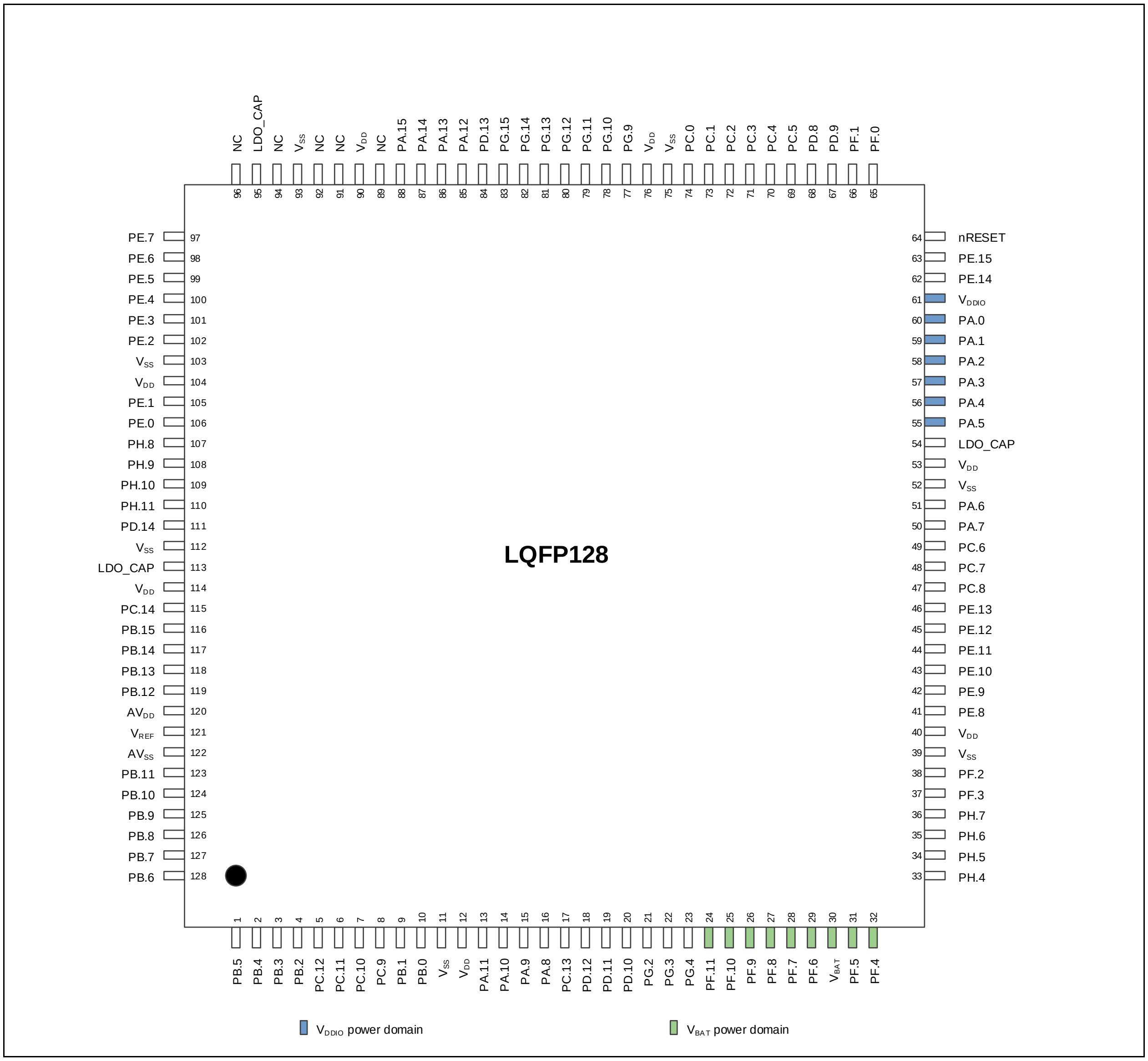
5.5 LQFP-64 Pin Diagram (USB FS + USB HS)

Corresponding Part Number: M484SGAAE2U, M484SIDAE2U



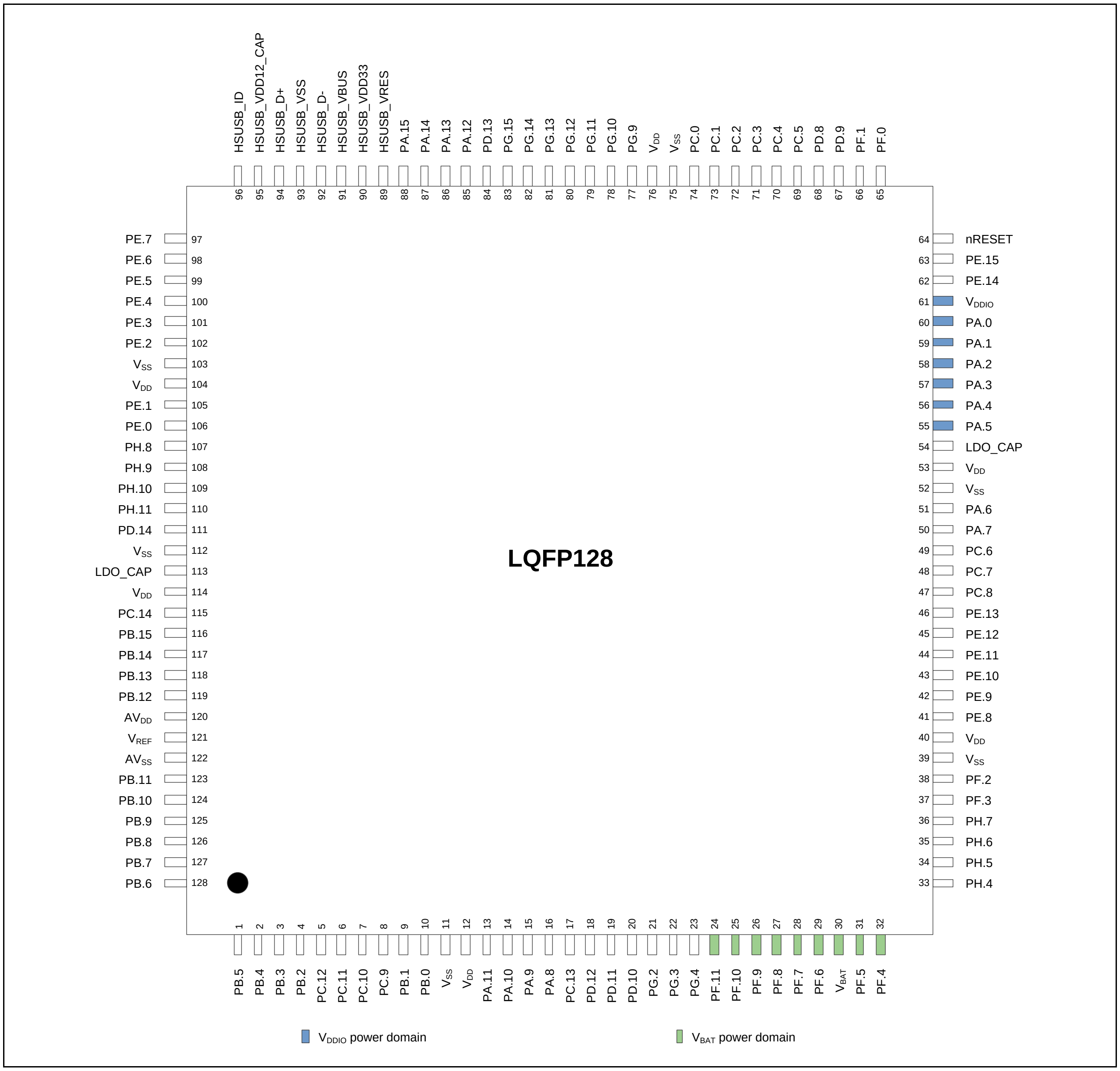
5.6 LQFP-128 Pin Diagram (1 USB FS)

Corresponding Part Number: M482KGAAE, M482KIDAE



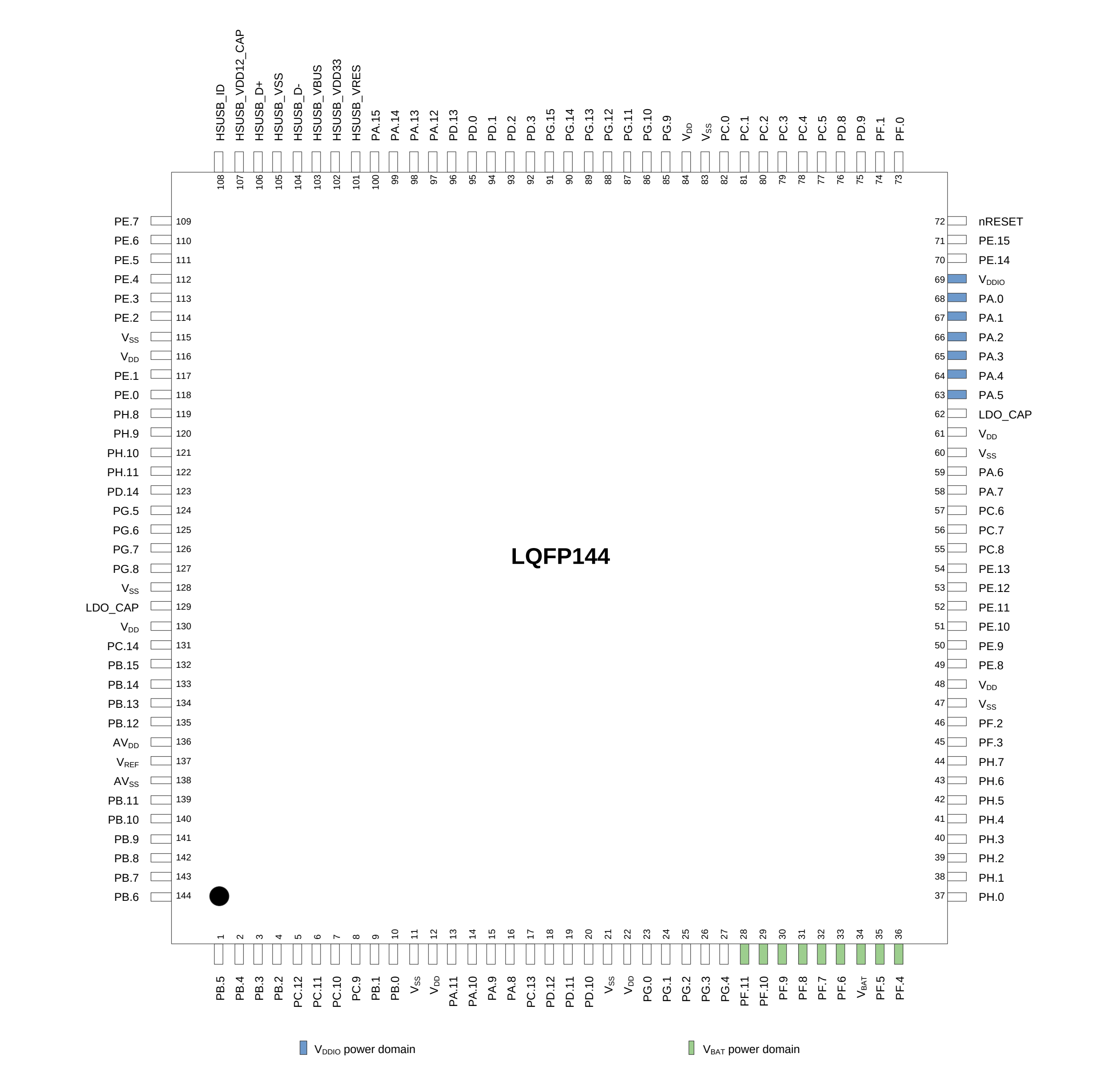
5.7 LQFP-128 Pin Diagram (USB FS + USB HS)

Corresponding Part Number: M483KIDAE, M484KIDAE, M485KIDAE, M487KIDAE



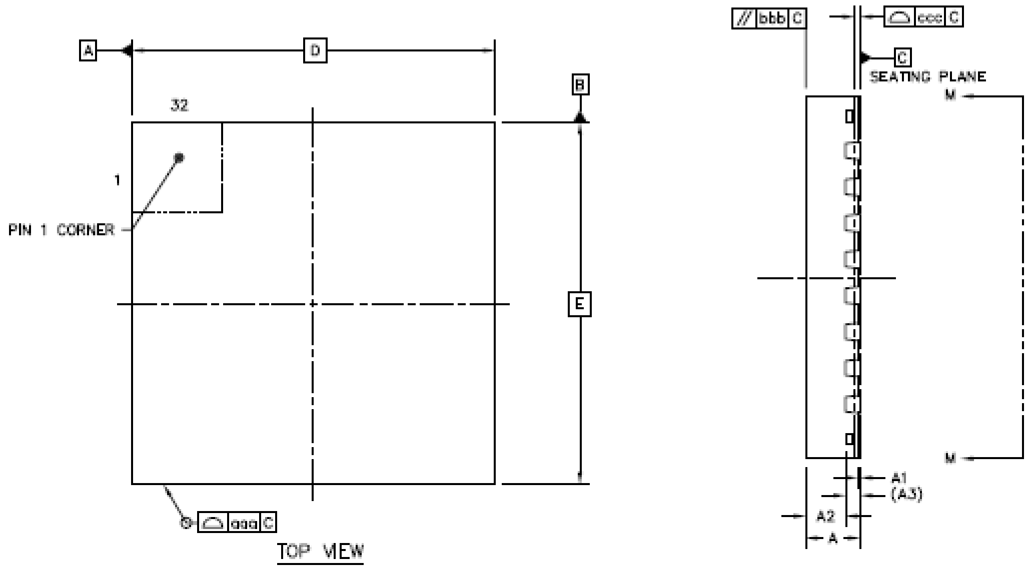
5.8 LQFP-144 Pin Diagram

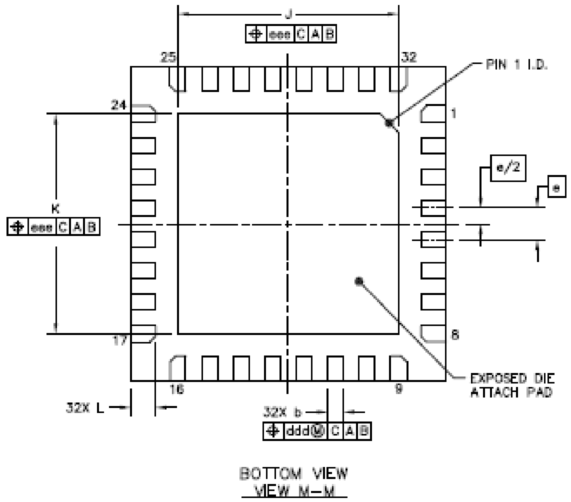
Corresponding Part Number: M487JIDAE



6 PACKAGE DIMENSION

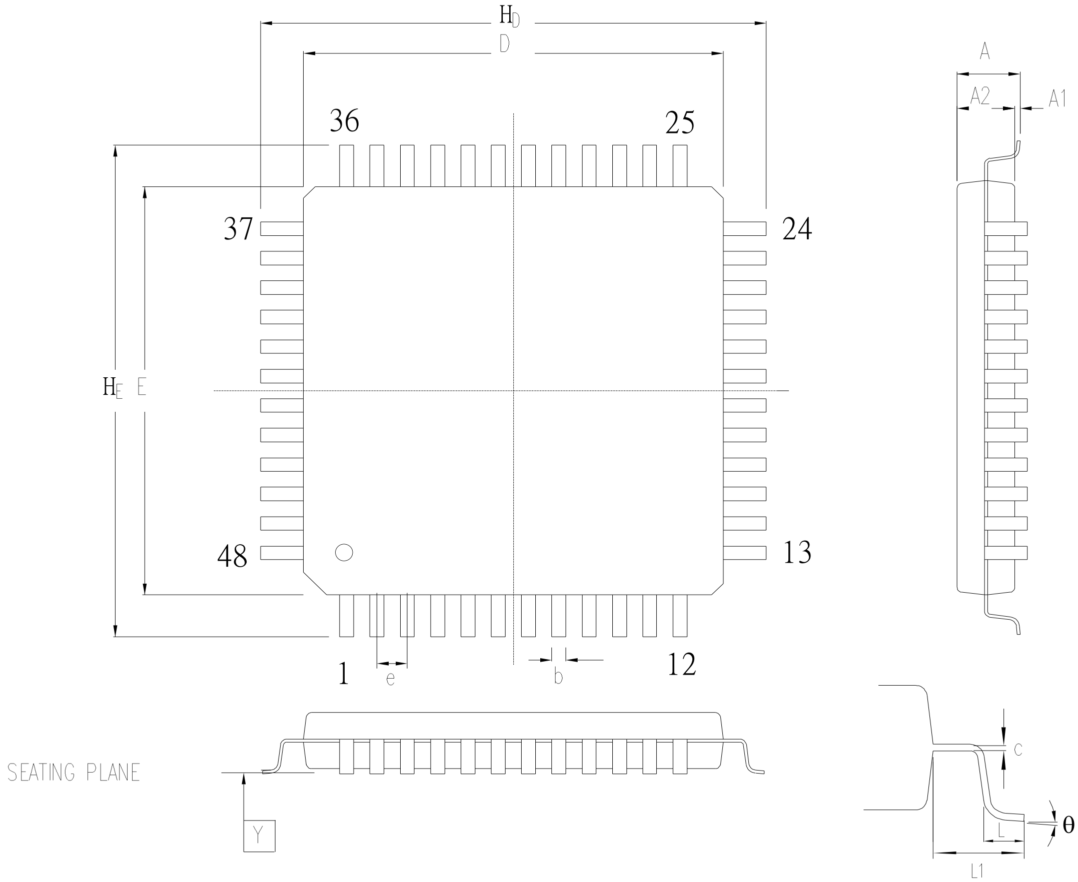
6.1 QFN 33L (5x5x0.8 mm³ Pitch 0.5 mm)





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

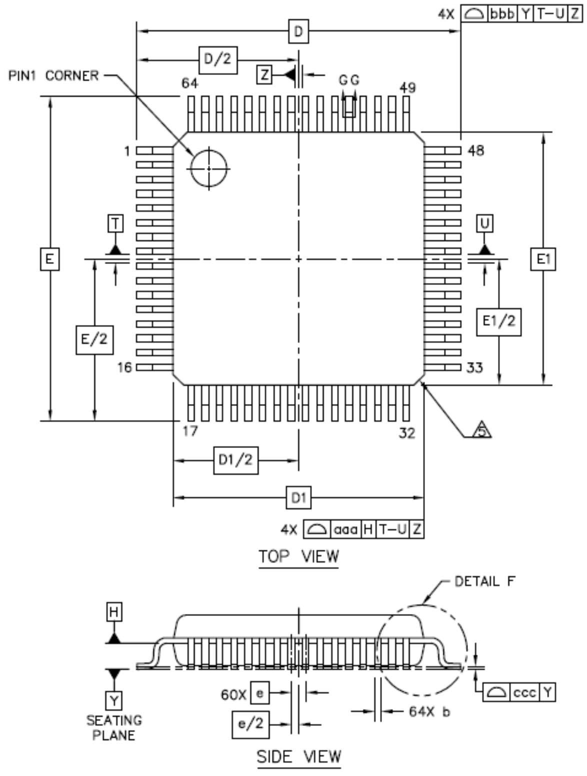
6.2 LQFP 48L (7x7x1.4 mm³ Footprint 2.0mm)



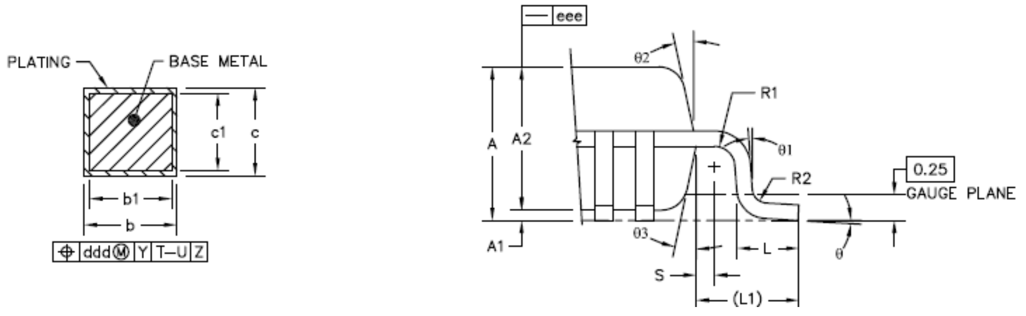
Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

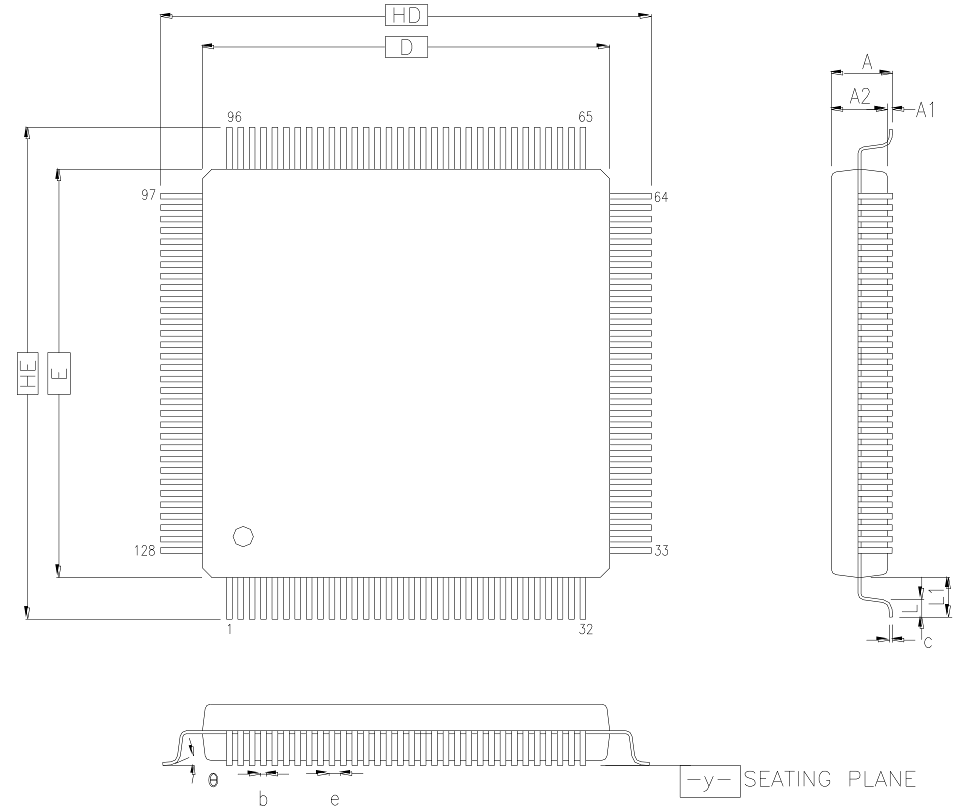
6.3 LQFP 64L (7x7x1.4 mm³ footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
FOOTPRINT		L	0.45	0.6	0.75
		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



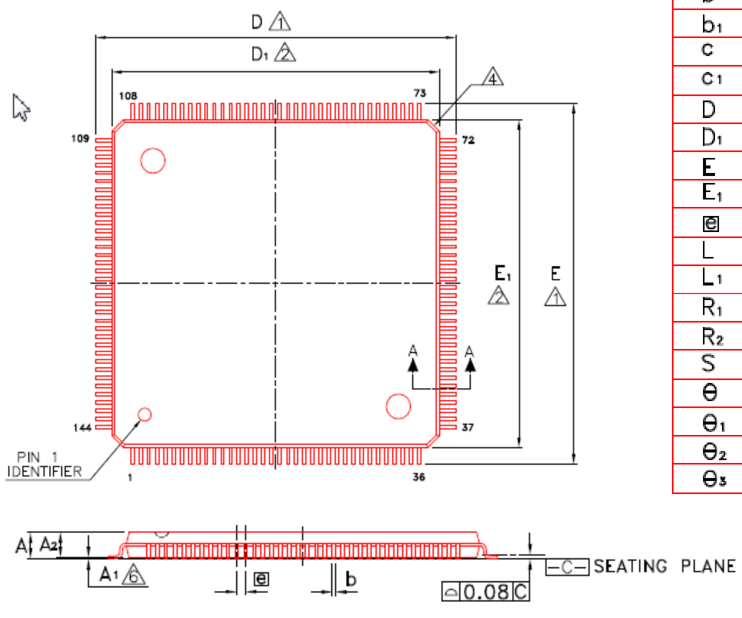
6.4 LQFP 128L (14x14x1.4 mm^3 footprint 2.0 mm)



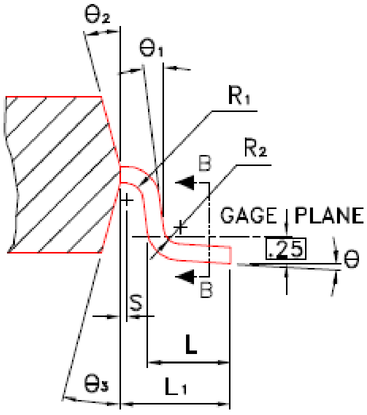
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

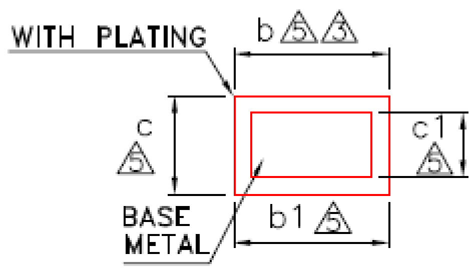
6.5 LQFP 144L (20x20x1.4 mm³ footprint 2.0 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	—	0.002	—	—
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.20 REF			0.008 REF		
c	0.12	—	0.20	0.005	—	0.008
c1	0.13 REF			0.005 REF		
D	21.85	22.00	22.15	0.860	0.866	0.872
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	21.85	22.00	22.15	0.860	0.866	0.872
E1	19.90	20.00	20.10	0.783	0.787	0.791
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.15 REF			0.006 REF		
R2	0.15 REF			0.006 REF		
S	0.19 REF			0.007 REF		
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	7° REF			7° REF		
θ2	12° REF			12° REF		
θ3	12° REF			12° REF		



SECTION A–A



SECTION B–B

7 REVISION HISTORY

Date	Revision	Description
2018.03.01	1.00	Initial version.

Important Notice

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.