# Pro**Labs**

# QDD-400G-ZR-S-C

Cisco<sup>®</sup> QDD-400G-ZR-S Compatible TAA 400GBase-ZR QSFP-DD Transceiver (SMF, Coherent, LC, DOM, ZR)

# Features:

- Hot pluggable QSFP-DD footprint (Type 2A)
- Supports 425Gbps Data Rate
- 8x 26.5625GBd PAM4 Serial Electrical Interface (400GAUI-8, RS (544/514) FEC)
- Duplex LC connector
- Tunable C-band Transmitter
- Coherent Receivers
- C-FEC (15%) with 10.7dB Net Coding Gain
- Up to 120km Point-to-Point Transmission on Single Mode Fibre
- Operating case temperature: -5C to 80C
- Power Dissipation < 18.3W
- Single +3.3V Power Supply
- RoHS Compliant

# **Applications:**

- 400GBase Ethernet
- Access and Enterprise

# **Product Description**

This Cisco<sup>®</sup> QDD-400G-ZR-S compatible QSFP-DD transceiver provides 400GBase-ZR+ throughput up to N/A over single-mode fiber (SMF) using a wavelength of 1528.77nm to 1567.13nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent Cisco<sup>®</sup> transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



Rev. 051523



### **Absolute Maximum Ratings**

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Storage Temperature	Ts	-40		85	°C	
Case Operating Temperature	Тор	-5		80	°C	
Relative Humidity (non-condensing)	RH			85	%	
Optical Receiver Overload				1	dBm	1
Supported Host Signal Types			425		Gbps	2
Line Baud Rate			59.84375		GBd	3

#### Notes:

- 1. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used
- 2. As per IEEE 802.3bs-2017
- 3. 400G DP-16QAM, C-FEC

# **Electrical Characteristics**

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.135	3.3	3.465	V	
Power Supply Current	lcc			6	А	
Power Consumption	PD		15.8	18.3	W	
Power Consumption	PD			1.5	W	1

#### Notes:

1. Low power mode

#### **Optical Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes	
Transmitter							
Average Output Power	Ро	-10	-8.5	-6	dBm	1, 2	
Laser Linewidth				300	kHz		
Transmitter VOA Dynamic Range		10			dB	3	
Output Power Stability		-1		1	dB		
In-Band OSNR		40			dB/0.1nm		
Out-of-Band OSNR		35			dB/0.1nm		
Frequency Range		191.275		196.125	THz	4	
Centre Frequency		ν <sub>T</sub> -1.5	VT	v <sub>T</sub> +1.5	GHz	5	
Channel Spacing		6.25			GHz		
Centre Wavelength Range	Τλ	1528.58		1567.34	nm		
Centre Wavelength	Τλ	λΤ -15	λτ	λΤ +15	pm		
Receiver							
Receiver Operating Wavelength	Rλ	1528.58		1567.34	nm		
Receiver Sensitivity	S			-20	dBm	6	
Receiver Overload	P <sub>OL</sub>	1			dBm	7	
Receiver Input Power Range		-12		1	dBm	8	
Extended Receiver Input Power Range		-15		1	dBm	9	
Acquisition Range		-3.6		3.6	GHz	10	
Upstream Tx Linewidth				500	kHz		
OSNR Tolerance			24	26	dB	11	
Crosstalk Tolerance				7	dB	12	
Chromatic Dispersion Tolerance				2400	ps/nm	13	

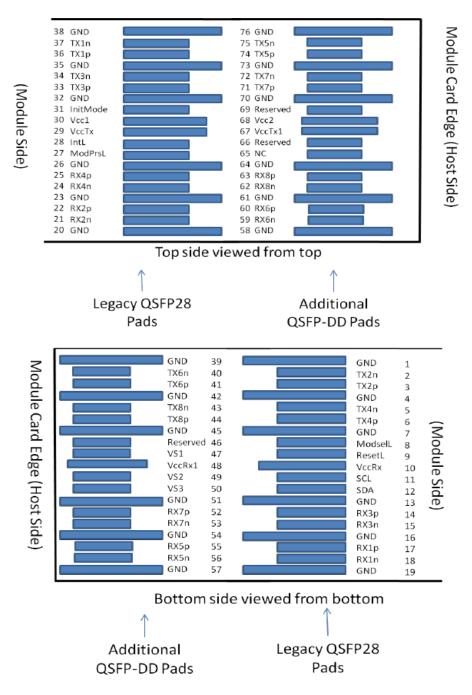
# Notes:

- 1. Output power coupled into a  $9/125 \mu m$  single mode fibre
- 2. The output power is settable in steps of 0.1 dB within the specified wavelength range
- 3. With Tx VOA attenuation set to minimum
- 4. Per ITU-T G.694.1 DWDM grid definition
- 5. Applies also to LO
- 6. Minimum input power needed to achieve post-FEC BER ≤10<sup>-15</sup>, 400G DP-16QAM, OSNR>35dB
- 7. The optical input to the receiver should not exceed this value. Transmitters must never be directly connected to receivers before ensuring that proper optical attenuation is used
- 8. An input power in this range guarantees optimum OSNR performance
- 9. With ≤1dB OSNR tolerance degradation
- 10. Frequency offset between received carrier and LO
- 11. At optimum input power range

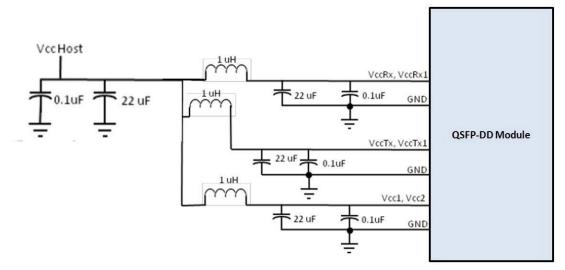
- 12. Ratio of accumulated crosstalk channels to signal power
- 13. Less than 0.5dB receiver sensitivity penalty compared to OSNR>35dB

PinLogicSymbolName/DescriptionsPlug Sequence1GNDGround182CML-ITx2nTransmitter Inverted Data Input383CML-ITx2pTransmitter Non-Inverted Data Input384GNDGround185CML-ITx4nTransmitter Inverted Data Input386CML-ITx4nTransmitter Non-Inverted Data Input387GNDGround188LVTTL-IModiele Select389LVTTL-IResettModule Select3810VcRx+3.3V Power Supply Receiver2811LVCMOS-I/OSCL2-wire serial Interface dock3812LVCMOS-I/OSDA2-wire serial Interface dock3813GNDGround181814CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3nReceiver Inverted Data Output3816GNDGround181817CML-ORx1nReceiver Inverted Data Output3818CML-ORx2nReceiver Inverted Data Output3820GNDGround181821CML-ORx2nReceiver Inverted Data Output3822CML-ORx2nReceiver Inverted Data Output3823GNDGround181824CML-ORx2nReceiver Inverted Data Output38<	Pin Descriptions						
2CML-ITx2nTransmitter Inverted Data Input383CML-ITx2pTransmitter Non-Inverted Data Input384CML-ITx4nTransmitter Inverted Data Input385CML-ITx4nTransmitter Inverted Data Input386CML-ITx4nTransmitter Non-Inverted Data Input387GNDGround188LVTL-IModSelLModule Select389LVTTL-IResetLModule Select3810VCcRx+3.3V Power Supply Receiver2811LVCMOS-I/OSCL2-wire serial interface clock3812LVCMOS-I/OSCL2-wire serial interface clock3813GNDGround181814CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3nReceiver Non-Inverted Data Output3816GNDGround181817CML-ORx1nReceiver Inverted Data Output3818CML-ORx2nReceiver Inverted Data Output3819GNDGround181820GNDGround181821CML-ORx2nReceiver Inverted Data Output3822CML-ORx2nReceiver Inverted Data Output3823GNDGround1824CML-ORx4nReceiver Inverted Data Output3825CML-O <th>Pin</th> <th>Logic</th> <th>Symbol</th> <th>Name/Descriptions</th> <th>Plug Sequence</th>	Pin	Logic	Symbol	Name/Descriptions	Plug Sequence		
3CML-ITx2pTransmitter Non-Inverted Data Input384GNDGroundIB5CML-ITx4nTransmitter Inverted Data Input386CML-ITx4pTransmitter Non-Inverted Data Input387GNDGroundIB8LVTTL-IModSelLModule Select389LVTTL-IResetLModule Reset3810VccRx+3.3V Power Supply Receiver2811LVCMOS-I/OSLL2-wire serial interface clock3812LVCMOS-I/OSDA2-wire serial interface data3813GNDGroundIB1814CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3nReceiver Inverted Data Output3816GNDGroundIB1817CML-ORx1nReceiver Inverted Data Output3818CML-ORx1nReceiver Inverted Data Output3819GNDGroundIB1820GNDGroundIB1821CML-ORx2nReceiver Inverted Data Output3822CML-ORx4nReceiver Inverted Data Output3823GNDGroundIB24CML-ORx4nReceiver Inverted Data Output3825CML-ORx4nReceiver Inverted Data Output3826GNDGroundIB27	1		GND	Ground	18		
4Image: Second seco	2	CML-I	Tx2n	Transmitter Inverted Data Input	ЗВ		
SCML-ITx4nTransmitter Inverted Data Input386CML-ITx4pTransmitter Non-Inverted Data Input387CML-ITx4pTransmitter Non-Inverted Data Input388LVTTL-IModSelLModule Select389LVTTL-IResetLModule Reset3810VcRx+3.3 V Power Supply Receiver2811LVCMOS-I/OSCL2-wire serial Interface dock3812LVCMOS-I/OSDA2-wire serial Interface data3813GNDGround181814CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3pReceiver Inverted Data Output3816GNDGround181817CML-ORx1nReceiver Inverted Data Output3818CML-ORx1nReceiver Inverted Data Output3819GNDGround181820GNDGround181821CML-ORx2nReceiver Inverted Data Output3823CML-ORx2nReceiver Non-Inverted Data Output3824CML-ORx2nReceiver Non-Inverted Data Output3825CML-ORx4nReceiver Non-Inverted Data Output3824CML-ORx4nReceiver Inverted Data Output3825CML-ORx4pReceiver Non-Inverted Data Output3826GNDGround<	3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	ЗВ		
6CML-ITx4pTransmitter Non-Inverted Data Input3B7GNDGroundIB8LVTL-IModSelLModule Select3B9LVTL-IResetLModule Reset3B10VcCRx+3.3V Power Supply Receiver2B11LVCMOS-I/OSCL2-wire serial interface dock3B12LVCMOS-I/OSDA2-wire serial interface data3B13GNDGroundIB3B14CML-ORx3pReceiver Non-Inverted Data Output3B15CML-ORx3nReceiver Non-Inverted Data Output3B16GNDGroundIB1B17CML-ORx1pReceiver Non-Inverted Data Output3B18CML-ORx1pReceiver Non-Inverted Data Output3B19GNDGroundIB1B20GNDGroundReceiver Non-Inverted Data Output3B21CML-ORx1nReceiver Inverted Data Output3B22CML-ORx2nReceiver Inverted Data Output3B23GNDGroundIB3B24CML-ORx4nReceiver Non-Inverted Data Output3B25CML-ORx4nReceiver Non-Inverted Data Output3B26GNDGroundIB3B27LVTL-OModPrsLModule Present3B28LVTL-OInttInterrupt3B29VcC1x+3.3V	4		GND	Ground	18		
7Image: Constraint of Constraint	5	CML-I	Tx4n	Transmitter Inverted Data Input	ЗВ		
8LVTIL-1ModSelLModule Select389LVTIL-1ResetLModule Reset3810VccRx+3.3V Power Supply Receiver2811LVCMOS-I/OSCL2-wire serial interface clock3812LVCMOS-I/OSDA2-wire serial interface clock3813GNDGround1814CML-0Rx3pReceiver Non-Inverted Data Output3815GNLORx3nReceiver Inverted Data Output3816GNDGround181817CML-0Rx1pReceiver Inverted Data Output3818CML-0Rx1nReceiver Inverted Data Output3819GNDGround181820GNDGround183821CML-0Rx2nReceiver Inverted Data Output3822CML-0Rx2nReceiver Inverted Data Output3823GNDGround183824CML-0Rx4nReceiver Inverted Data Output3825CML-0Rx4nReceiver Inverted Data Output3826GNDGround183827LVTL-0NedPrsLModule Present3828LVTL-0IntLInterrupt3829VcC1+3.3V Power supply transmitter2830GNDGroundIntilialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3831LV	6	CML-I	Тх4р	Transmitter Non-Inverted Data Input	3B		
9LVTIL-IResetLModule Reset3810VCCR+3.3V Power Supply Receiver2811LVCMOS-I/OSCL2-wire serial interface clock3812LVCMOS-I/OSDA2-wire serial interface data3813CML-ORx3pReceiver Non-Inverted Data Output3814CML-ORx3pReceiver Inverted Data Output3815CML-ORx3nReceiver Inverted Data Output3816GNDGround181117CML-ORx1nReceiver Non-Inverted Data Output3818CML-ORx1nReceiver Inverted Data Output3819GNDGround181820CML-ORx1nReceiver Inverted Data Output3821CML-ORx1nReceiver Inverted Data Output3822CML-ORx2nReceiver Inverted Data Output3823GNDGround183824CML-ORx4nReceiver Inverted Data Output3825CML-ORx4pReceiver Inverted Data Output3826GNDGround183827LVTIL-OModPrsLModule Present3828LVTIL-OIntLInterrupt3829VccTx+3.3V Power supply transmitter2830IVTIL-IInitModeIniterization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3832GND <th>7</th> <th></th> <th>GND</th> <th>Ground</th> <th>18</th>	7		GND	Ground	18		
10VccRx+3.3V Power Supply Receiver2811LVCMOS-I/OSCL2-wire serial interface clock3812LVCMOS-I/OSDA2-wire serial interface data3813CML-OSDA2-wire serial interface data3814CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3nReceiver Inverted Data Output3816GNDGround18	8	LVTTL-I	ModSelL	Module Select	3B		
11LVCMOS-I/OSCL2-wire serial interface clock3812LVCMOS-I/OSDA2-wire serial interface data3813CML-OSNDGround1814CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3nReceiver Inverted Data Output3816GNDGround18	9	LVTTL-I	ResetL	Module Reset	ЗВ		
12LVCMOS-I/OSDA2-wire serial interface data3813GNDGroundIB14CML-0Rx3pReceiver Non-Inverted Data Output3815CML-0Rx3nReceiver Inverted Data Output3816GNDGroundIB17CML-0Rx1pReceiver Inverted Data Output3818CML-0Rx1nReceiver Inverted Data Output3819CML-0Rx1nReceiver Inverted Data Output3820GNDGroundGround1821CML-0Rx2nReceiver Inverted Data Output3822CML-0Rx2nReceiver Inverted Data Output3823GNDGround183824CML-0Rx2nReceiver Inverted Data Output3825CML-0Rx4nReceiver Inverted Data Output3826GNDGround183827LVTL-0Rx4nReceiver Inverted Data Output3828CML-0Rx4nReceiver Non-Inverted Data Output3829CML-0Rx4nReceiver Non-Inverted Data Output3828LVTL-0IntLInterrupt3829LVTL-0ModPrsLModule Present3829Vcc1x+3.3V Power supply transmitter2830LVTL-1Initialization mode; In legacy QSFP applications, the InitMode pails called LPMODE31LVTL-1Initialization mode; In legacy Q	10		VccRx	+3.3V Power Supply Receiver	2B		
13GNDGround1B14CML-ORx3pReceiver Non-Inverted Data Output3815CML-ORx3nReceiver Inverted Data Output3816GNDGround1817CML-ORx1pReceiver Non-Inverted Data Output3818CML-ORx1nReceiver Inverted Data Output3819GNDGroundIB20GNDGroundIB21CML-ORx2nReceiver Inverted Data Output3822CML-ORx2nReceiver Inverted Data Output3823GNDGroundIB24CML-ORx2nReceiver Inverted Data Output3825CML-ORx4nReceiver Inverted Data Output3826GNDGroundIB27LVTL-ORx4nReceiver Inverted Data Output3826GNDGroundIB27LVTL-ONddPrsLModule Present3828LVTL-OIntLInterrupt3829Vcc1x+3.3V Power supply transmitter2830Vcc1+3.3V Power supply2831LVTL-IInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE38CML-ITx3pTransmitter Non-Inverted Data Input3834CML-ITx3pTransmitter Inverted Data Input38	11	LVCMOS-I/O	SCL	2-wire serial interface clock	ЗВ		
14CML-ORx3pReceiver Non-Inverted Data Output3B15CML-ORx3nReceiver Inverted Data Output3B16GNDGround1BI17CML-ORx1pReceiver Non-Inverted Data Output3B18CML-ORx1nReceiver Inverted Data Output3B19Image: Composition of Composi	12	LVCMOS-I/O	SDA	2-wire serial interface data	3B		
15CML-ORx3nReceiver Inverted Data Output3816GNDGround1B1117CML-ORx1pReceiver Non-Inverted Data Output3818CML-ORx1nReceiver Inverted Data Output3819CML-ORx1nReceiver Inverted Data Output3820GNDGroundIB1820CML-ORx2nReceiver Inverted Data Output3821CML-ORx2nReceiver Inverted Data Output3822CML-ORx2pReceiver Inverted Data Output3823CML-ORx4nReceiver Inverted Data Output3824CML-ORx4pReceiver Inverted Data Output3825CML-ORx4pReceiver Inverted Data Output3826CML-ORx4pReceiver Non-Inverted Data Output3825CML-ORx4pReceiver Non-Inverted Data Output3826CML-ORx4pReceiver Non-Inverted Data Output3827LVTTL-OModule Present3828LVTTL-OIntlInterrupt3829VccTx+3.3V Power supply transmitter2830Vcc1+3.3V Power supply2831LVTTL-IInitModeGround1833CML-ITransmitter Non-Inverted Data Input3834CML-ITx3nTransmitter Inverted Data Input38	13		GND	Ground	18		
16GNDGround1BImage: constraint of the section of the sectio	14	CML-O	Rx3p	Receiver Non-Inverted Data Output	ЗВ		
17CML-0Rx1pReceiver Non-Inverted Data Output3B18CML-0Rx1nReceiver Inverted Data Output3B19GNDGroundIB20GNDGNDGround1B21CML-0Rx2nReceiver Inverted Data Output3B22CML-0Rx2pReceiver Non-Inverted Data Output3B23GNDGround1B24CML-0Rx4nReceiver Inverted Data Output3B25CML-0Rx4pReceiver Inverted Data Output3B26GNDGround1B27LVTTL-0ModPrsLModule Present3B28LVTTL-0IntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTL-IInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	15	CML-O	Rx3n	Receiver Inverted Data Output	ЗВ		
18CML-ORx1nReceiver Inverted Data Output3B19GNDGroundIB20GNDGroundIB21CML-ORx2nReceiver Inverted Data Output3B22CML-ORx2pReceiver Non-Inverted Data Output3B23GNDGroundIB24CML-ORx4nReceiver Inverted Data Output3B25CML-ORx4nReceiver Inverted Data Output3B26GNDGroundIB3B27LVTTL-OModPrsLModule Present3B28LVTTL-OIntlInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32CML-ITx3pTransmitter Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	16	GND	Ground	1B			
19GNDGround1B20GNDGroundIB21CML-ORx2nReceiver Inverted Data Output3B22CML-ORx2pReceiver Inverted Data Output3B23GNDGroundIB24CML-ORx4nReceiver Inverted Data Output3B25CML-ORx4pReceiver Non-Inverted Data Output3B26GNDGroundIB27LVTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B		
20GNDGround1B21CML-ORx2nReceiver Inverted Data Output3B22CML-ORx2pReceiver Non-Inverted Data Output3B23GNDGroundIB24CML-ORx4nReceiver Inverted Data Output3B25CML-ORx4pReceiver Inverted Data Output3B26GNDGroundIB3B27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32CML-ITx3pTransmitter Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	18	CML-O	Rx1n	Receiver Inverted Data Output	3B		
21CML-0Rx2nReceiver Inverted Data Output3B22CML-0Rx2pReceiver Non-Inverted Data Output3B23GNDGroundIB24CML-0Rx4nReceiver Inverted Data Output3B25CML-0Rx4pReceiver Non-Inverted Data Output3B26GNDGroundIB27LVTL-0ModPrsLModule Present3B28LVTL-0IntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1st.3V Power supply2B31LVTTL-1Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGroundIB33CML-1Tx3pTransmitter Non-Inverted Data Input3B34CML-1Tx3nTransmitter Inverted Data Input3B	19		GND	Ground	18		
22CML-ORx2pReceiver Non-Inverted Data Output3B23GNDGround1B24CML-ORx4nReceiver Inverted Data Output3B25CML-ORx4pReceiver Non-Inverted Data Output3B26GNDGroundIB27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	20		GND	Ground	1B		
23GNDGround1B24CML-ORx4nReceiver Inverted Data Output3B25CML-ORx4pReceiver Non-Inverted Data Output3B26GNDGroundIB27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGroundIB33CML-ITx3pTransmitter Non-Inverted Data Input3B	21	CML-O	Rx2n	Receiver Inverted Data Output	3B		
24CML-ORx4nReceiver Inverted Data Output3B25CML-ORx4pReceiver Non-Inverted Data Output3B26GNDGroundIB27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGroundIB33CML-ITx3pTransmitter Inverted Data Input3B	22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B		
25CML-ORx4pReceiver Non-Inverted Data Output3B26GNDGroundIB27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGroundIB33CML-ITx3pTransmitter Inverted Data Input3B	23		GND	Ground	18		
26GNDGround1B27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	24	CML-O	Rx4n	Receiver Inverted Data Output	3B		
27LVTTL-OModPrsLModule Present3B28LVTTL-OIntLInterrupt3B29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitiModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGroundIB33CML-ITx3pTransmitter Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B		
28LVTTL-OIntLInterrupt3B29VcCTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	26		GND	Ground	1B		
29VccTx+3.3V Power supply transmitter2B30Vcc1+3.3V Power supply2B31LVTTL-IInitiAlization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	27	LVTTL-O	ModPrsL	Module Present	3B		
30Vcc1+3.3V Power supply2B31LVTTL-IInitModeInitialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	28	LVTTL-0	IntL	Interrupt	3B		
31LVTTL-IInitiAlization mode; In legacy QSFP applications, the InitMode pad is called LPMODE3B32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	29		VccTx	+3.3V Power supply transmitter	2B		
32GNDGround1B33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	30		Vcc1		2B		
33CML-ITx3pTransmitter Non-Inverted Data Input3B34CML-ITx3nTransmitter Inverted Data Input3B	31	LVTTL-I		called LPMODE			
34 CML-I Tx3n Transmitter Inverted Data Input 3B			GND				
	33		Тх3р	•	3B		
35 GND Ground 1B	34	CML-I	Tx3n	Transmitter Inverted Data Input	3B		
	35		GND	Ground	18		
36     CML-I     Tx1p     Transmitter Non-Inverted Data Input     3B	36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B		

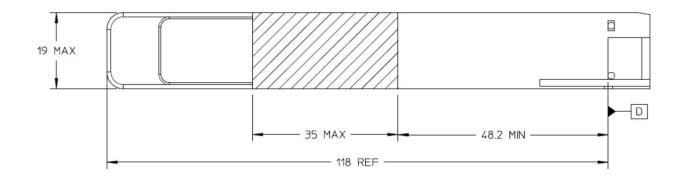
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Тх6р	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Тх8р	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
67		GND	Ground	1A
68		NC	No Connect	3A
69		Reserved	For future use	3A
70		VccTx1	3.3V Power Supply	2A
71		Vcc2	3.3V Power Supply	2A
72		Reserved	For Future Use	3A
73		GND	Ground	1A
74	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx7n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

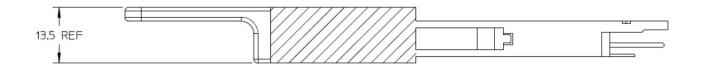


# **Recommended Power Supply Filter**



# **Mechanical Specifications**





#### **About ProLabs**

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

#### **Complete Portfolio of Network Solutions**

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

# **Trusted Partner**

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.



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