

## **Customer Information Notification**

2020120021: i.MX 8 QuadMax/QuadPlus Automotive Datasheet Rev1

**Note:** This notice is NXP Company Proprietary.

Issue Date: Jan 10, 2021 Effective date: Jan 11, 2021

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#### **Management summary**

NXP Semiconductors is announcing datasheet revisions for i.MX 8QuadMax and i.MX 8QuadPlus Automotive products.

NXP has made several changes and clarifications which are in the new datasheet.

All changes to the datasheet can be seen in the revision history section at the end of the document.

### **Change Category**

Fab Process	[]Assembly Process	[]Product Marking	[]Test Process	[]Design
[]Wafer Fab Materials	[]Assembly Materials	[]Mechanical Specification	[]Test Equipment	[]Errata
[]Wafer Fab Location	[]Assembly Location	[]Packing/Shipping/Labeling	[]Test Location	[X]Electrical spec./Test coverage
[]Firmware	[]Other			

### **PCN** Overview

### **Description**

NXP Semiconductors is announcing datasheet revisions from Rev0 to Rev1 for i.MX 8QuadMax and i.MX 8QuadPlus Automotive products.

NXP has made several changes and clarifications are in the new datasheet.

All changes to the datasheet can be seen in the revision history section at the end of the document.

The new Rev1 datasheets are attached and will be located here on NXP.com:

 $https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors: IMX\_HOME$ 

Corresponding ZVEI Delta Qualification Matrix ID: SEM-DS-02.

For customers who have special part numbers, contact your NXP marketing or sales representative for additional ordering information.

#### Reason

The following changes were revised in the datasheets:

Removed MLB specifications. Added note in several places that MLB functionality is not supported.

Table 1? Removed MLB

Figure 1 ? Removed block that referenced MLB and DTCP.

Table 4? Removed MLB.

Table 6 ? Added HDMI note at bottom of page 17.

Table 8 ? Updated footnote 4 since SATA is now supported but HDMI-RX is not. Added MLB footnotes 5 and 6.

Table 9? Added sentence to footnote 5 concerning EMI/EMC.

Table 10? Added MLB footnotes 1 and 2.

Table 15 ? Added MLB footnotes 1 and 2. Will change ?used to determine? to ?used as determined by.?

Table 22 ? Changed last row from PCle gen3 to PCle gen1. (fixed error)

Section 4.5.3? Added new HDMI DC section. Added Table 37 per IC Design spec.

Section 4.7 ? Removed reference to MLB.

Table 52 ? LPDDR4: Added row to table that defines Number of Address Rows supported is 16 (R0-R15).

Table 92 ? Added 2 sentences to footnote 1 concerning PCle compliancy (Gen1/2) and capability (Gen3).

Table 124 ? Removed QSPI1 row (fixed error because not boot source)

Table 125 ? Updated footnote 1 since SATA is now supported but HDMI-RX is not. Added MLB footnotes 2 and 3.

Table 126 ? Updated footnote 3 since SATA is now supported but HDMI-RX is not. Added MLB footnotes 4 and 5.

Section 4.6.1 ? New section that is an improved description of overshoot and undershoot limitations. Table 6 refers to the new section, as well as footnotes of 9 other tables. 4.6.1 corrects an error in a Table 6 footnote with 400 mV changed to 350 mV in the new section. All other tables spec?d 300 or 350 mV in the previous revision; the new spec relaxes or matches the previous data sheet. The new section aligns with the JEDEC LPDDR4 spec and Samsung TFSOI spec.

#### **Identification of Affected Products**

Product identification does not change

### Anticipated Impact on Form, Fit, Function, Reliability or Quality

No Impact on form, fit, function, reliability or quality

### **Data Sheet Revision**

A new datasheet will be issued

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# **Contact and Support**

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

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NXP Quality Management Team.

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**NXP Semiconductors** 

High Tech Campus, 5656 AG Eindhoven, The Netherlands

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#### **Affected Part Numbers**

MIMX8QM5AVUFFAB

MIMX8QM6AVUFFAB

MIMX8QP5AVUFFAB

MIMX8QP6AVUFFAB

MIMX8QM6AVUFFABR

MIMX8QM3AVUFFAB

MIMX8QM4AVUFFAB

MIMX8QM5CVUFFAB

MIMX8QM6CVUFFAB

MIMX8QP3AVUFFAB

MIMX8QP4AVUFFAB

MIMX8QP5CVUFFAB

MIMX8QP6CVUFFAB