GE06MPS06E
650V 6A SiC Schottky MPS™ Diode

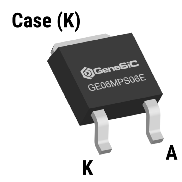
Silicon Carbide Schottky Diode

V_{RRM}	=	650 V
I_F (T_C = 163°C)	=	6 A
Q_C	=	15 nC

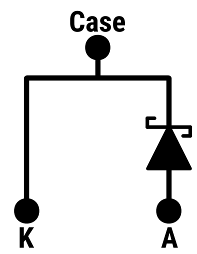
Features

- Gen5 Thin Chip Technology for Low V_F
- Low Conduction Losses for All Load Conditions
- Superior Figure of Merit Q_C/I_F
- Enhanced Surge Current Robustness
- Low Thermal Resistance
- Temperature Independent Fast Switching
- Positive Temperature Coefficient of V_F
- High dV/dt Ruggedness

Package



TO-252-2



RoHS

REACH

Advantages

- Optimal Price Performance
- Improved System Efficiency
- Enables Extremely Fast Switching
- Reduced Cooling Requirements
- Increased System Power Density
- Zero Reverse Recovery Current
- Easy to Parallel without Thermal Runaway
- High System Reliability

Applications

- Switched Mode Power Supply (SMPS)
- Solar Inverter
- Server and Telecom Power Supply
- Battery Charger
- Uninterruptible Power Supply (UPS)

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Repetitive Peak Reverse Voltage	V_{RRM}		650	V	
Continuous Forward Current	I_F	T_C = 100°C, D = 1 T_C = 135°C, D = 1 T_C = 163°C, D = 1	17 12 6	A	Fig. 4
Non-Repetitive Peak Forward Surge Current, Half Sine Wave	$I_{F,SM}$	T_C = 25°C, t_P = 10 ms T_C = 150°C, t_P = 10 ms	33 27	A	
Repetitive Peak Forward Surge Current, Half Sine Wave	$I_{F,RM}$	T_C = 25°C, t_P = 10 ms T_C = 150°C, t_P = 10 ms	20 14	A	
Non-Repetitive Peak Forward Surge Current	$I_{F,MAX}$	T_C = 25°C, t_P = 10 µs	165	A	
i^2t Value	$\int i^2 dt$	T_C = 25°C, t_P = 10 ms	5.445	A^2s	
Non-Repetitive Avalanche Energy	E_{AS}	L = 4.4 mH, I_{AS} = 6 A	79	mJ	
Diode Ruggedness	dV/dt	V_R = 0 ~ 520 V	200	V/ns	
Power Dissipation	P_{TOT}	T_C = 25°C	133	W	Fig. 3
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

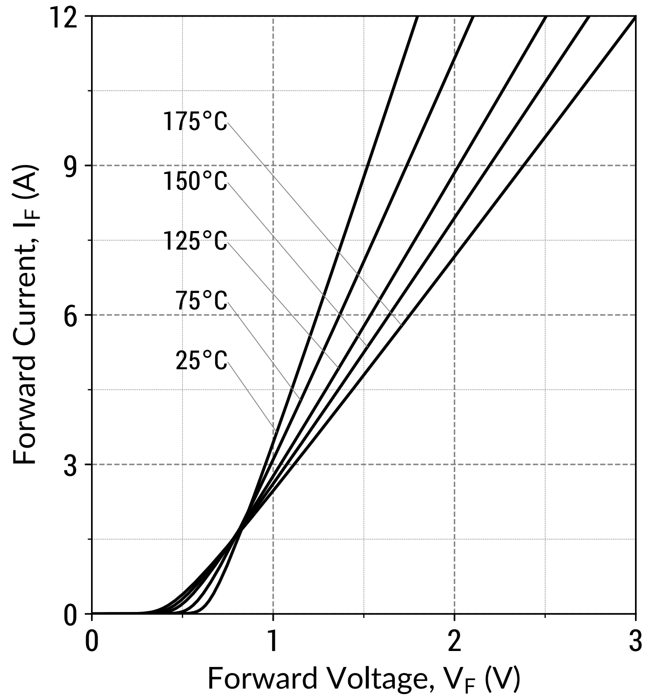
Electrical Characteristics

Parameter	Symbol	Conditions		Values Min.	Values Typ.	Values Max.	Unit	Note
Diode Forward Voltage	V_F	I_F = 6 A, T_j = 25°C			1.25	1.35	V	Fig. 1
		I_F = 6 A, T_j = 150°C			1.64			
Reverse Current	I_R	V_R = 650 V, T_j = 25°C			1	5	μA	Fig. 2
		V_R = 650 V, T_j = 150°C			42			
Total Capacitive Charge	Q_C	$I_F \leq I_{F,MAX}$ dI_F/dt = 200 A/μs	V_R = 200 V		10		nC	Fig. 7
			V_R = 400 V		15			
Switching Time	t_S		V_R = 200 V		< 10		ns	
			V_R = 400 V					
Total Capacitance	C	V_R = 1 V, f = 1MHz			279		pF	Fig. 6
		V_R = 400 V, f = 1MHz			20			

Thermal/Package Characteristics

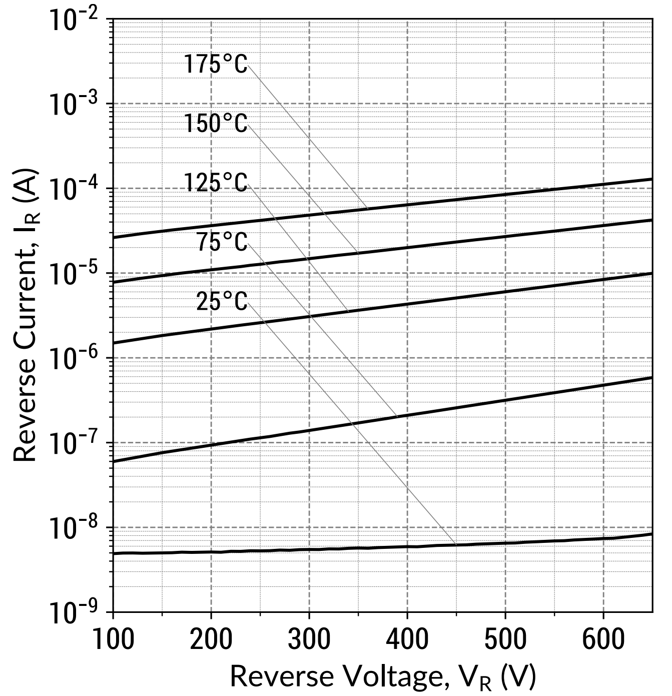
Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Thermal Resistance, Junction - Case	R_{thJC}			1.13		°C/W	Fig. 9
Weight	W_T			0.3		g	

Figure 1: Typical Forward Characteristics



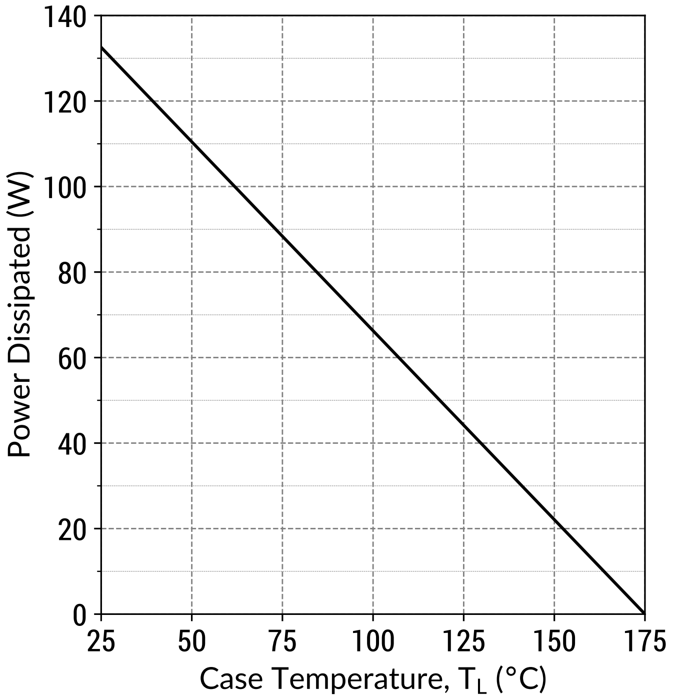
$I_F = f(V_F,T_j)$; t_P = 250 µs

Figure 2: Typical Reverse Characteristics



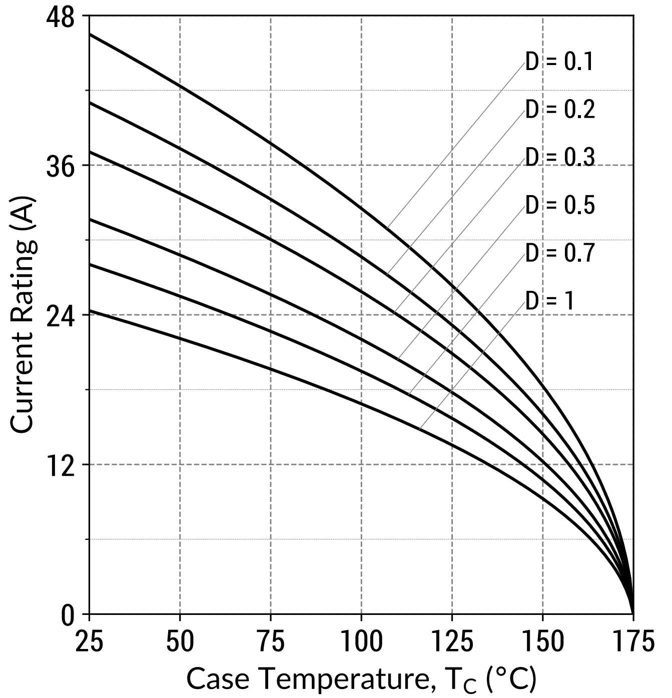
$I_R = f(V_R,T_j)$

Figure 3: Power Derating Curves



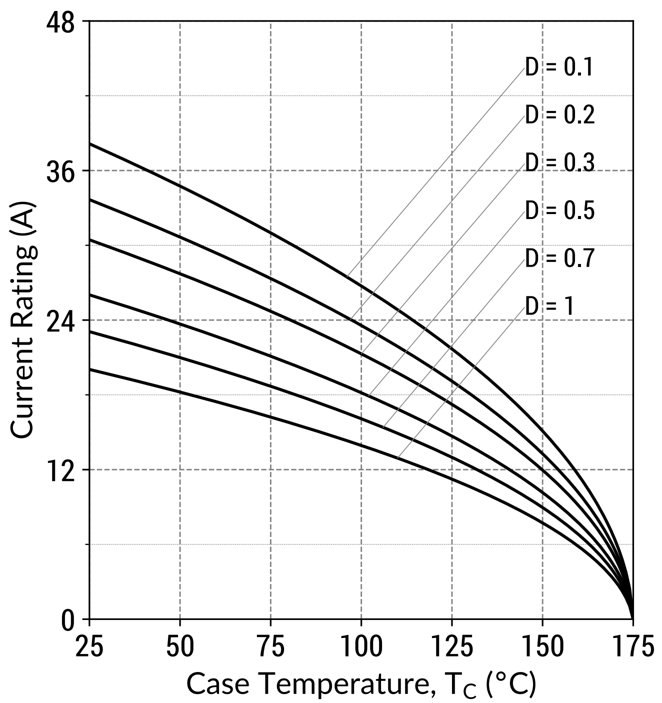
$P_{TOT} = f(T_C)$; T_j = 175°C

Figure 4: Current Derating Curves (Typical V_F)



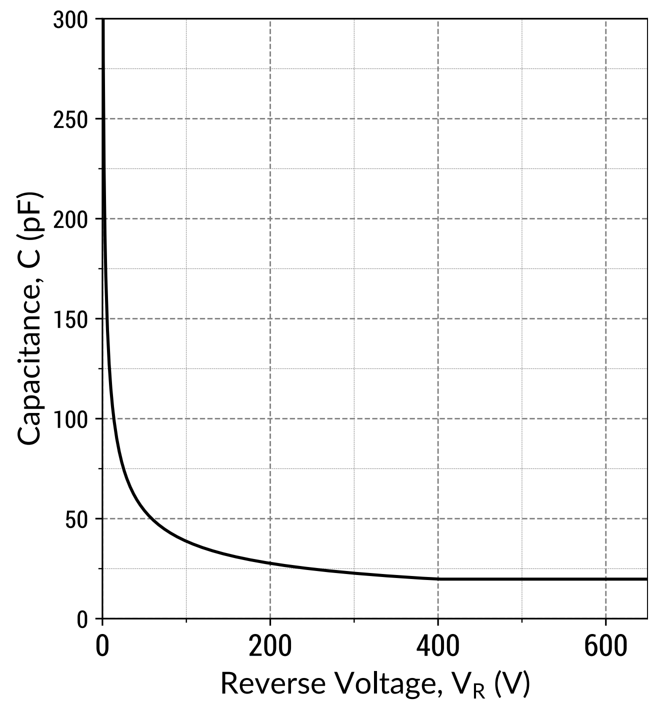
$I_F = f(T_C)$; $D = t_P/T$; $T_j \leq$ 175°C; f_{SW} > 10kHz

Figure 5: Current Derating Curves (Maximum V_F)



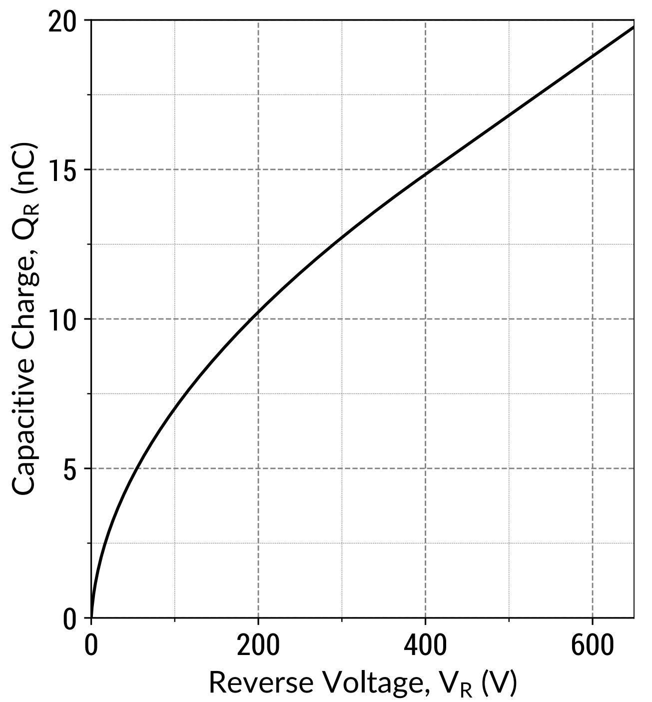
$I_F = f(T_C)$; $D = t_P/T$; $T_j \leq 175°C$; $f_{SW} > 10kHz$

Figure 6: Typical Junction Capacitance vs Reverse Voltage Characteristics



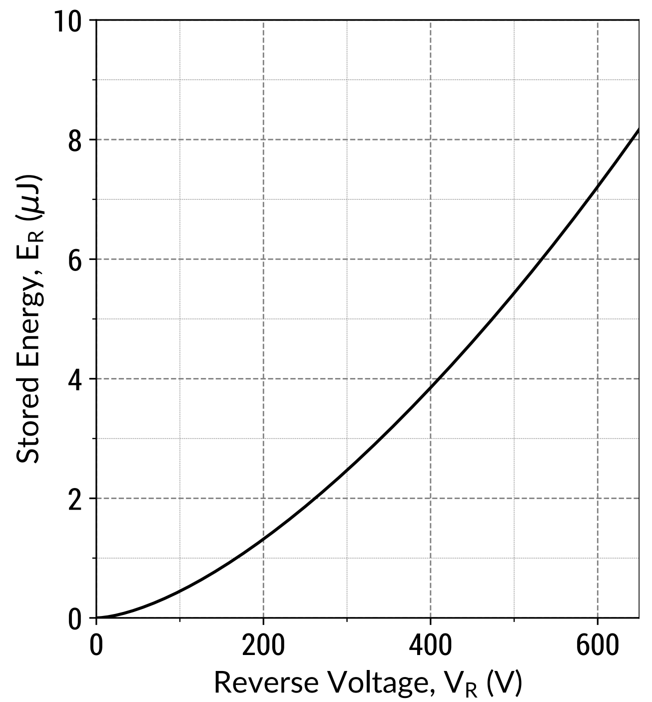
$C = f(V_R)$; f = 1MHz

Figure 7: Typical Capacitive Charge vs Reverse Voltage Characteristics



$Q_C = f(V_R)$; f = 1MHz

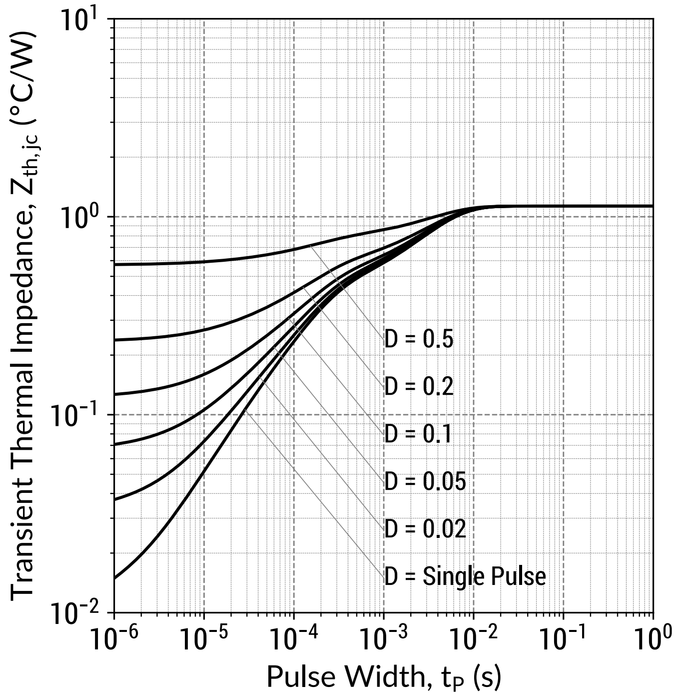
Figure 8: Typical Capacitive Energy vs Reverse Voltage Characteristics



$E_C = f(V_R)$; f = 1MHz

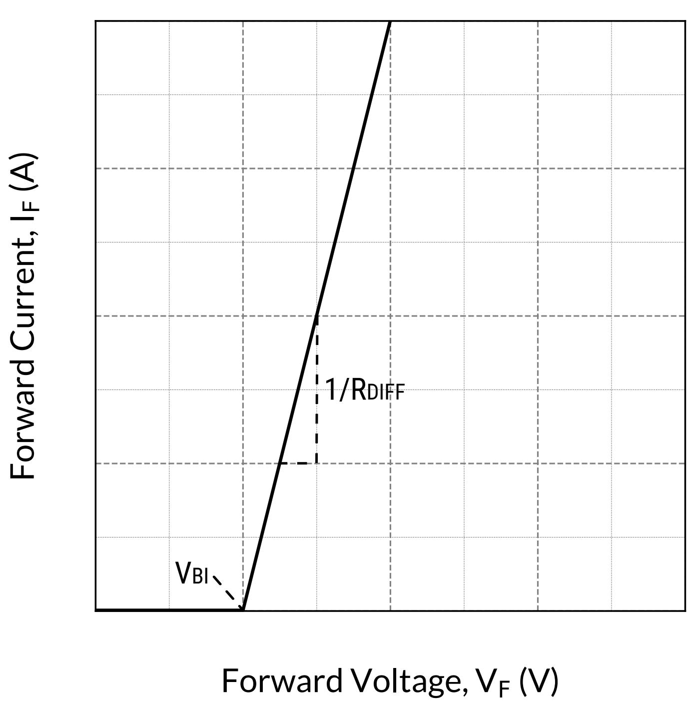
GeneSiC SEMICONDUCTOR

Figure 9: Transient Thermal Impedance



$Z_{th,jc} = f(t_P, D)$; $D = t_P/T$

Figure 10: Forward Curve Model



$I_F = f(V_F, T_j)$

Forward Curve Model Equation:

$I_F = (V_F - V_{BI})/R_{DIFF}$ (A)

Built-In Voltage (V_{BI}):

$V_{BI}(T_j) = m \times T_j + n$ (V)

m = -0.00124 (V/°C)

n = 0.72 (V)

Differential Resistance (R_{DIFF}):

$R_{DIFF}(T_j) = a \times T_j^2 + b \times T_j + c$ (Ω)

a = 1.6e-06 (Ω/°C²)

b = 0.000454 (Ω/°C)

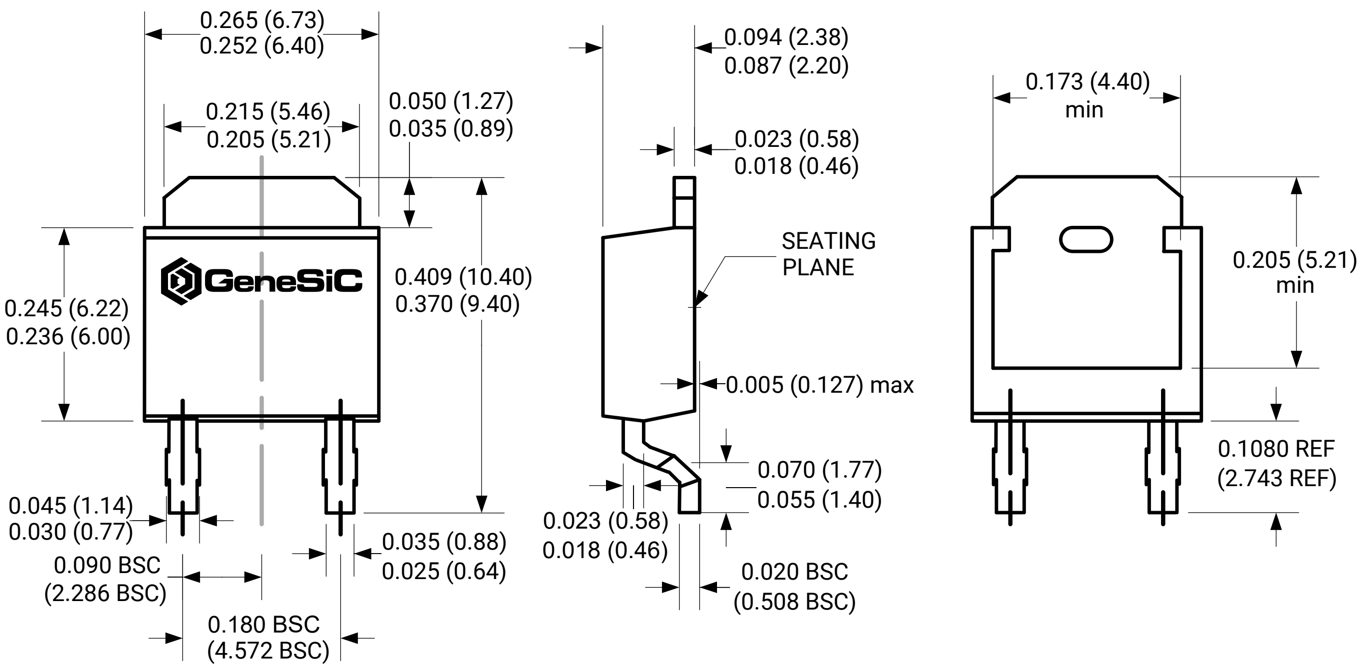
c = 0.0802 (Ω)

Forward Power Loss Equation:

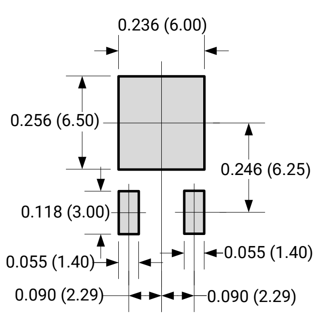
$P_{LOSS} = V_{BI}(T_j) \times I_{AVG} + R_{DIFF}(T_j) \times I_{RMS}^2$

Package Dimensions

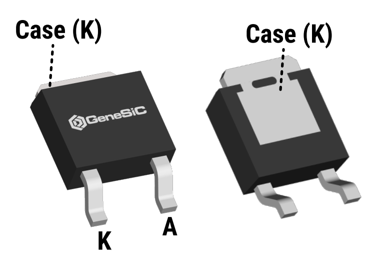
TO-252-2 Package Outline



Recommended Solder Pad Layout



Package View



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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Related Links

- SPICE Models: https://www.genesicsemi.com/sic-schottky-mps/GE06MPS06E/GE06MPS06E_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-schottky-mps/GE06MPS06E/GE06MPS06E_PLECS.zip
- CAD Models: https://www.genesicsemi.com/sic-schottky-mps/GE06MPS06E/GE06MPS06E_3D.zip
- Evaluation Boards: https://www.genesicsemi.com/technical-support
- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

Revision History

Date	Revision	Comments	Supersedes
Jul. 27, 2020	Rev 1	Initial Release	

www.genesicsemi.com/sic-schottky-mps/

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