Littelfuse®

Expertise Applied | Answers Delivered

LF2304N

Half-Bridge Gate Driver

Features

- Drives two N-channel MOSFETs or IGBTs in a half bridge configuration
- Floating high-side driver in bootstrap operation to 600V
- 290mA source/600mA sink output current capability
- Outputs tolerant to negative transients
- Internal logic and deadtime (100ns) to protect MOSFETs
- Logic input (HIN and LIN) 3.3V capability
- Schmitt triggered logic inputs with internal pull down
- Under Voltage Lockout (UVLO) for high and low side drivers

Description

The LF2304N is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. The high voltage technology enables the LF2304N's high side to switch to 600V in a bootstrap operation.

LF2304N logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. An internal deadtime of 100ns protects high-voltage MOSFETs from shoot-through.

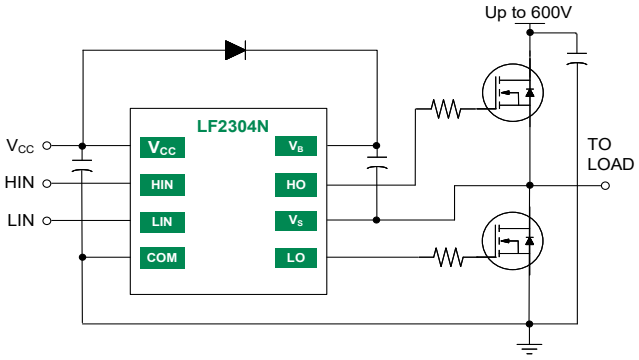
LF2304N is offered in SOIC(N)-8 package and operates over the extended temperature range of -40°C to +125°C.

Applications

- Motor Controls
- AC-DC Inverters
- DC-DC Converters
- Class D Power Amplifiers

SOIC(N)-8

Typical Application



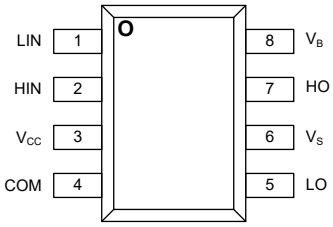
Ordering Information

Year Year Week Week

Part#	Package	Pack /Qty	Mark
LF2304NTR	SOIC(N)-8	Tape & Reel / 2500	YYWW LF2304N LOT ID

1 Specifications

1.1 Pin Diagrams



Top View: SOIC(N)-8

LF2304N

1.2 Pin Descriptions

Pin #	Pin Name	Pin Type	Pin Description
1	LIN	Input	Logic input for low side gate driver output, in phase with LO
2	HIN	Input	Logic input for high-side gate driver output, in phase with HO
3	V_{CC}	Power	Low-side and logic fixed supply
4	COM	Power	Low-side and logic return
5	LO	Output	Low-side gate drive output
6	V_S	Power	High-side floating supply return
7	HO	Output	High-side gate drive output
8	V_B	Power	High-side floating supply

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
High side floating supply voltage	V_B	-0.3	+624	V
High side floating supply offset voltage	V_S	V_B-24	V_B+0.3	V
High side floating output voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Offset supply voltage transient	dV_S/dt	--	50	V/ns
Low side fixed supply voltage	V_{CC}	-0.3	+24	V
Low side output voltage	V_{LO}	-0.3	V_{CC}+0.3	V
Logic input voltage (HIN and LIN)	V_{IN}	-0.3	V_{CC}+0.3	V
Package power dissipation	P_D	--	0.625	W
Junction Operating Temperature	T_J	--	+150	°C
Storage Temperature	T_{STG}	-55	+150	° C

Unless otherwise specified all voltages are referenced to COM . All electrical ratings are at T_A= 25 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.4 Thermal Characteristics

Parameter	Symbol	Rating	Unit
Junction to ambient	$\emptyset_{JA}$	200	° C/W

When mounted on a standard JEDEC 2-layer FR-4 board - JESD51-3

1.5 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
High side floating supply absolute voltage	V_B	V_S + 10	V_S + 20	V
High side floating supply offset voltage	V_S	***NOTE 1***	600	V
High side floating output voltage	V_{HO}	V_S	V_B	V
Low side and logic fixed supply voltage	V_{CC}	10	20	V
Low side output voltage	V_{LO}	0	V_{CC}	V
Logic input voltage	V_{IN}	0	5	V
Ambient temperature	T_A	-40	125	°C

Unless otherwise specified all voltages are referenced to COM

NOTE1 *High-side driver remains operational for V_S transients down to -5V*

1.6 DC Electrical Characteristics

V_{CC} =V_{BS}=15V, T_A = 25 °C and V_{COM} = 0V , unless otherwise specified

The V_{IN} and I_{IN} parameters are applicable to both logic input pins: HIN and LIN . The V_O and I_O parameters are applicable to the respective output pins: HO and LO and are referenced to COM

Parameter	Symbol	Conditions	MIn	Typ	Max	Unit
Logic "1" input voltage	V_{IH}	V_{CC} = 10 V to 20 V **Note2**	2.3	--	--	V
Logic "0" input voltage	V_{IL}		--	--	0.7	
Logic input voltage hysteresis	$V_{IN(HYS)}$		--	0.3	--	
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O = 2mA	--	0.05	0.2	
Low level output voltage, V_O	V_{OL}	I_O = 2mA	--	0.02	0.1	
Offset supply leakage current	I_{LK}	V_B = V_S = 600V	--	--	50	µA
Quiescent V_{BS} supply current	I_{BSQ}	V_{IN} = 0V or 5V	20	60	150	
Quiescent V_{CC} supply current	I_{CCQ}	V_{IN} = 0V or 5V	50	260	400	µA
Logic "1" input bias current	I_{IN+}	V_{IN} = 5V	--	5	40	µA
Logic "0" input bias current	I_{IN-}	V_{IN} = 0V	--	1.0	5.0	
V_{BS} UVLO off positive going threshold	V_{BSUV+}	--	7.7	8.7	9.7	V
V_{BS} UVLO enable negative going threshold	V_{BSUV-}	--	7.0	8.0	9.0	
V_{BS} UVLO hysteresis	$V_{BSUV(HYS)}$	--	--	0.7	--	
V_{CC} UVLO off positive going threshold	V_{CCUV+}	--	7.7	8.7	9.7	
V_{CC} UVLO enable negative going threshold	V_{CCUV-}	--	7.0	8.0	9.0	
V_{CC}UVLO hysteresis	$V_{CCUV(HYS)}$	--	--	0.7	--	
Output high short circuit pulsed current	I_{O+}	V_O = 0V, t ≤ 10 µs	60	290	--	mA
Output low short circuit pulsed current	I_{O-}	V_O = 15V, t ≤ 10 µs	130	600	--	

NOTE2 *For optimal operation, it is highly recommended the input pulse (to HIN and LIN) should have a minimum amplitude of 2.5V with a minimum pulse width of 200ns.*

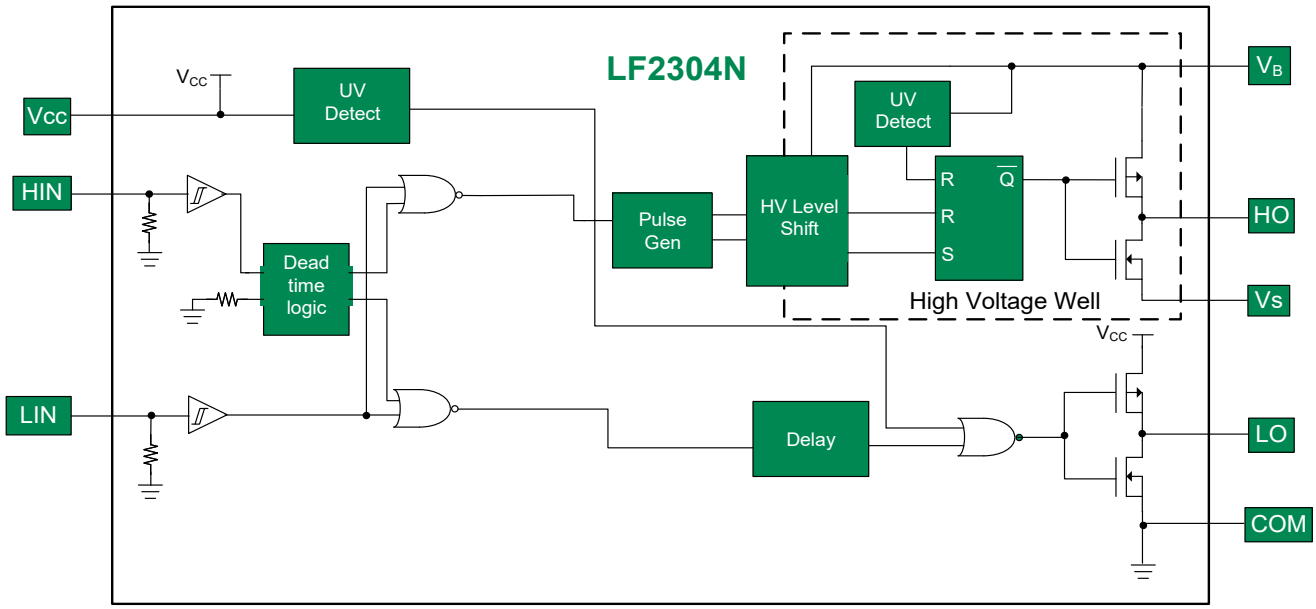
1.7 AC Electrical Characteristics

V_{CC}= V_{BS}= 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on propagation delay	t_{ON}	V_S = 0V	--	95	210	ns
Turn-off propagation delay	t_{OFF}	V_S = 0 V or 600V	--	100	210	
Propagation delay matching, HO & LO turn on/off	t_{DM}	--	--	--	50	
Turn-on rise time	t_r	--	--	70	120	
Turn-off fall time	t_f	--	--	35	60	
Deadtime: $t_{DT\ LO\text{-}HO}$ & $t_{DT\ HO\text{-}LO}$	t_{DT}	--	80	100	190	
Deadtime Matching	$t_{DT\ MT}$	--	--	--	50	

2 Functional Description

2.1 Functional Block Diagram



2.2 Timing Waveforms

Figure 1. Input / Output Logic Diagram

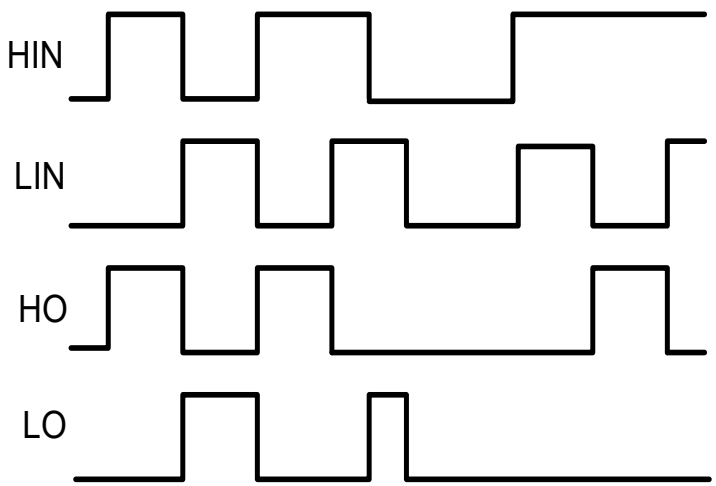
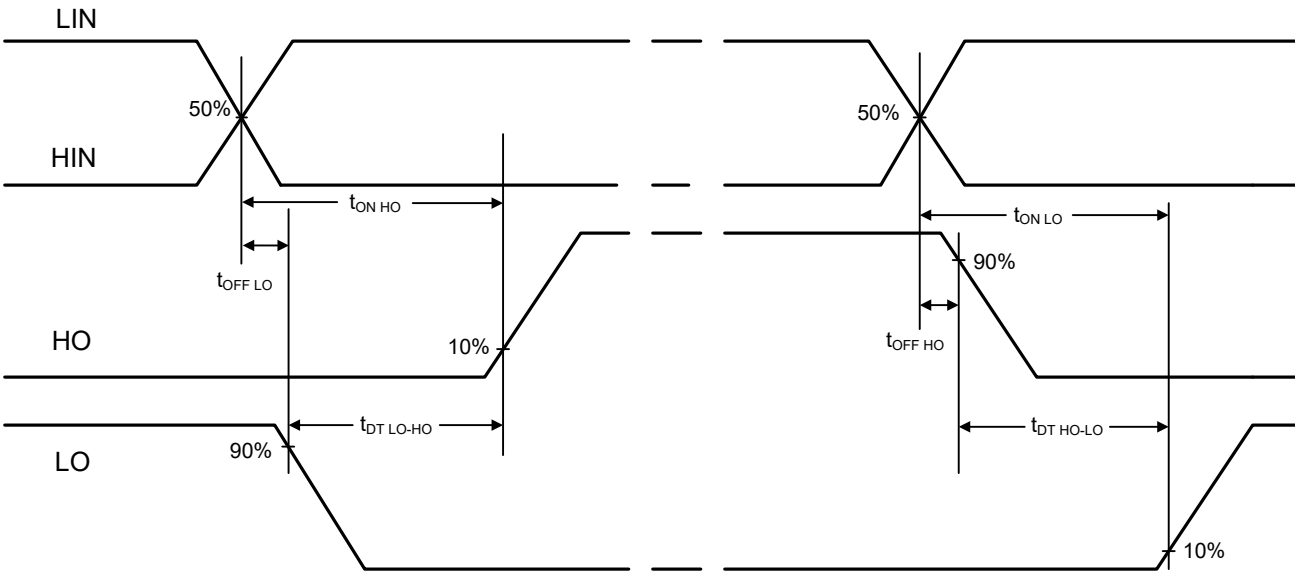


Figure 2. Input-to-Output Delay Timing Diagram



Deadtime: $t_{DT\ LO-HO} = t_{ON\ HO} - t_{OFF\ LO}$

$t_{DT\ HO-LO} = t_{ON\ LO} - t_{OFF\ HO}$

Delay matching

$t_{DM\ OFF} = |t_{OFF\ LO} - t_{OFF\ HO}|$

$t_{DM\ ON} = |t_{ON\ LO} - t_{ON\ HO}|$

Deadtime Matching : $t_{DT\ MT} = |t_{DT\ LO-HO} - t_{DT\ HO-LO}|$

2.3 LF2304N : 3-phase motor drive application

The LF2304N, half-bridge gate driver is used to optimally and efficiently drive the gate of MOSFETs or IGBTs. Below (figure 3) is an example application using the LF2304N with MOSFETs to make three halfbridge circuits used to drive a three phase motor. Typical 3 phase motor applications are AC Induction motors, PMSMs, and BLDC motors; the LF2304N also is typically used for stepper motor applications. LF2304N can also be used in power supplies. In this discussion, the important parameters needed to design in the LF2304N are discussed; main sections are bootstrap resistor, diode, and capacitor selection, gate driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

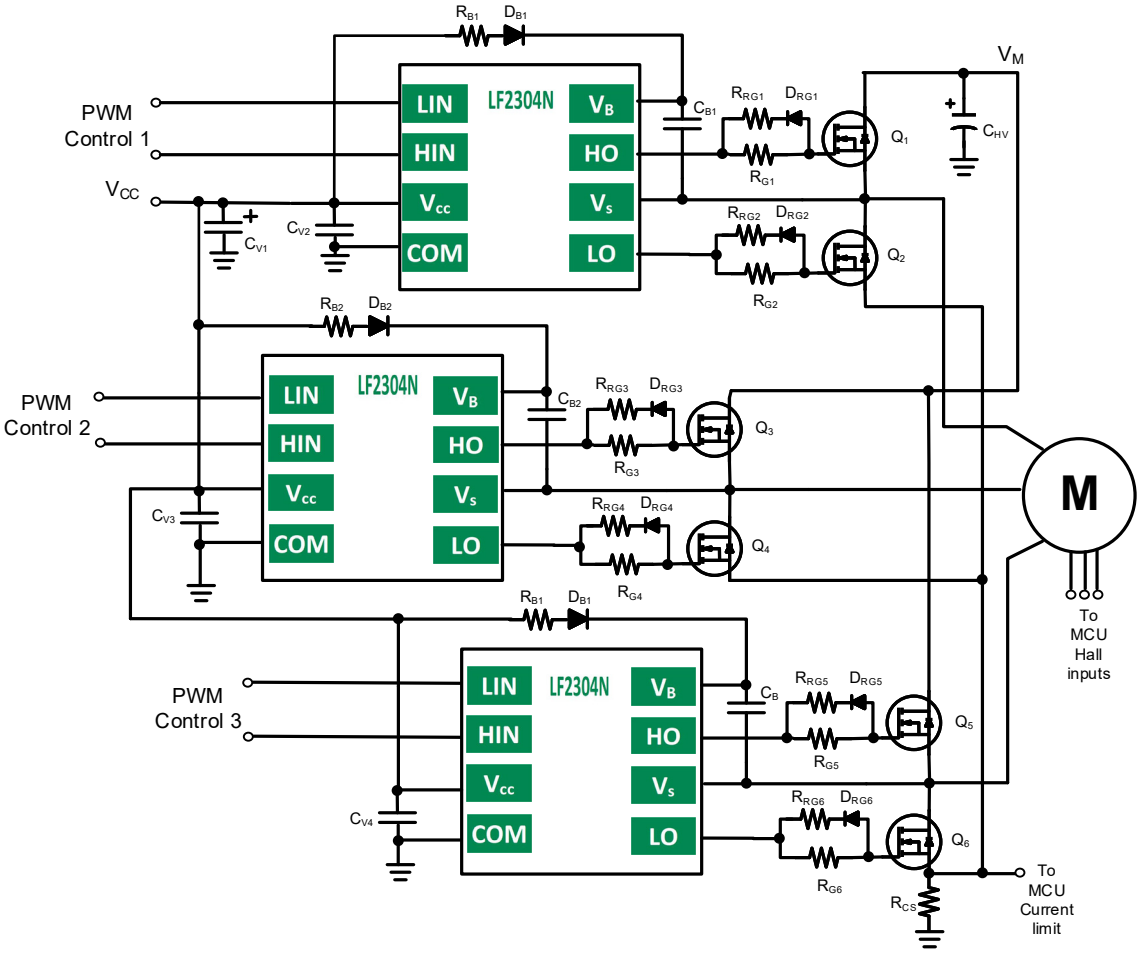


Figure 3. Three phase motor drive application example using the LF2304N

3 Application Information

3.1 Bootstrap resistor selection

Considering figure 3, when the low side MOSFET (Q2, Q4, or Q6) turns on, V_S pulls to GND and the bootstrap capacitor (CB1, CB2, and CB3) is charged. When the high side MOSFET (Q1, Q3, and Q5) is turned on, V_S swings above V_{CC} and the charge on the bootstrap capacitor (CB) provides current to drive the IC high side gate driver. The first charge of CB from V_{CC} through the bootstrap resistor (RB1, RB2, and RB3) and bootstrap diode (DB1, DB2, and DB3) occurs when power is first applied and low side turns on the first time. At this time the charge current is the largest as typically CB is not discharged fully at each cycle during normal operation

A bootstrap resistor (RBS) is included in the bootstrap circuit to limit the inrush current that charges CB when V_S pulls below V_{CC}; this inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spike on V_S and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of RBS and CBS as well as V_{CC} level. The aim in resistor selection for the application is to slow down the inrush current but have limited effect on the RC time constant of charging CBS.

Typically, values for RBS are 3Ω to 10Ω, enough to dampen the the inrush current but have little effect on the V_{BS} turn on. Below are some scopeshots illustrating the effect of different RBS values.

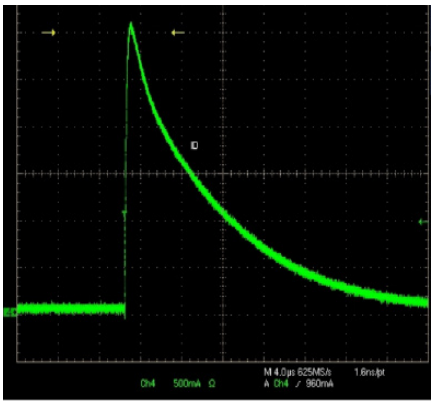


Figure 4. Bootstrap inrush current with RBS=3Ω, CBS=2.2µF

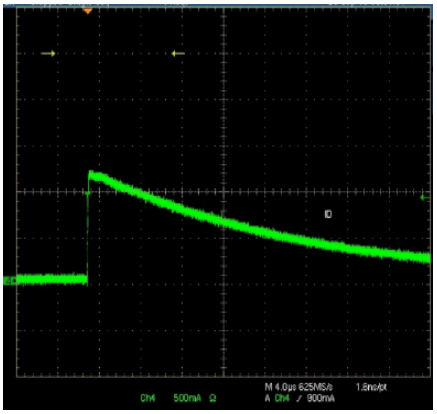


Figure 5. Bootstrap inrush current with RBS=10Ω, CBS=2.2µF

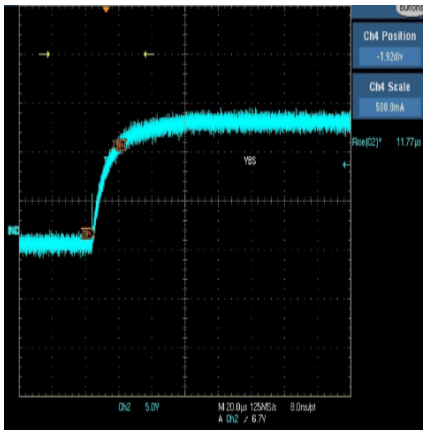


Figure 6. VBS rise time (11.8µs) with CBS=2.2µF and RBS=3Ω resister

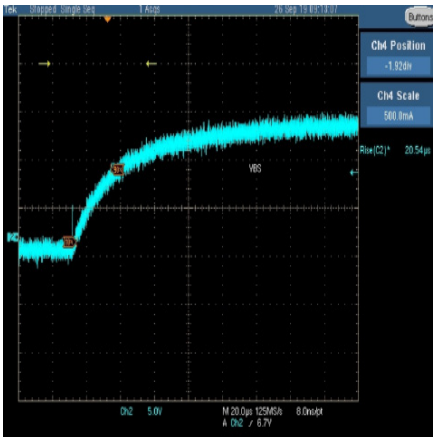


Figure 7. VBS rise time (20.5µs) with CBS=2.2µF and RBS=10Ω resister

3.2 Bootstrap capacitor selection

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop (ΔV_{BS}) that can be guaranteed when the high side device is turned on. In other words, the minimum gate-source voltage (V_{GS}min) must be greater than the UVLO of the high side circuit, specifically V_{BSUV-} level. Therefore, if V_{GS}min is the minimum gate-source voltage such that:

$V_{GS}min > V_{BSUV-}$

Then:

$\Delta V_{BS} = V_{CC} - V_F - V_{GS}min - V_X$

Where

- V_{CC} is the supply voltage to the LF2103N
- VF is the voltage drop across the bootstrap diode (DBS)
- V_X is the voltage drop across the MOSFET

V_X is calculated as the current seen across low side MOSFET multiplied by its R_{DSON} and is simply V_{CE-ON} at the specify output current if an IGBT were used instead.

In addition to the voltage drops across these components, other factors that cause VBS to drop are leakages, charge required to turn on the power devices, and duration of the high-side on time. The total charge (QT) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [ILK\_N] * THON$

Where

Q_G = gate charge of power device
Q_{LS} = level shift charge required per cycle
THON = high-side on time
ILK_N = sum of all leakages that include:

- I_{GSS}/I_{GES}: Gate-source leakage of the power device
- I_{LK_DB}: Bootstrap diode leakage
- I_{LK_IC}: Offset supply leakage of HVIC
- I_{QBS}: Quiescent current for high side supply

$CBmin \geq QT / \Delta VBS$

Q_{LS} is not listed in the datasheet; depending on the process technology, it could range anywhere from 3-20nC for 500V to 1200V process respectively. Assuming a value of 10nC for technology should be sufficient with added margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

Example using MOSFET

The follow example uses a power MOSFET as the switching device with the following and desired parameters:

- Power device = DMNH6021SK3Q
- HVIC gate driver = LF2304N
- V_{CC} = 12V
- Q_G = 20nC
- I_{GSS} = 100nA
- THON = 10µs
- R_{DSON} = 25mΩ max, 125°C
- I_{OUT} = 5A
- I_{QBS} = 150µA
- I_{LK_IC} = 50µA
- Q_{LS} = 10nC
- V_F = 1.0V
- I_{LK_DB} = 100µA
- V_{GS}min = 10V

From equations above:

ΔV_{BS} = 12V- 1.0V-10V-(0.625V) = 0.375V
$Q_T = Q_G + Q_{LS} + [ILK\_N]*THON$; where ILK_N * THON = 3nC

Thus Q_T = 20nC + 10nC +3nC = 33nC

Therefore CBmin = 33nC / 0.375V= 88nF

The bootstrap capacitor calculated in the above problem is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used, minimally. Utilizing values lower than this could result in over charging of the bootstrap capacitor especially during $-V_S$ transients. Typically for motor driver applications CBS = 1µF to 10µF are used, and for power supplies typically CBS = 0.1µF to 2.2µF. Also it is recommended to use low ESR ceramic capacitors as close to the V_B and V_S pin as possible (see PCB layout suggestions section).

3.3 Bootstrap diode selection

The chosen bootstrap diode (DBS) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the V_S node. The diode's current rating is simply the product of total charge (QT) required by the HVIC and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the CBS cap. A 1A ultrafast recovery diode is typical for LF2304N applications.

3.4 Gate resistor selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and the key is performing this function quickly but with minimal noise and ringing to the overall system. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

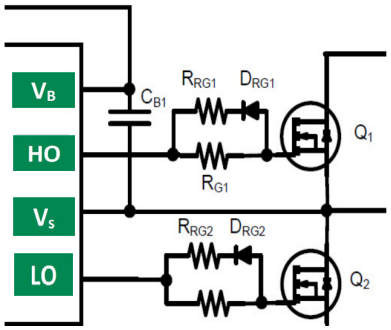


Figure 8. Gate drive high-side and low-side components for LF2304N

Considering the gate driver components for LF2304N in fig 8 , with the careful selection of RG1 and RRG1, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET. For turn on, all current will go from the IC through RG1 and charge the MOSFET gate capacitance, hence increasing or decreasing RG1 will increase or decrease rise time in the application. With the addition of DRG1 , the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitance, through RRG1 and DRG1 to the driver in the IC to V_S for high side and COM for low side. So increasing or decreasing RRG1 will increase or decrease the fall time. Sometimes finer control is not needed and only RG1 and RG2 is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. Generally, for motors, the switching speed is slower, the deadtime is longer, and the application has more inherent noise, hence higher values are recommended, for example RG = 10Ω - 100Ω. For power supplies, the switching speed is faster, deadtimes are shorter for efficiency, and so smaller values are typically used, for example RG = 3Ω - 20Ω.

To have equal switching times for high-side and low-side, it is recommended that the gate driver components for high-side and low-side are mirrored. For example RRG1=RRG2, DRG1=DGR2, and RG2=RG2.

3.5 Decoupling capacitors

For optimal operation, V_{CC} decoupling is crucial for all gate driver ICs. With poor decoupling, largerr V_{CC} transients will occur at the IC when switching, and for greater and longer V_{CC} drop the IC can go into UVLO.

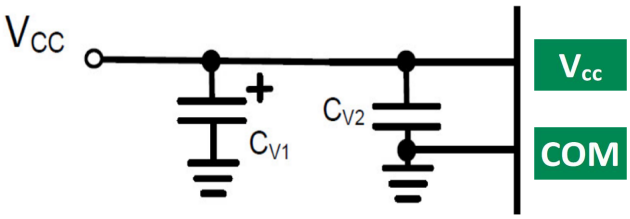


Figure 9. Suggested VCC decoupling

As shown in fig 9, two decoupling capacitors are recommended CV1 and CV2. CV1 can be a larger electrolytic, for example 47mF, 50V, used to dampen low frequency drains on supply; CV1 does not need to be right next to the IC. But CV2 is used to decouple faster edge changes to $_{VCC}$, and should be a low ESR ceramic capacitor placed close to the V_{CC} pin. This component provides stability when VCC is quickly pulled down with load from the IC; typical values are 0.1mF to 1mF. For applications with multiple gate driver ICs (for example BLDC motor drive with 3 x gate drivers as shown in figure 3), one larger electrolytic (CV1) can be used and the three ceramic caps (CV2, CV3, CV4) should be used close to the VCC pin (see Layout section also).

3.6 Input resistors

The LF2304N PWM inputs, HIN and LIN, are very high impedance inputs with a pull down resistor to COM for both the HIN and LIN (figure 10). The pull down resistor on HIN and LIN has a value of approximately 1.0MΩ.

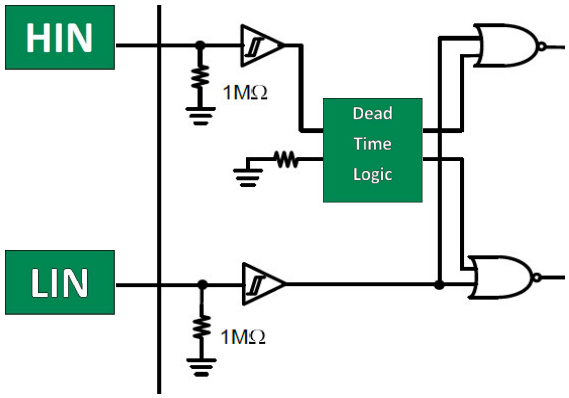


Figure 10. Input logic for LF2304N

3.7 IC drive current and MOSFET/IGBT gate charge

Gate driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the LF2304N the drive current is source I_{O+}=290mA typical, and sink I_{O-}=600mA typical.

For a given MOSFET/IGBT, with the known drive current of the LF2304N, you can estimate how long it will take to turn on/off the MOSFET/IGBT with the equation:

t = Qg/ I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current.

For example with the Diodes' DGTD65T15H2TF, 650V IGBT, Qg=61nC; and with the LF2304N I_{O+}=290 nA and I_{O-}=600mA, the tr = 210ns and tf = 102ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also an addition of a gate resistor will increase the tr and tf.

3.8 Unexpected shoot-through with dV_{DS}/dt

Unwanted MOSFET turn-on, caused by C_{GD} x dV_{DS}/dt (see fig. 11) is often the cause of unexplained shoot through in the halfbridge circuit. Depending on the ratio of the C_{GS}/ C_{GD} , when the dV_{DS}/dt across low side MOSFET (Q2) occurs (i.e when high side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot through. In effect a gate bouncing occurs causing a ringing on the V_S line and the power ground.

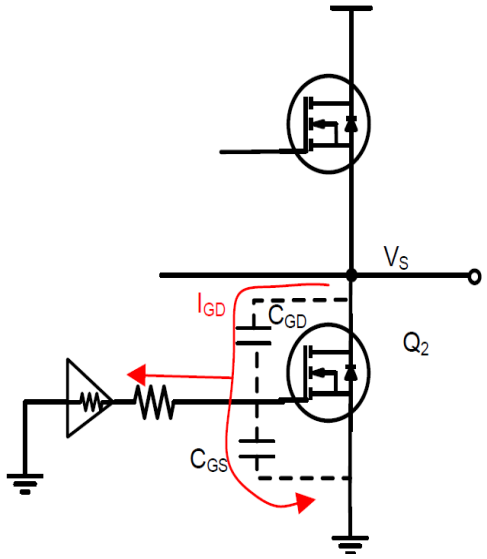


Figure 11. Unexpected shoot through with dV_{DS}/dt

Considering fig. 11

$I_{GD} = C_{GD}$ x dV_{DS}/dt

I_{GD} will flow towards the resistive load (and small inductive due to parasitics) of the gate driver and the C_{GS} of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of C_{GS}/ C_{GD}); having a Ciss/Cres as large as possible will minimize this phenomenon. Also an external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase C_{GS}/ C_{GD}.

3.9 Minimum pulse width recommendation

The LF2304N has RC filter on the input lines to be more resilient in noisy environments. With a rising edge at the input to the gate driver, and then after the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the halfbridge will turn on producing bus voltage at the output. This MOSFET turn on produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure the turn off occurs after this event. As a rule of thumb, this minimum pulse should be 2x deadtime for halfbridge drivers; hence for the LF2304N, the minimum pulse recommended at the logic inputs is 200ns.

During typical operation, the LF2304N will respond to an input greater than 50ns (approximate value from the RC input filter response). Hence for an input pulse greater than 50ns approximately the IC will follow the pulse as expected; and for an input pulse less than 50ns, there will be no response from the IC.

3.10 PCB layout suggestions

Layout plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 12 shows the schematic with parasitic inductances in the high current path (LP1, LP2, LP3, LP4) which would be caused by inductance in the metal of the trace. Considering fig. 12, the length of the tracks in red should be minimized, and the bootstrap capacitor (CB) and the decoupling capacitor (CD) should be placed as close to the IC as possible as well as using low ESR ceramic capacitors.

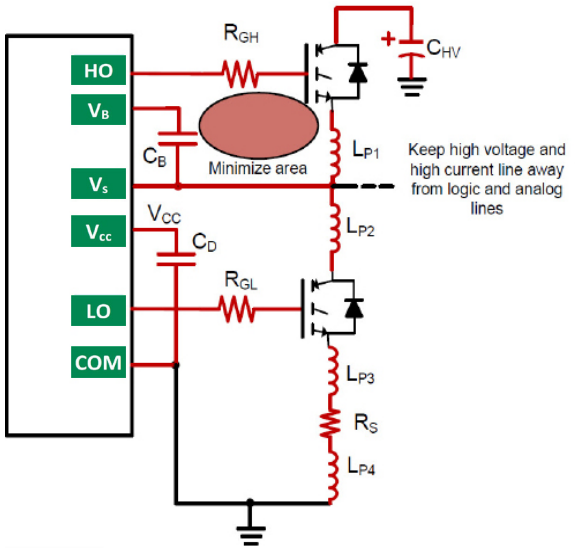


Figure 12. Layout suggestions for LF2304N in a halfbridge, lines in red should be as short as possible

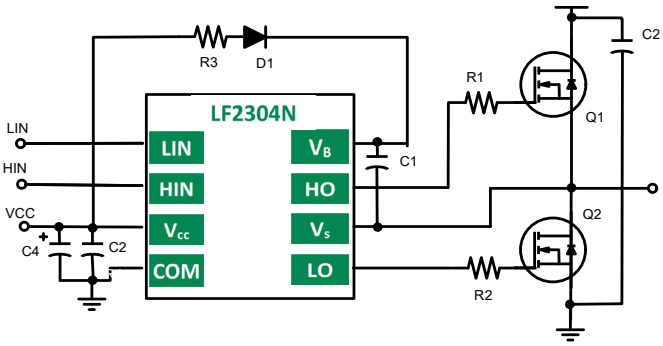


Figure 13. Schematic for layout example shown in figure 14.

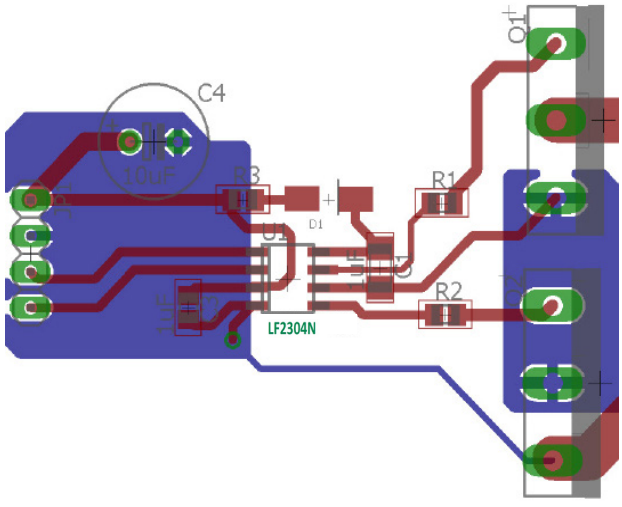


Figure 14. Example layout of the schematic shown in Figure 13.

4 Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033.**

Device	Moisture Sensitivity Level (MSL) Classification
LF2304N	MSL3

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Reflow Profile

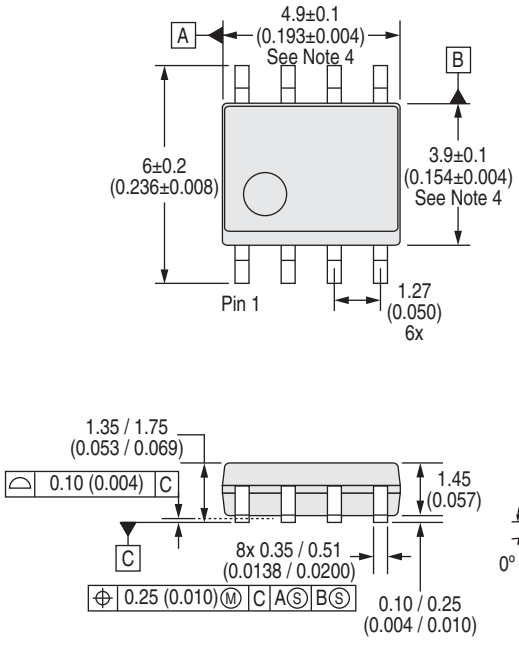
Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

Device	Classification Temperature(Tc)	Dwell Time (tp)	Max Reflow Cycles
LF2304N	260°C	30 seconds	3

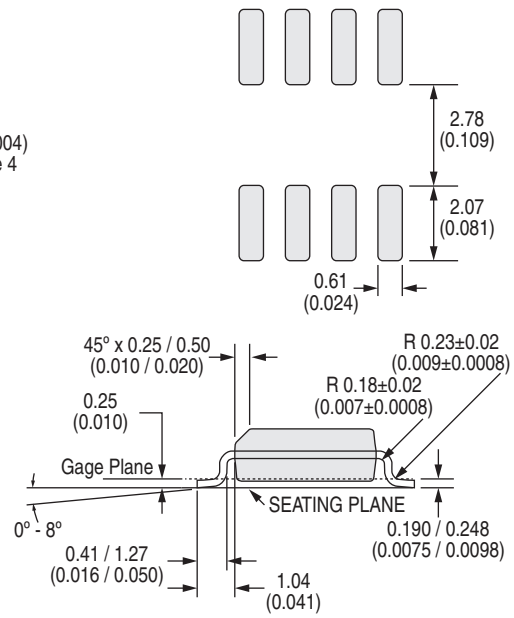
4.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

5 Package Dimensions SOIC(N)-8



Recommended PCB Land Pattern



Notes: (Unless otherwise specified)
1. Controlling dimension: millimeters.
2. All dimensions are in mm (inches).
3. Reference JEDEC registration MS-012, variation AA.
4. Not including mold flash, protrusion, or gate burrs
   0.15 (0.006) maximum per end.

Dimensions:
Minimum / Maximum

Important Notice

Specification: DS-LF2304N-R01

Printed in USA.
09 / 20 / 2021