| Title: Datasheet for ADC12J4000  Customer Contact: PCN Manager Dept: Quality  Change Type:  Assembly Site Design Wafer Bump Si  Assembly Process Data Sheet Wafer Bump Mi  Assembly Materials Part number change Wafer Bump Process Packing/Shipping/Labeling Test Site Wafer Fab Site  Packing/Shipping/Labeling Test Process Wafer Fab Materials Wafer Fab Materials Wafer Fab Materials Packing/Shipping/Labeling Test Process Wafer Fab Materials Notification Details  Description of Change:  Texas Instruments Incorporated is announcing an information only notification etc.  The product datasheet(s) is being updated as summarized below.  The following change history provides further details.  Changes from Revision B (September 2014) to Revision C  Added additional voltage difference parameters to the Absolute Maximum Ratings table.  Added Junction temperature to the Absolute Maximum Ratings table.  Added common mode voltage parameter to the Recommended Operating Conditions table. Changed CLK to SYSREF, and SYNC  Changed the f <sub>s</sub> / 4 + F <sub>N</sub> spur MAX limit from −58.7 dBFS to −60 dBFS to align with the SFDR max limit of 60 dBFS to Deleted the Differential Analog Input Connection image in The Analog Inputs section  Added note about offset adjust in Background Calibration Mode to the Offset Adjust section and I/O offset register tables  Added the Calibration Cycle Timing for Different Calibration Modes and Options table in the Timing Calibration Mode section  | erials<br>ess<br>2J4000   |  |  |  |  |
|--|---|--|--|--|--|
| Customer Contact: PCN Manager Dept: Quality Change Type:  Assembly Site Design Wafer Bump Si Assembly Process Data Sheet Wafer Bump Mi Assembly Materials Part number change Wafer Bump Process Wafer Bump Mi Mechanical Specification Test Site Wafer Fab Site Wafer Fab Site Wafer Fab Site Wafer Fab Mate Packing/Shipping/Labeling Test Process Wafer Fab Mate Wafer Fab Mate Wafer Fab Process Wafer Fab Mate Wafer F  | erials<br>ess<br>2J4000   |  |  |  |  |
| Change Type:  Assembly Site  Assembly Process  Assembly Process  Assembly Materials  Part number change  Wafer Bump Mi  Wafer Bump Mi  Assembly Materials  Part number change  Wafer Bump Process  Wafer Fab Site  Wafer Fab Site  Wafer Fab Materials  Wafer Fab Process  Notification Details  Description of Change:  Texas Instruments Incorporated is announcing an information only notification etc.  The product datasheet(s) is being updated as summarized below.  The following change history provides further details.  Texas  Instruments  ADC1:  SLAS989C JANUARY 2014 - REVISED J  Changes from Revision B (September 2014) to Revision C  Added additional voltage difference parameters to the Absolute Maximum Ratings table  Added common mode voltage parameter to the Recommended Operating Conditions table. Changed CLK to SYSREF, and ~SYNC.  Changed the f <sub>S</sub> / 4 + F <sub>NI</sub> spur MAX limit from −58.7 dBFS to −60 dBFS to align with the SFDR max limit of 60 dBFS  Deleted the Differential Analog Input Connection image in The Analog Inputs section  Added note about offset adjust in Background Calibration Mode to the Offset Adjust section and I/O offset register tables.  Added the Calibration Cycle Timing for Different Calibration Modes and Options table in the Timing Calibration Mode section   | erials<br>ess<br>2J4000   |  |  |  |  |
| Assembly Site  Design  Data Sheet  Wafer Bump Si  Assembly Process  Data Sheet  Wafer Bump Mi  Assembly Materials  Part number change  Wafer Bump Pr  Wafer Bump Pr  Wafer Fab Site  Packing/Shipping/Labeling  Test Site  Wafer Fab Site  Wafer Fab Materials  Wafer | erials ess  2J4000 ULY 2015   |  |  |  |  |
| Assembly Process  Assembly Materials  Part number change  Wafer Bump Mechanical Specification  Test Site  Packing/Shipping/Labeling  Test Process  Wafer Fab Site  Wafer Fab Materials  Wafer Fab Materials  Wafer Fab Site  Wafer Fab Materials  Wafer Fab Materials | erials ess  2J4000 ULY 2015   |  |  |  |  |
| Assembly Materials  Part number change  Mechanical Specification  Test Site  Wafer Fab Site  Wafer Fab Mate  Wafer Fab Process  Notification Details  Description of Change:  Texas Instruments Incorporated is announcing an information only notification etc.  The product datasheet(s) is being updated as summarized below.  The following change history provides further details.  Texas Instruments  ADC1:  SLASSB9C – JANUARY 2014– REVISED J  Changes from Revision B (September 2014) to Revision C  Added additional voltage difference parameters to the Absolute Maximum Ratings table  Added Junction temperature to the Absolute Maximum Ratings table  Added common mode voltage parameter to the Recommended Operating Conditions table. Changed CLK to SYSREF, and ~SYNC  Changed the f <sub>S</sub> / 4 + F <sub>IN</sub> spur MAX limit from –58.7 dBFS to –60 dBFS to align with the SFDR max limit of 60 dBFS  Deleted the Differential Analog Input Connection image in The Analog Inputs section  Added note about offset adjust in Background Calibration Mode to the Offset Adjust section and I/O offset register tables  Added the Calibration Cycle Timing for Different Calibration Modes and Options table in the Timing Calibration Mode section  | erials<br>ess<br>2J4000<br>ULY 2015   |  |  |  |  |
| Mechanical Specification   | erials<br>ess<br>2J4000<br>ULY 2015   |  |  |  |  |
| Packing/Shipping/Labeling   Test Process   Wafer Fab Mate   Wafer Fab Process   Waf    | 2J4000<br>ULY 2015  |  |  |  |  |
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| Added the Calibration Cycle Timing for Different Calibration Modes and Options table in the Timing Calibration Mode section  | 27  |  |  |  |  |
| Mode section   | 31  |  |  |  |  |
| Changed 0x004-0x005 to RESERVED in the Standard SPI-3.0 Registers summary table  | 46  |  |  |  |  |
| Changed 0x004-0x005 to RESERVED in the Standard SPI-3.0 Registers summary table  |   |  |  |  |  |
|  |   |  |  |  |  |
| The datasheet number will be changing.   |   |  |  |  |  |
| Device Family Change From: Change 7  |   |  |  |  |  |
| ADC12J4000 SLAS989B SLAS989  | )C  |  |  |  |  |
| These changes may be reviewed at the datasheet links provided. http://www.ti.com/product/ADC12J4000  |   |  |  |  |  |
| Reason for Change:   |   |  |  |  |  |
| o more accurately reflect device characteristics.  |   |  |  |  |  |
| Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / ne   | antivo)   |  |  |  |  |
| No anticipated impact. This is a specification change announcement only. There are no o the actual device.   | gative):  |  |  |  |  |
| Changes to product identification resulting from this PCN:   |   |  |  |  |  |
| None.  |   |  |  |  |  |
| WAZI IV. a   |   |  |  |  |  |

| <b>Product Affected:</b> |                 |                |                |
|--------------------------|-----------------|----------------|----------------|
| ADC12J4000NKE            | ADC12J4000NKE10 | ADC12J4000NKER | ADC12J4000NKET |

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

| Location     | E-Mail                         |
|--------------|--------------------------------|
| USA          | PCNAmericasContact@list.ti.com |
| Europe       | PCNEuropeContact@list.ti.com   |
| Asia Pacific | PCNAsiaContact@list.ti.com     |
| Japan        | PCNJapanContact@list.ti.com    |