

Mode

Bypass mode

LNA Active mode

5 GHz Low Noise Amplifier with Bypass function

■ FEATURES

- Operating frequency f = 4900 to 5925 MHz
- Operating voltage
- 2.5 to 5.5 V
- [LNA active mode]
- 16 dB typ.
- High gain
- Low noise figure 0.95 dB typ.
- High IIP3 +9 dBm typ.
- Small package size 1.6 x 1.6 x 0.397 mm³ typ.
- RoHS compliant and Halogen Free, MSL1

■ GENERAL DESCRIPTION

The NJG1175KG1 is a low noise amplifier for wireless receiver applications in the 4900 MHz to 5925 MHz. This LNA has a LNA pass-through function to select LNA active mode or bypass mode.

The NJG1175KG1 achieves High linearity, Low distortion, high gain, and low noise figure.

Integrated ESD protection device on each port achieves excellent ESD robustness.

The small and thin ESON6-G1 package is adopted.

APPLICATION

- LTE advanced in unlicensed spectrum (LTE-U/LAA)
- WLAN (IEEE 802.11 a/n/ac/ax)
- Small cell, CPE
- Access points, routers, gateways
- Wireless routers
- 5 GHz ISM radios

BLOCK DIAGRAM (ESON6-G1)



■ PIN CONFIGURATION

"H"=VCTL(H), "L"=VCTL(L)

VCTL

L

Н

■ TRUTH TABLE

PIN NO.	SYMBOL	DESCRIPTION
1	VCTL	Control signal input terminal
2	RFIN	RF input terminal
3	GND	Ground terminal
4	GND	Ground terminal
5	RFOUT	RF output terminal
6	VDD	Operating voltage supply terminal
Exposed pad	GND	Ground terminal

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PRODUCT NAME INFORMATION



ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	RoHS	HALOGEN- FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs.)
NJG1175KG1	ESON6-G1	Yes	Yes	Sn-Bi	1175	3.5	3,000

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
RF Input Power ⁽¹⁾	PIN	+15	dBm
Supply Voltage ⁽²⁾	V _{DD}	6.0	V
Control Voltage ⁽³⁾	Vctl	6.0	V
Power Dissipation ⁽⁴⁾	PD	1200	mW
Operating Temperature	Topr	-40 to +105	°C
Storage Temperature	T _{stg}	-55 to +150	°C

(1): V_{DD} = 3.3 V

(2): VDD port

(3): VCTL port

(4): Mounted on four-layer FR4 PCB with through-hole (101.5 \times 114.5 mm), T_j = 150°C

■ POWER DISSIPATION VS.AMBIENT TEMPERATURE

Please, refer to the following Power Dissipation and Ambient Temperature.

(Please note the surface mount package has a small maximum rating of Power Dissipation [P_D], a special attention should be paid in designing of thermal radiation.)

Power Dissipation - Ambient Temperature Characteristic





■ RECOMMENDED OPERATING CONDITIONS

					T _a = 25°C
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	2.5	3.3	5.5	V
Control Voltage (HIGH)	V _{CTL(H)}	1.3	3.3	5.5	V
Control Voltage (LOW)	Vctl(L)	0	0	0.3	V

■ ELECTRICAL CHARACTERISTICS 1 (DC CHARACTERISTICS)

$T_a = 25^{\circ}C$, $Z_s = Z_l = 50 \Omega$, with application circuit

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PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current 1	11			10	10	m۸
(LNA active mode)	IDD I	$RF OFF, V_{DD} = 3.3 V, V_{CTL} = 3.3 V$	-	15	10	ША
Operating Current 2				20	100	
(Bypass mode)	IDD2	RF OFF, VDD = 3.3 V, VCTL = 0 V	-	20	100	μA
Control Current	lc⊤∟	RF OFF, V _{CTL} = 3.3 V	-	25	50	μA

■ ELECTRICAL CHARACTERISTICS 2 (RF CHARACTERISTICS: LNA active mode)

 f_{RF} = 4900 to 5925 MHz, V_{DD} = 3.3 V, V_{CTL} = 3.3 V, T_a = 25°C, Z_s = Z_l = 50 Ω , with application circuit

$R_{\rm F} = 4000 \ 10000000000000000000000000000000$				ilouit		
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Small signal gain	Gain	Exclude PCB and connector losses *1	12	16	-	dB
Noise figure	NF	Exclude PCB and connector losses *2	-	0.95	1.6	dB
Input power at 1 dB gain compression point 1	P-1dB(IN)1		-14	-5	-	dBm
Input 3 rd order intercept point 1	IIP3_1	$f1 = f_{RF}, f2 = f_{RF} + 1 \text{ MHz}, P_{IN} = -30 \text{ dBm}$	-3	+9	-	dBm
RF IN return loss 1	RLi1		6	13	-	dB
RF OUT return loss 1	RLo1		6	18	-	dB
Gain settling time 1	Ts1	Bypass to LNA active mode, To be within 1 dB of the final gain	-	0.5	2	μS
Gain settling time 2	Ts2	LNA active to bypass mode, To be within 1 dB of the final insertion loss	-	1	2	μS

*1: PCB and connector losses: 0.60 dB @ 4900 MHz, 0.64 dB @ 5500 MHz, 0.69 dB @ 5925 MHz

*2: PCB and connector losses: 0.27 dB @ 4900 MHz, 0.30 dB @ 5500 MHz, 0.31 dB @ 5925 MHz

■ ELECTRICAL CHARACTERISTICS 3 (RF CHARACTERISTICS: Bypass mode)

 f_{RF} = 4900 to 5925 MHz, V_{DD} = 3.3 V, V_{CTL} = 0 V, T_a = 25°C, Z_s = Z_l = 50 Ω , with application circuit

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Insertion loss	Loss	Exclude PCB and connector losses *1	-	5.5	9	dB
Input power at 1 dB gain	$P_1 dR(IN)2$		0	10	_	dBm
compression point 2			0	+3	-	ubiii
Input 3 rd order intercept		$f1 = f_{2} + f_{2} = f_{2} + 1 \text{ MHz } P_{2} = -15 \text{ dBm}$	0	±1 1	_	dBm
point 2	IIF 3_2	11 - 1RF, 12 - 1RF + 1 Win 12, F = 10 GBm	0	714	-	ubm
RF IN return loss 2	RLi2		4	10	-	dB
RF OUT return loss 2	RLo2		4	11	-	dB

*1: PCB and connector losses: 0.60 dB @ 4900 MHz, 0.64 dB @ 5500 MHz, 0.69 dB @ 5925 MHz

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■ ELECTRICAL CHARACTERISTICS (LNA active mode)

 V_{DD} = 3.3 V, V_{CTL} = 3.3 V, T_a = 25°C, Z_s = Z_l = 50 $\Omega,$ with application circuit













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ELECTRICAL CHARACTERISTICS (LNA active mode)

 V_{DD} = 3.3 V, V_{CTL} = 3.3 V, T_a = 25°C, Z_s = Z_l = 50 $\Omega,$ with application circuit





Zout

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ELECTRICAL CHARACTERISTICS (Bypass mode)

 V_{DD} = 3.3 V, V_{CTL} = 0 V, T_a = 25°C, Z_s = Z_l = 50 $\Omega,$ with application circuit



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ELECTRICAL CHARACTERISTICS (Bypass mode)

 V_{DD} = 3.3 V, V_{CTL} = 0 V, T_a = 25°C, Z_s = Z_l = 50 Ω , with application circuit



JRC

■ ELECTRICAL CHARACTERISTICS (LNA active mode)

 V_{CTL} = 3.3 V, Z_{s} = Z_{l} = 50 $\Omega,$ with application circuit











IIP3 vs. Ambient Temperature



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ELECTRICAL CHARACTERISTICS (Bypass mode)

 V_{CTL} = 0 V, Z_{s} = Z_{l} = 50 $\Omega,$ with application circuit



IIP3 vs. Ambient Temperature



■ ELECTRICAL CHARACTERISTICS (DC)

 $Z_s = Z_l = 50 \Omega$, with application circuit





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■ APPLICATION CIRCUIT



<PARTS LIST>

Part ID	Value	Notes
L1	1.3 nH	LQP03TN_02 Series (MURATA)
C1	1000 pF	GRM03 Series (MURATA)

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■ EVALUATION BOARD · PCB LAYOUT



PCB Information Substrate: FR-4 Thickness: 0.2mm Microstrip line width: 0.4mm (Z₀=50Ω) Size: 14.0mm x 14.0mm

<PCB LAYOUT GUIDELINE>



PRECAUTIONS

• All external parts should be placed as close as possible to the IC.

• For good RF performance, all GND terminals (include the exposed pad) must be connected to PCB ground plane of substrate, and via-holes for GND should be placed near the IC.

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■ RECOMMENDED FOOTPRINT PATTERN (ESON6-G1)

PKG: 1.6 mm x 1.6 mm Pin pitch: 0.5 mm Land
Mask (Open area) *Metal mask thickness : 100μm
Resist (Open area)



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■ NOISE FIGURE MEASUREMENT BLOCK DIAGRAM



Measurement Setup

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■ PACKAGE OUTLINE



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[CAUTION]

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