

N-Channel Power MOSFET

60V, 240mA, 2.5Ω

FEATURES

- Low $R_{DS(ON)}$ to minimize conductive losses
- Logic level
- Low gate charge for fast power switching
- ESD Protected 2.5KV (HBM)
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

KEY PERFORMANCE PARAMETERS

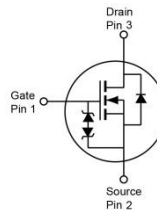
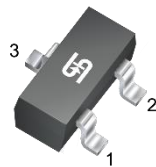
PARAMETER	VALUE	UNIT
V_{DS}	60	V
$R_{DS(on)}$ (max)	$V_{GS} = 10V$	2.5
	$V_{GS} = 4.5V$	3
Q_g	0.91	nC

APPLICATIONS

- Low Side Load Switching
- Level Shift Circuits
- General Switch Circuits



SOT-323



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_A = 25^\circ\text{C}$	240
		$T_A = 125^\circ\text{C}$	109
Pulsed Drain Current	I_{DM}	0.96	A
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	298
		$T_A = 125^\circ\text{C}$	60
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	MAXIMUM	UNIT
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	420	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. The $R_{\theta JA}$ limit presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	60	--	--	V
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	1	1.4	2.5	V
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	± 10	μA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 60V$	I_{DSS}	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 60V$ $T_J = 125^\circ\text{C}$		--	--	100	
Drain-Source On-State Resistance (Note 3)	$V_{GS} = 10V, I_D = 240mA$	$R_{DS(on)}$	--	1.9	2.5	Ω
	$V_{GS} = 4.5V, I_D = 220mA$		--	2	3	
Forward Transconductance (Note 3)	$V_{DS} = 5V, I_D = 240mA$	g_{fs}	--	0.5	--	S
Dynamic (Note 3)						
Total Gate Charge	$V_{GS} = 4.5V, V_{DS} = 30V,$ $I_D = 240mA$	Q_g	--	0.68	--	nC
Gate-Source Charge		Q_{gs}	--	0.43	--	
Gate-Drain Charge		Q_{gd}	--	0.17	--	
Input Capacitance	$V_{GS} = 0V, V_{DS} = 30V$ $f = 1.0MHz$	C_{iss}	--	30	--	pF
Output Capacitance		C_{oss}	--	15	--	
Reverse Transfer Capacitance		C_{rss}	--	6	--	
Switching (Note 3)						
Turn-On Delay Time	$V_{GS} = 10V, V_{DS} = 30V,$ $I_D = 240mA, R_G = 6\Omega$	$t_{d(on)}$	--	2.72	--	ns
Turn-On Rise Time		t_r	--	2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	7.98	--	
Turn-Off Fall Time		t_f	--	9.5	--	
Source-Drain Diode						
Forward Voltage (Note 2)	$V_{GS} = 0V, I_S = 240mA$	V_{SD}	--	--	1.2	V
Reverse Recovery Time	$I_S = 240mA,$ $di/dt = 100A/\mu s$	t_{rr}	--	10	--	ns
Reverse Recovery Charge		Q_{rr}	--	3.2	--	nC

Notes:

1. Silicon limited current only.
2. Pulse test: Pulse Width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Switching time is essentially independent of operating temperature.

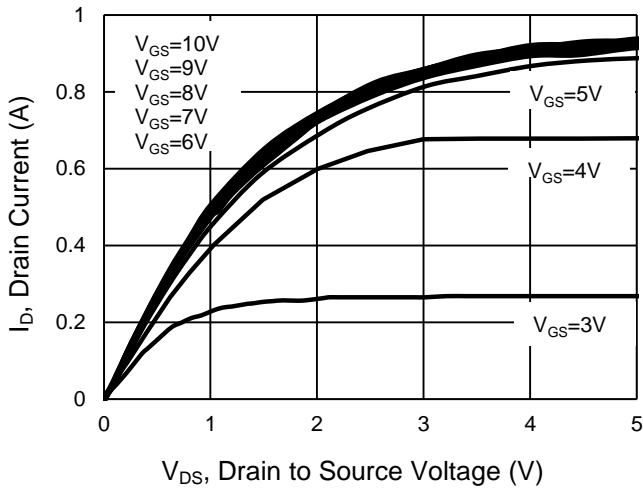
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM2N7002AKCU RFG	SOT-323	3,000pcs / 7" Reel

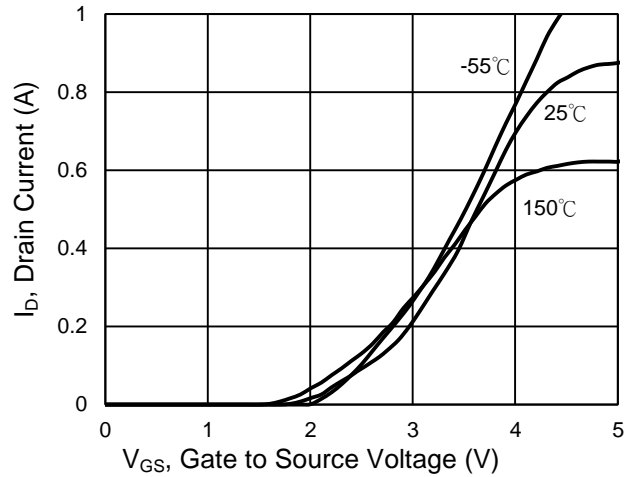
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

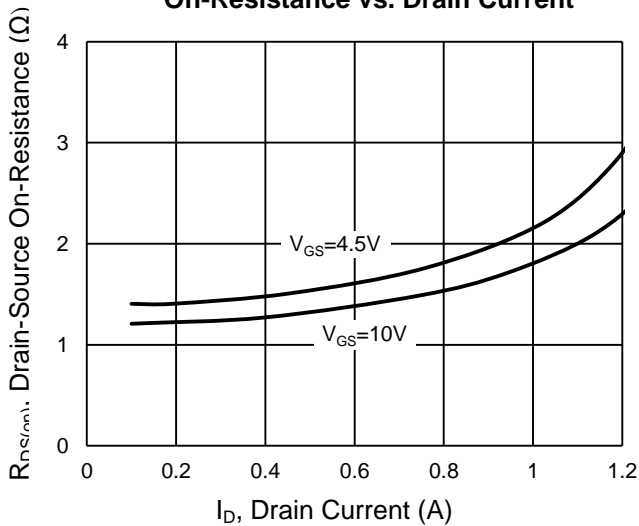
Output Characteristics



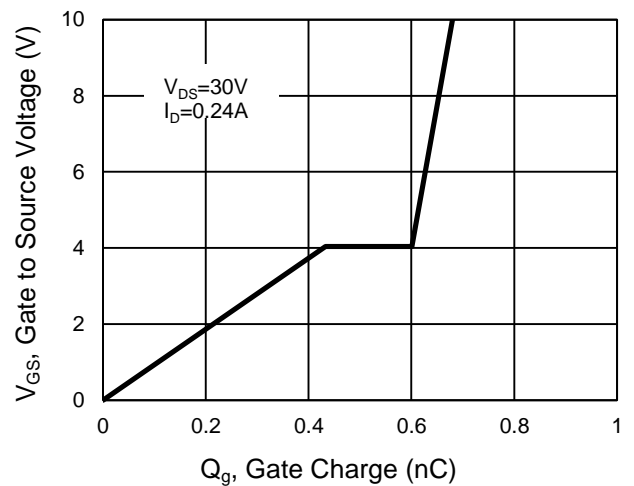
Transfer Characteristics



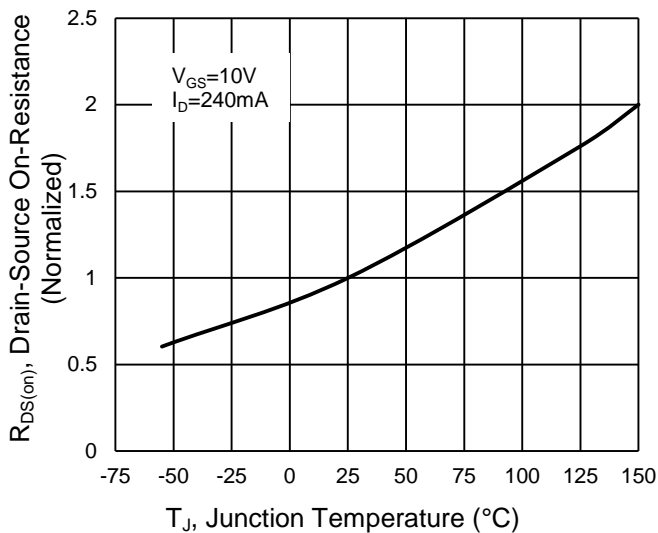
On-Resistance vs. Drain Current



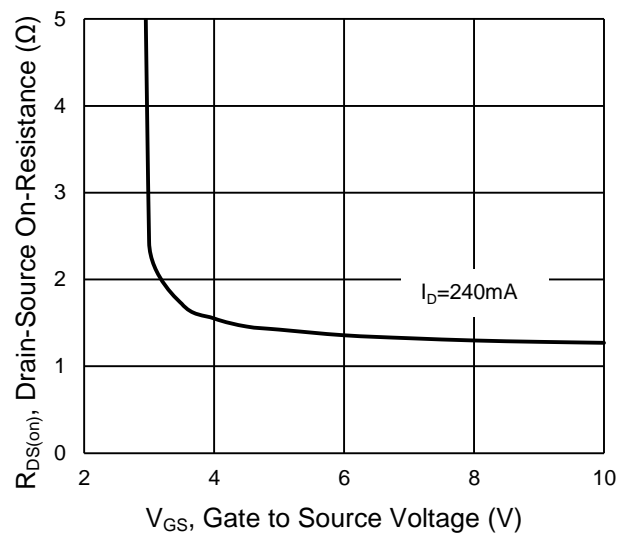
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



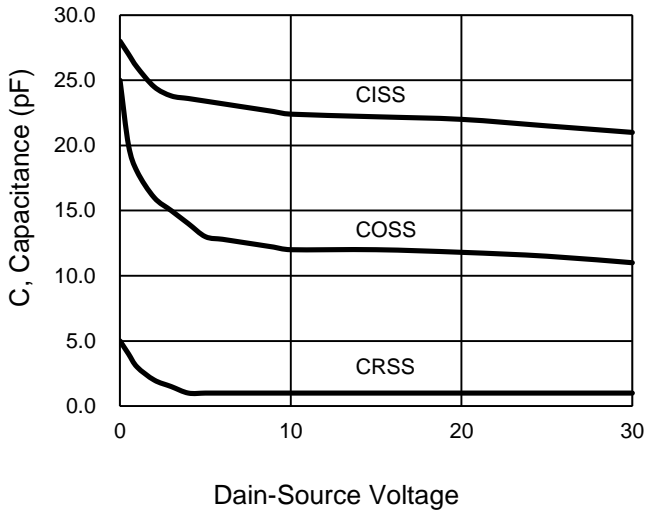
On-Resistance vs. Gate-Source Voltage



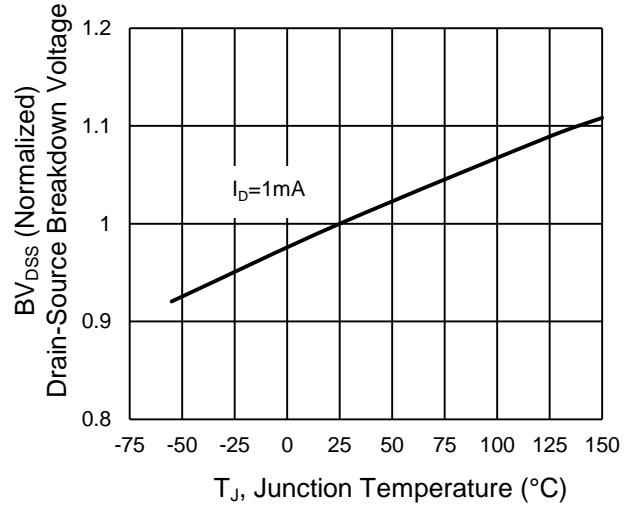
CHARACTERISTICS CURVES

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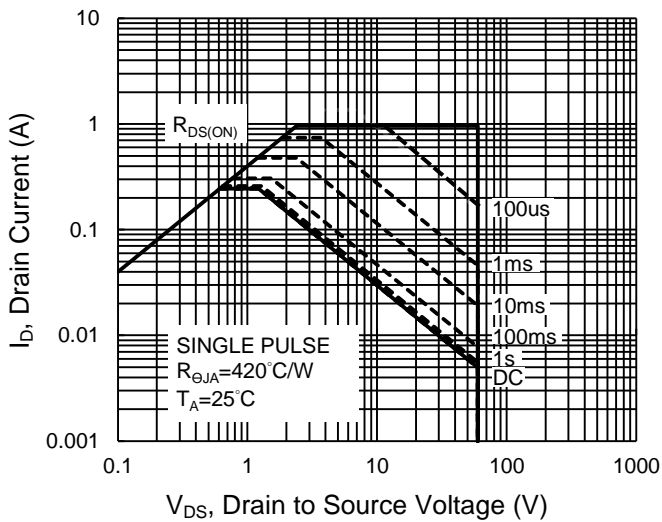
Capacitance vs. Dr



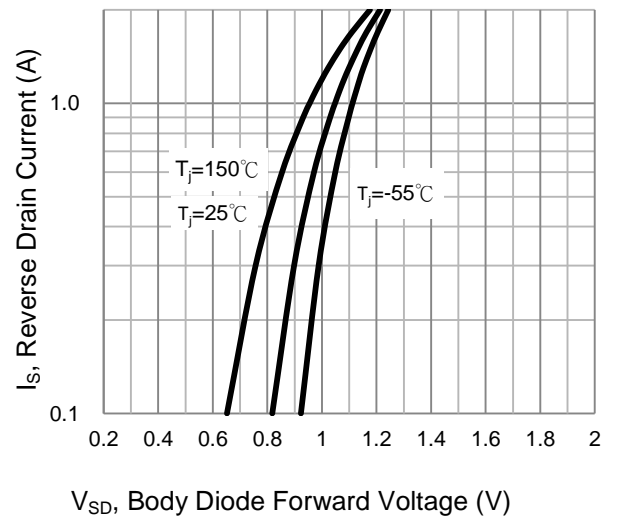
BV_{DSS} vs. Junction Temperature



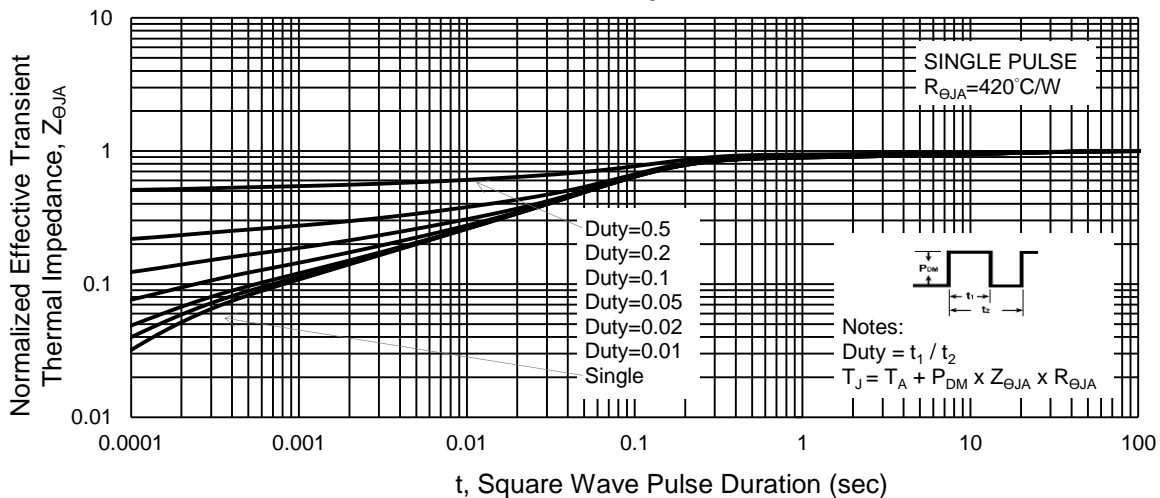
Maximum Safe Operating Area, Junction-to-Ambient



Source-Drain Diode Forward Current vs. Voltage

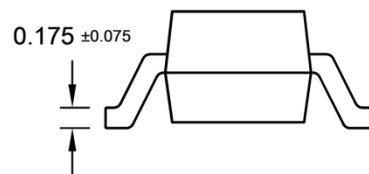
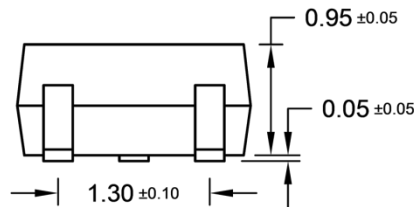
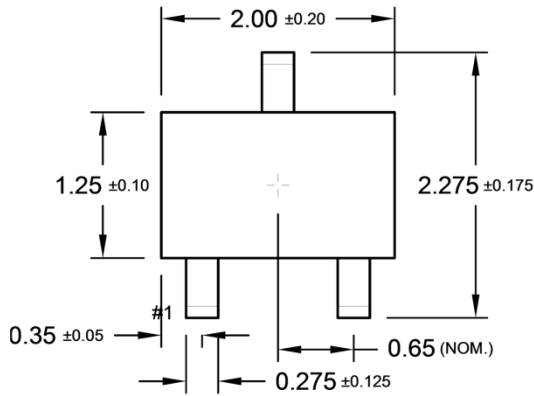


Normalized Thermal Transient Impedance, Junction-to-Ambient

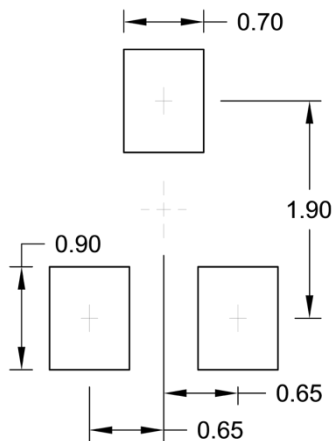


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

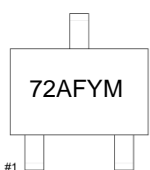
SOT-323



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- 72A** = Device code
 - F** = Site Code
 - Y** = Year Code
 - M** = Month code
- | | | | |
|---------------|---------------|---------------|---------------|
| O =Jan | P =Feb | Q =Mar | R =Apr |
| S =May | T =Jun | U =Jul | V =Aug |
| W =Sep | X =Oct | Y =Nov | Z =Dec |

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