



# MX555ANS25M0000

## Ultra-Low Jitter 25MHz LVDS XO

### ClockWorks® FUSION

### General Description

The MX555ANS25M0000 is an ultra-low phase jitter XO with LVDS output optimized for high line rate applications.

### Features

- 25MHz LVDS
- Typical phase noise:
  - 100fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

### Absolute Maximum Ratings<sup>1</sup>

Supply Voltage (VIN).....	+4.6V
Lead Temperature (soldering, 10s).....	260°C
Case Temperature.....	115°C
Storage Temperature (T <sub>g</sub> ).....	-65°C to +125°C
ESD Machine Model.....	200V
ESD Rating (HBM).....	2kV

### Operating Ratings<sup>2</sup>

Supply Voltage (VIN).....	+2.375V to +3.63V
Ambient Temperature (TA).....	-40°C to +85°C
Junction Thermal Resistance	
LGA (T <sub>jc</sub> ) Still Air.....	58°C/W

### Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 100 Ohms between Q and /Q.<sup>3</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current			90	100	mA
F0	Center Frequency			25		MHz
	Frequency Stability	Note 4			±50	ppm
∅j	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		220 100		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		100		400	ps
	Duty Cycle		45		55	%
VOH	Output High Voltage VOH max = VCM max + 1/2 VOD max	LVDS output levels	1.248	1.375	1.602	V
VOL	Output Low Voltage VOL min = VCM min - 1/2 VOD max	LVDS output levels	0.898	1.025	1.252	V
VOD	Output Differential Voltage		247	350	454	mV
VCM	Common Mode Output Voltage		1.125	1.2	1.375	V

#### Notes:

1. Exceeding the absolute maximum ratings may damage the device.
2. The device is not guaranteed to function outside its operating ratings.
3. Guaranteed after thermal equilibrium.
4. Inclusive of initial accuracy, temperature drift, aging, shock, vibration.

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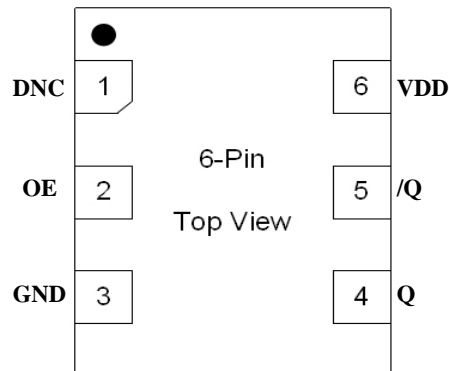
Revision 1.0  
[tcghelp@microchip.com](mailto:tcghelp@microchip.com)

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ANS25M0000	MX555A	NS0250	Tube	6-Pin 5mm x 3.2mm LGA
MX555ANS25M0000-TR	MX555A	NS0250	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

## Pin Configuration



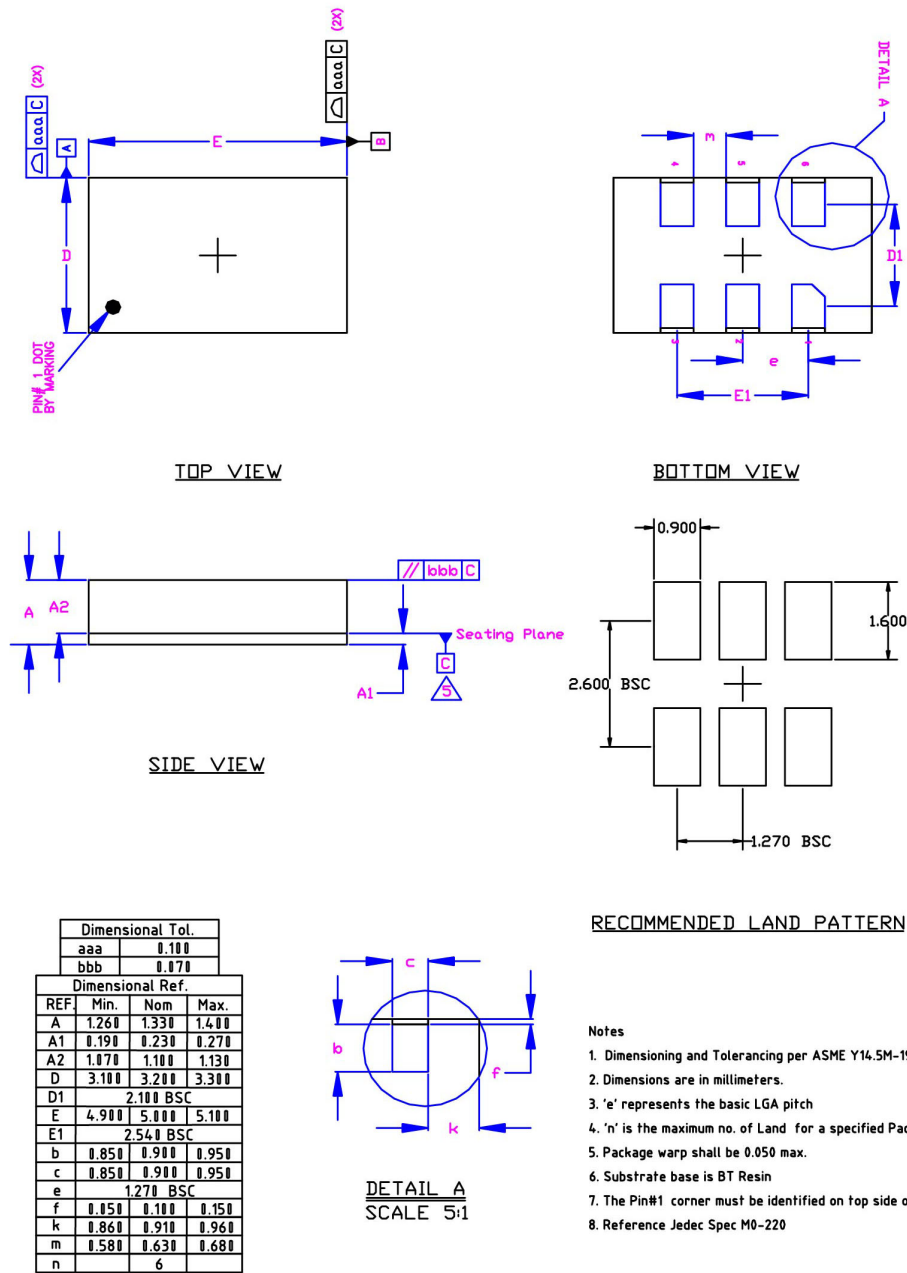
## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	DNC			Make no connection, leave floating.
2	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up (Internal)
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVDS	Clock Output Frequency = 25MHz
6	VDD	PWR		Power Supply

## Environmental Specifications

Thermal Shock	MIL-STD-883, Method 1011, Condition A
Moisture Resistance	MIL-STD-883, Method 1004
Mechanical Shock	MIL-STD-883, Method 2002, Condition C
Mechanical Vibration	MIL-STD-883, Method 2007, Condition A
Resistance to Soldering Heat	J-STD-020C, Table 5-2 Pb-free devices (except 2 cycles max)
Hazardous Substance	Pb-Free / RoHS / Green Compliant
Solderability	JESD22-B102-D Method 2 (Preconditioning E)
Terminal Strength	MIL-STD-883, Method 2004, Test Condition D
Gross Leak	MIL-STD-883, Method 1014, Condition C
Fine Leak	MIL-STD-883, Method 1014, Condition A2, R1=2x10 <sup>-8</sup> atm cc/s
MSL Level	Crystal - MSL-1, Package MSL-3
Solvent Resistance	MIL-STD-202, Method 215

### Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



**RECOMMENDED LAND PATTERN**

- Notes**
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
  2. Dimensions are in millimeters.
  3. 'e' represents the basic LGA pitch
  4. 'n' is the maximum no. of Land for a specified Package.
  5. Package warp shall be 0.050 max.
  6. Substrate base is BT Resin
  7. The Pin#1 corner must be identified on top side only.
  8. Reference Jecdec Spec M0-220

**Note:**

3. Package information is correct as of the publication date. For updates and most current information, go to [www.microchip.com](http://www.microchip.com).

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