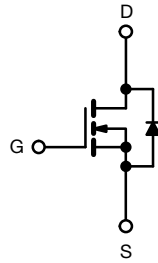
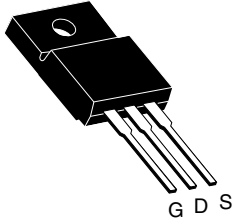


## Power MOSFET

**TO-220 FULLPAK**


N-Channel MOSFET

### FEATURES

- Low figure-of-merit  $R_{on} \times Q_g$
- 100 % avalanche tested
- Gate charge improved
- $t_{rr}/Q_{rr}$  improved
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

### Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	560	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	1
$Q_g$ max. (nC)	34	
$Q_{gs}$ (nC)	7.8	
$Q_{gd}$ (nC)	10.4	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-220 FULLPAK
Lead (Pb)-free	SiHF8N50L-E3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	500	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current <sup>a</sup>	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	$I_D$	A
Pulsed Drain Current <sup>b</sup>			$I_{DM}$	
Linear Derating Factor		0.32	$W/^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>c</sup>	$E_{AS}$	180	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	40	W
Peak Diode Recovery $dV/dt$ <sup>d</sup>	$dV/dt$	24	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$	
Soldering Recommendations (Peak temperature) <sup>e</sup>	For 10 s	300		
Mounting Torque	M3 screw	0.6	Nm	


### Notes

- Drain current limited by maximum junction temperature.
- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 10\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 6\text{ A}$ .
- $I_{SD} \leq 8\text{ A}$ ,  $dI/dt \leq 460\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

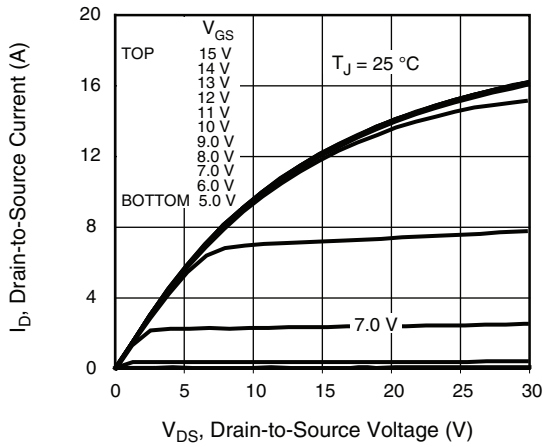
### THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	65	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	3.1	

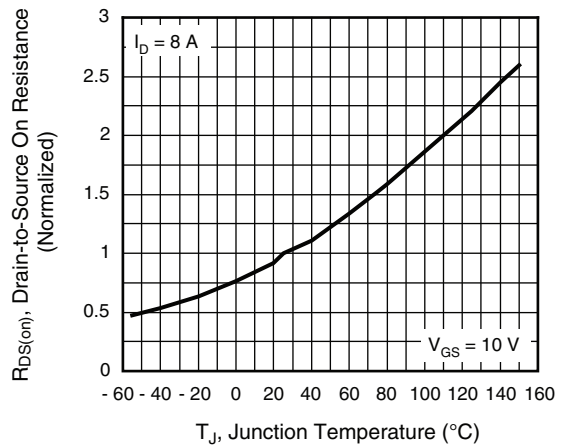


SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA	-	0.5	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	-	5.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	50	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V   I <sub>D</sub> = 4.0 A	-	0.85	1	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 3 A	-	2	-	S
<b>Dynamic</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz	-	873	-	pF
Output Capacitance	C <sub>oss</sub>		-	105	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	11	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V   I <sub>D</sub> = 6 A, V <sub>DS</sub> = 400 V	-	22	34	nC
Gate-Source Charge	Q <sub>gs</sub>		-	7.8	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	10.4	-	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 6 A R <sub>G</sub> = 14 Ω, V <sub>GS</sub> = 10 V	-	17.3	-	ns
Rise Time	t <sub>r</sub>		-	35	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	23.6	-	
Fall Time	t <sub>f</sub>		-	17	-	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain	-	0.7	-	Ω
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8	A
Pulsed Diode Forward Current	I <sub>SM</sub>		-	-	22	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 8 A, V <sub>GS</sub> = 0 V	-	-	1.5	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> , dI/dt = 100 A/μs, V <sub>R</sub> = 15 V	-	63	-	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	114	-	nC
Body Diode Reverse Recovery Current	I <sub>RRM</sub>		-	3.3	-	A

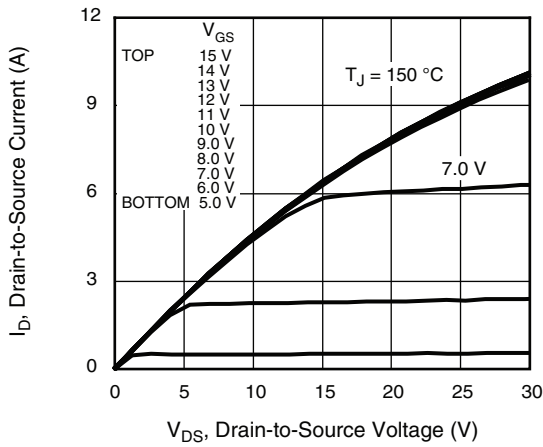
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



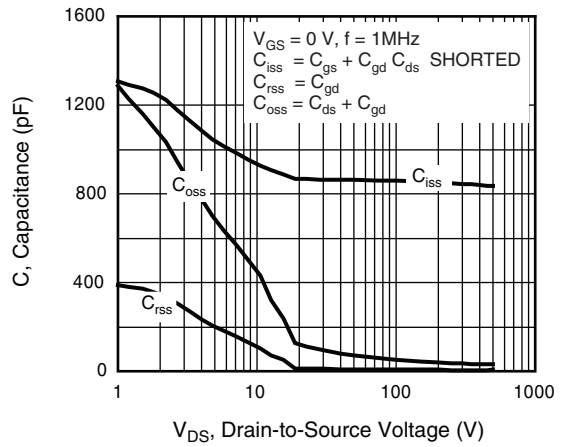
**Fig. 1 - Typical Output Characteristics**



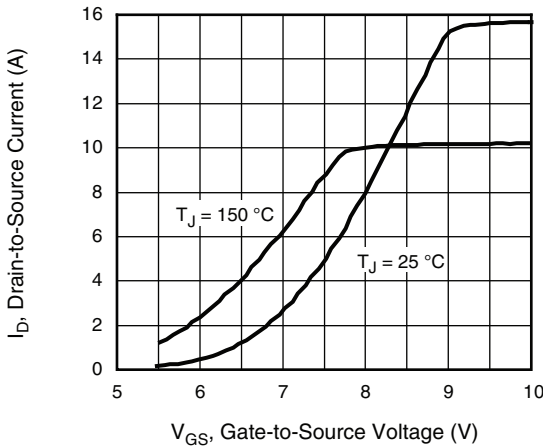
**Fig. 4 - Normalized On-Resistance vs. Temperature**



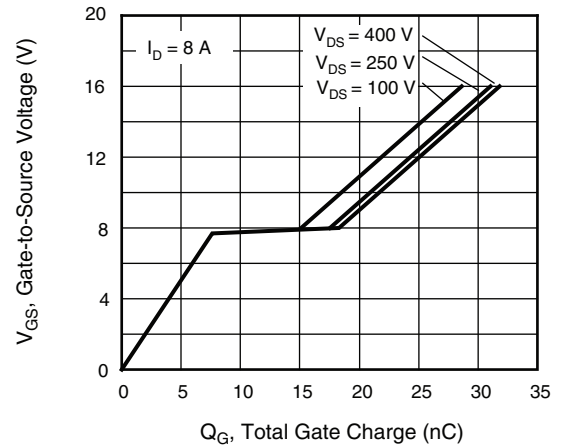
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

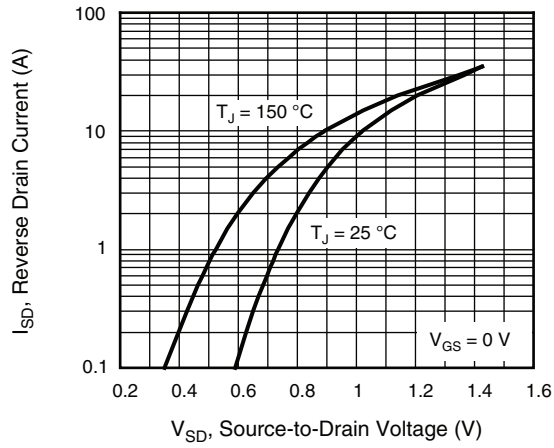


Fig. 7 - Typical Source-Drain Diode Forward Voltage

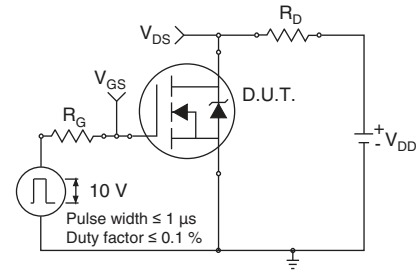


Fig. 9a - Switching Time Test Circuit

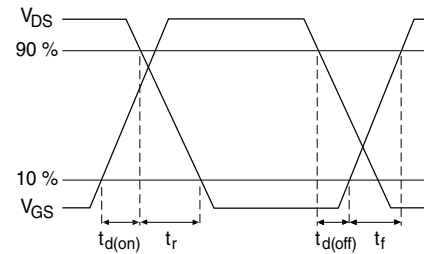


Fig. 9b - Switching Time Waveforms

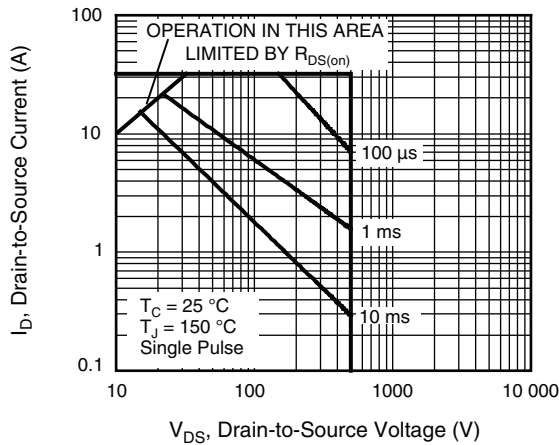


Fig. 8 - Maximum Safe Operating Area

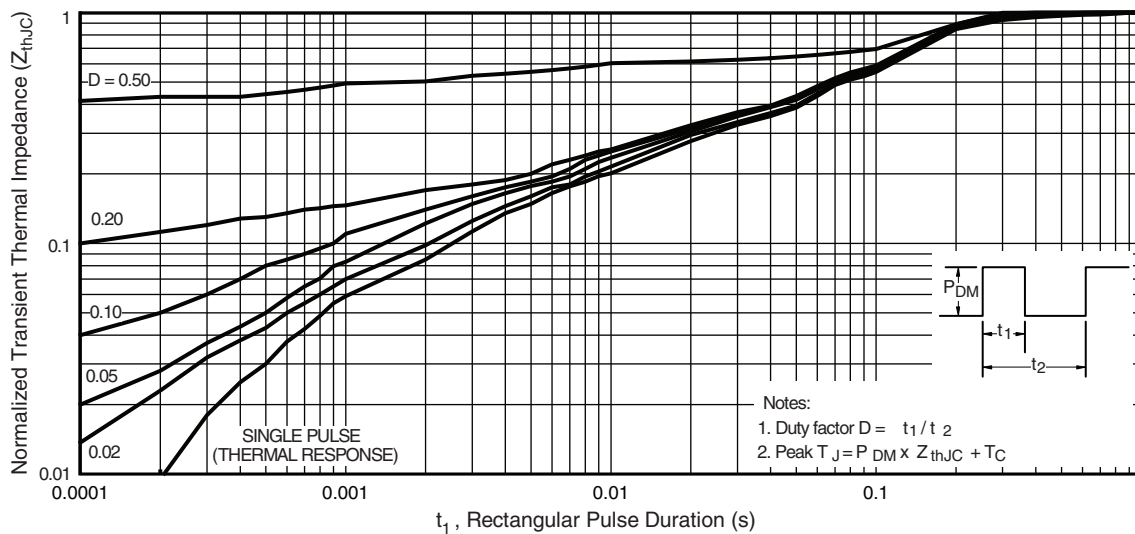
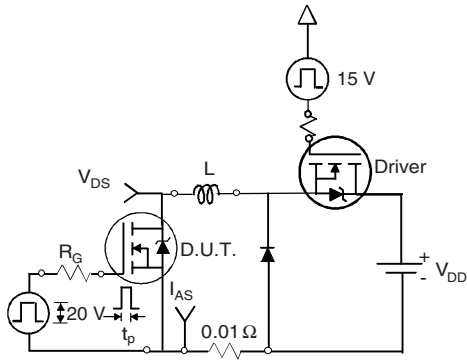
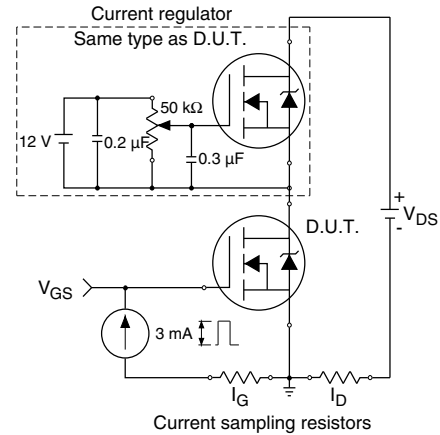


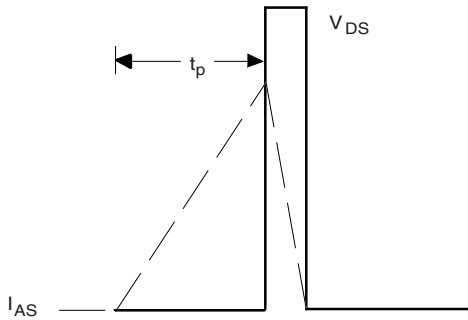
Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



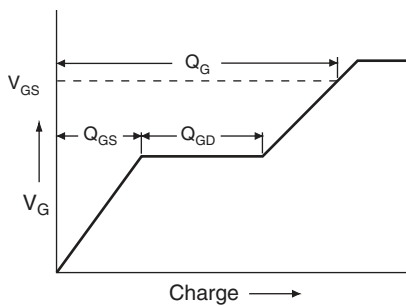
**Fig. 11a - Unclamped Inductive Test Circuit**



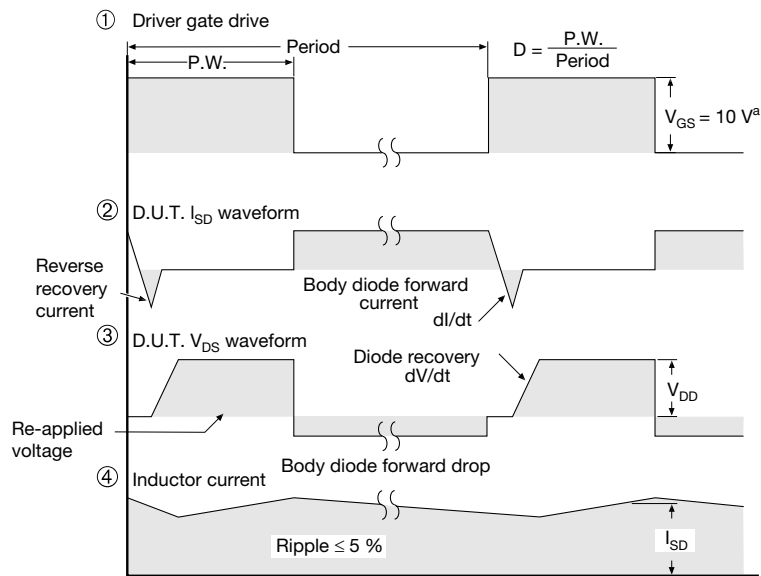
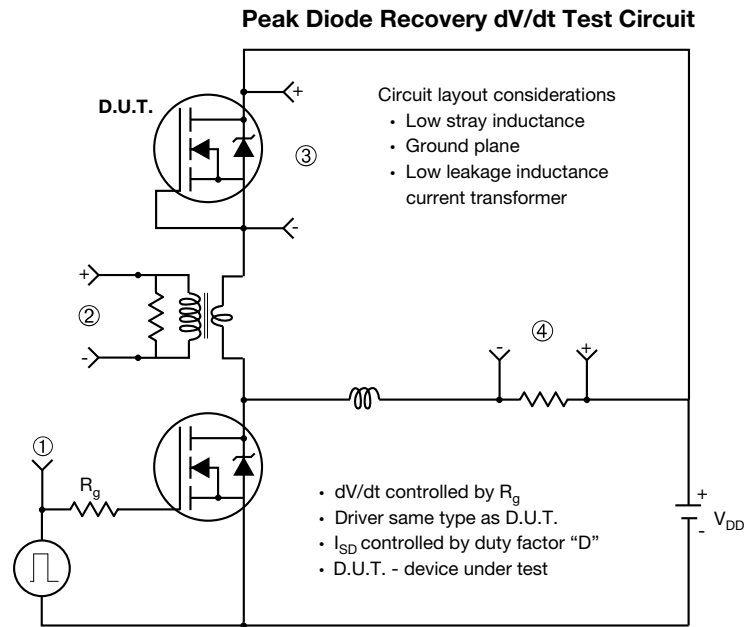
**Fig. 12b - Gate Charge Test Circuit**



**Fig. 11b - Unclamped Inductive Waveforms**



**Fig. 12a - Basic Gate Charge Waveform**



**Note**

a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 13 - For N-Channel**

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# TO-220 FULLPAK (High Voltage)

## OPTION 1: FACILITY CODE = 9



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.60	4.70	4.80
b	0.70	0.80	0.91
b1	1.20	1.30	1.47
b2	1.10	1.20	1.30
C	0.45	0.50	0.63
D	15.80	15.87	15.97
e	2.54 BSC		
E	10.00	10.10	10.30
F	2.44	2.54	2.64
G	6.50	6.70	6.90
L	12.90	13.10	13.30
L1	3.13	3.23	3.33
Q	2.65	2.75	2.85
Q1	3.20	3.30	3.40
$\varnothing R$	3.08	3.18	3.28

### Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking



OPTION 2: FACILITY CODE = Y



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

ECN: E19-0180-Rev. D, 08-Apr-2019  
DWG: 5972

Notes

1. To be used only for process drawing
2. These dimensions apply to all TO-220 FULLPAK leadframe versions 3 leads
3. All critical dimensions should C meet  $C_{pk} > 1.33$
4. All dimensions include burrs and plating thickness
5. No chipping or package damage
6. Facility code will be the 1<sup>st</sup> character located at the 2<sup>nd</sup> row of the unit marking





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