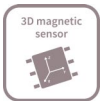
TLI493D-A2B6

Low Power 3D Hall Sensor with I²C Interface



User Manual

About this document

Scope and purpose

This document provides product information and descriptions regarding:

- I²C Registers
- I²C Interface
- Diagnostic

Intended audience

This document is aimed at engineers and developers of hard and software using the sensor TLI493D-A2B6.

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1 I²C Registers

The TLI493D-A2B6 includes several registers that can be accessed via Inter-Integrated Circuit interface (I²C) to read data as well as to write and configure settings.

1.1 Registers overview

A bitmap overview is presented in **Figure 1**. Basically the following sections are available:

- measurement data (green bits in registers 00_Htill 05_H)
- sensor status and diagnostics (grey bits in registers 05_H, 06_H, 10_H and 11_H)
- configuration parameters such as the power mode (orange bits in registers 10_H, 11_H and 13_H)

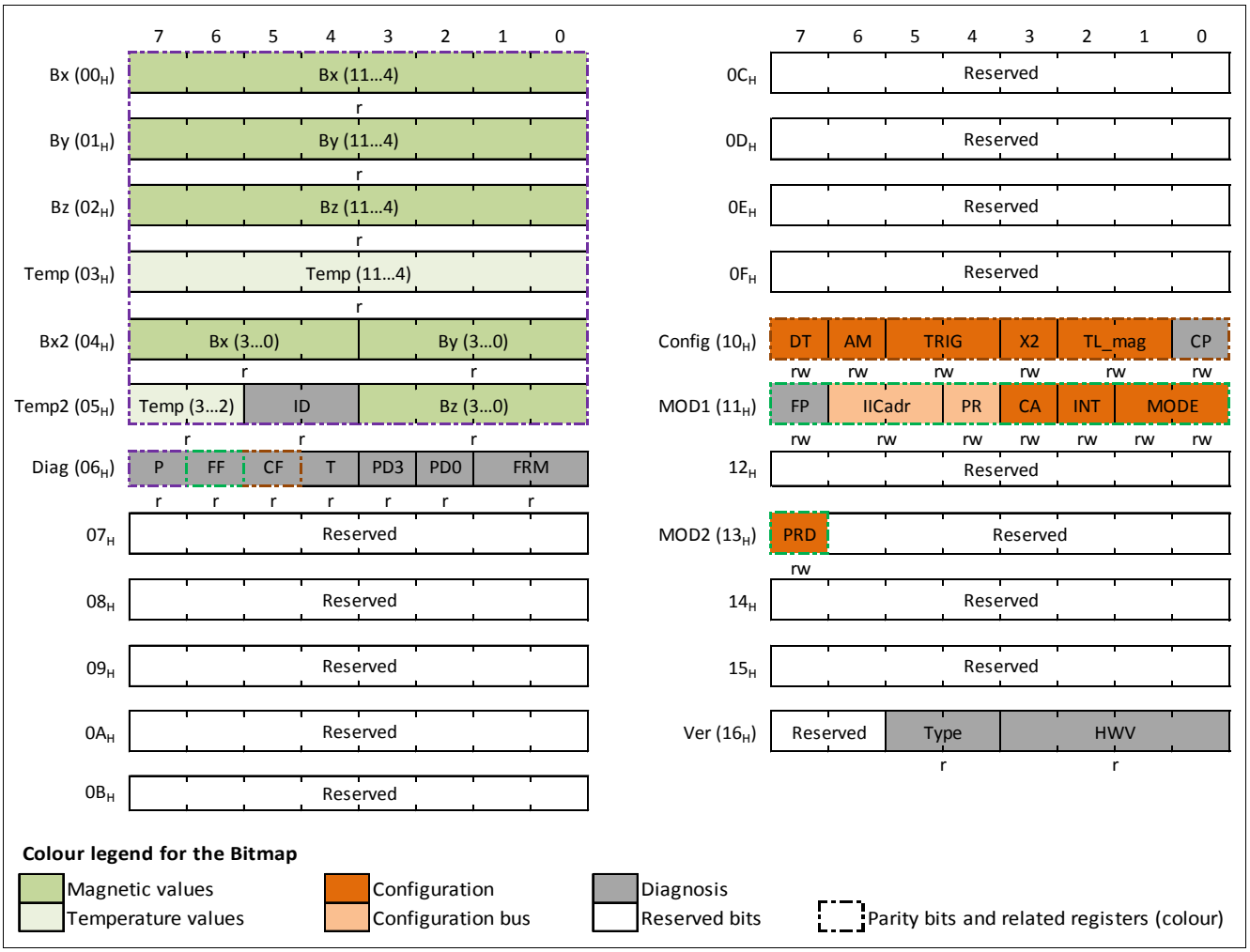


Figure 1 TLI493D-A2B6 Bitmap

The diagnostic register 06_H contains parity information as a diagnostic mechanism. The bitmap illustrates this and marks the relationship of the sections to this flags with different colored lines/frames around the bit contents.

Table 1 Registers overview

Register name	Register long name	Address
Bx, By and Bz	Magnetic values MSBs	00_H, 01_H, 02_H
Temp	Temperature value MSBs	03_H
Bx2	Magnetic values LSBs	04_H
Temp2	Temperature and magnetic LSBs and device address	05_H
Diag	Sensor diagnostic and status register	06_H
Config	Configuration register	10_H
MOD1	Power mode, interrupt, address, parity	11_H
MOD2	Low Power Mode update rate	13_H
Ver	Version register	16_H

1.2 Register descriptions

The I²C registers can be read or written at any time. It is recommended to read measurement data in a synchronized fashion, i.e. after an interrupt pulse (/INT). This avoids reading inconsistent sensor or diagnostic data, especially in fast mode. Additionally, several flags can be checked to ensure the register values are consistent and the ADC was not running at the time of readout.

1.2.1 Bit types

The TLI493D-A2B6 contains read bits, write bits and reserved bits.

Table 2 Bit Types

Abbreviation	Function	Description
r	Read	Read-only bits
rw	Read Write	Readable and writable bit
	Reserved	Bits that must keep the default values (read prior to write required)

1.2.2 Measurement data and registers combined in the I²C parity bit “P”

The I²C communication of the registers in this chapter is protected with the parity bit “P”, described in the Diag register with the address 06_H. See also Figure 1 - parity bits and related registers.

To make sure all data is consistent, the registers from 00_H to 06_H should be read with the same I²C command. Otherwise, the sampled data (X, Y, Z, Temperature) may correspond to different conversion cycles.

I²C Registers

Magnetic values MSBs

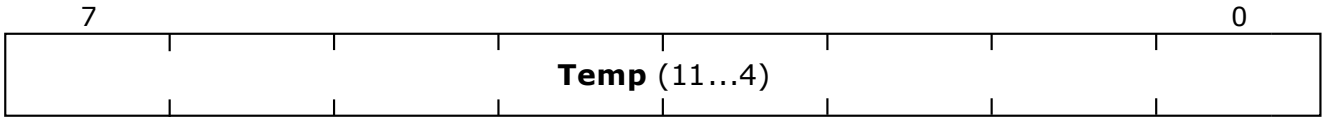
Register names	Address	Reset Value
Bx, By and Bz	00_H 01_H 02_H	80_H

Field	Bits	Type	Description
Bx, By and Bz	7:0	r	**Bx, By and Bz values** Signed value as two's complement from the HALL probes in the x, y and z-direction of the magnetic field. Contains the eight Most Significant Bits. If Bz is deactivated the Bz value is the reset value.

Back to TLI493D-A2B6 Bitmap.

Temperature value MSBs

Register name	Address	Reset Value
Temp	03_H	80_H

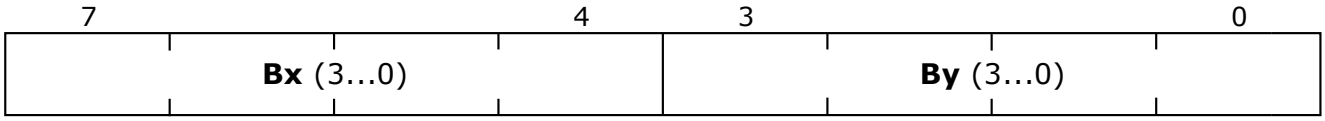


Field	Bits	Type	Description
Temp	7:0	r	**Temperature value** Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.

Back to TLI493D-A2B6 Bitmap.

Magnetic values LSBs

Register name	Address	Reset Value
Bx2	04_H	00_H



Field	Bits	Type	Description
Bx	7:4	r	**Bx value** Signed value as two's complement from the HALL probes in the x-direction of the magnetic field. Contains the four Least Significant Bits.
By	3:0	r	**By value** Signed value as two's complement from the HALL probes in the y-direction of the magnetic field. Contains the four Least Significant Bits.

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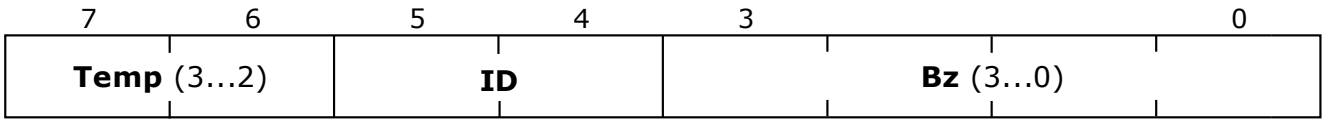
Temperature and magnetic LSBs and device address

Register name	Address	Reset Value
Temp2	05_H	00_H



Field	Bits	Type	Description
Temp	7:6	r	**Temperature value** Signed value as two's complement. If the temperature measurement is deactivated, the Temp value is the reset value.
ID	5:4	r	**ID** Readback of the sensor ID, from IICadr. µC shall verify the address sent by the sensor. See Table 4.
Bz	3:0	r	**Bz value** Signed value as two's complement from the HALL probes in the z-direction of the magnetic field. Contains the four Least Significant Bits. If Bz is deactivated the Bz value is 0_H.

Back to TLI493D-A2B6 Bitmap.

1.2.3 Configuration registers combined in the I²C parity flag “CF”

The I²C communication of the registers in this chapter is protected by the parity bit CF, which is described in the Diag register with the address 06_H. See also Figure 1 - parity bits and related registers.

Configuration register

Register name	Address	Reset Value
Config	10_H	00_H

7	6	5	4	3	2	1	0
DT	AM	TRIG		X2	TL_mag		CP

Field	Bits	Type	Description
DT	7	rw	**Disable Temperature** If 0_B temperature measurement is enabled. If 1_B temperature measurement is disabled. This means the Bx, By and Bz channels are measured. The Temp channel is disabled and contains the reset value until a new conversion with Temp is done.
AM	6	rw	**X/Y Angular Measurement** If 0_B the Bz measurement is enabled. If 1_B and the DT bit = 1_B the Bz measurement is disabled. This means the Bx and By channel is measured. The channels Bz and Temp contain the reset values until a new conversion with Bz and Temp is done. Note: If the DT bit = 0_B, the AM bit don’t care.
TRIG	5:4	rw	**Trigger options** If PR bit = 1_B (1-byte read protocol), the TRIG bits define the trigger mode of the device: If 00_B no ADC trigger on read. If 01_B ADC trigger on read before first MSB. If $1x_B$ ADC trigger on read after register 05_H. If PR bit = 0_B these bits have no effect.
X2	3	rw	**Short-range sensitivity** When this bit is set, the sensitivity of the Bx, By, and Bz ADC-conversion is doubled by a longer ADC integration time. The Temp result will not change, neither in sensitivity nor conversion time. See Table 3.
TL_mag	2:1	rw	**Magnetic temperature compensation** There are two bits for setting the sensitivity over temperature of the sensor to compensate a magnet temperature coefficient. If $00_B \rightarrow TC_0$ (no compensation) If $01_B \rightarrow TC_1$ If $10_B \rightarrow TC_2$ If $11_B \rightarrow TC_3$
CP	0	rw	**Configuration parity** The register 10_H is even parity protected with this bit. On startup or reset, this parity is OK and the CF bit in the status register 06_H is set.

Back to TLI493D-A2B6 Bitmap.

Table 3 X2 bit

X2 bit	Bx (11 ... 0)	By (11 ... 0)	Bz (11 ... 0)	T (11 ... 2)
0_B	Bx full-range	By full-range	Bz full-range	T full-range
1_B	Bx short-range	By short-range	Bz short-range	T full-range

1.2.4 Mode registers combined in the I²C parity flag “FF”

The I²C communication of the registers in this chapter is protected with the parity bit “FF”, described in the Diag register with the address 06_H. See also Figure 1 - parity bits and related registers.

Power mode, interrupt, address, parity

Register name	Address	Reset Value
MOD1	11_H	00_H

7	6	5	4	3	2	1	0
FP	IICadr		PR	CA	INT	MODE	

Field	Bits	Type	Description
FP	7	rw	**Fuse parity** The registers 11_H and 13_H (bit 7) are odd parity protected with this bit. If this parity bit is incorrect please see FF bit. To exit this state a sensor reset is necessary.
IICadr	6:5	rw	**I²C address** Bits can be set to 00_B, 01_B, 10_B or 11_B to define the slave address in bus configuration. See Table 4 and data sheet.
PR	4	rw	**I²C 1-byte or 2-byte read protocol** If 0_B this is the 2-byte read protocol: <start> <I²Cadr.> <reg.adr.> <data of reg.adr.> <data of reg.adr.+1> …. <stop> If 1_B this is the 1-byte read protocol: <start> <I²Cadr.> <data of reg.00_H> <data of reg.01_H> …. <stop> See Chapter 2.1.3
CA	3	rw	**Collision avoidance** Clock stretching only in master-controlled and low-power mode, not in fast mode. The CA bit interacts with the INT bit, see Table 5 and Chapter 2.2.

Field	Bits	Type	Description
INT	2	rw	**Interrupt enabled** If 1_B /INT disabled If 0_B /INT enabled: After a completed measurement and ADC-conversion, an /INT pulse will be generated. For bus configurations /INT timing constraints between I²C data transfers and interrupt pulses must be monitored and aligned. The INT bit interacts with the CA bit, see Table 5.
MODE	1:0	rw	**Power mode** If 00_B Low Power Mode: Cyclic measurements and ADC-conversions with a update rate, defined in the PRD registers. “No ADC trigger” must be used, see Table 6 and TRIG. If 01_B Master Controlled Mode (Power Down mode): Measurement triggering depends on the PR bit and is possible with I²C sub address byte (see Table 6) or TRIG bits. If 10_B is reserved and must not be used. If 11_B Fast Mode: The measurements and ADC-conversions are running continuously. It is recommended to set INT = 0_B and use a I²C clock speed ≥ 800 kHz.

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Table 4 Device address overview

The addresses are selected to ensure a minimum Hamming distance of 4 between them.

Address write	Address read	IICadr (bit-6)	IICadr (bit-5)	ID (bit-5)	ID (bit-4)
$6A_H$ [1)]	$6B_H$ [1)]	0_B	0_B	0_B	0_B
44_H	45_H	0_B	1_B	0_B	1_B
$F0_H$	$F1_H$	1_B	0_B	1_B	0_B
88_H	89_H	1_B	1_B	1_B	1_B

1) Default address after start up or reset.

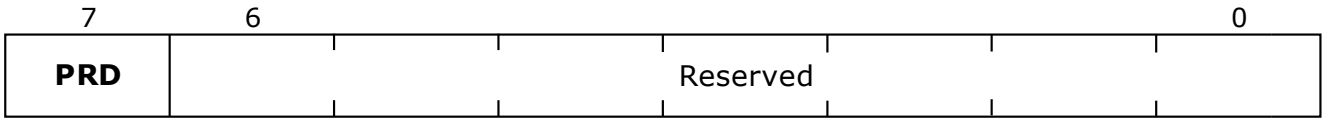
Table 5 /INT (interrupt) and clock stretching

In case the microcontroller tries to read sensor data the clock stretching pulls the SCL /INT line to low, as long as the measurement and ADC-conversion is not finished.

CA	INT	Configuration
0_B	0_B	/INT is enabled and will not be transmitted between <START> and <STOP>. /INT collision avoidance active.
0_B	1_B	/INT disabled. Clock stretching enabled. Suppress sensor read out during ongoing ADC conversion. This configuration must not be used with the “read” trigger-bits (7:5) = 010_B or 011_B (see Table 6) or with the trigger option TRIG bit = 01_B.
1_B	0_B	/INT is enabled and will be transmitted between <START> and <STOP>. /INT may collide with I²C clock from microcontroller.
1_B	1_B	/INT disabled. Clock stretching disabled. Unsynchronized sensor readouts may collide with ADC conversion.

Low Power Mode update rate

Register name	Address	Reset Value
MOD2	13_H	(bits 7:5) 000_B



Field	Bits	Type	Description
PRD	7	rw	**Update rate settings** If 0_B f_{Update} = fast. If 1_B f_{Update} = slow.
Reserved	6:0		**Factory settings**

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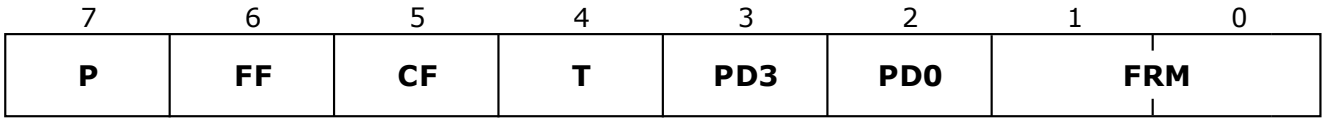
1.2.5 Diagnostic, status and version registers

The device provides diagnostic and status information in register 06_H and version information in register 16_H.

Sensor diagnostic and status register

Register name	Address	Reset Value
Diag	06_H	60_H



Field	Bits	Type	Description
P	7	r	**Bus parity** This bit adds up to an odd parity of the registers 00_H through 05_H (including 05_H), described in Chapter 1.2.2. The parity bit is generated during the I²C readout. The address byte, register byte and acknowledge bits are not included in the parity sum. If the parity calculated by the microcontroller after I²C reads is incorrect, these values must be treated as invalid.

Field	Bits	Type	Description
FF	6	r	**Fuse parity flag** Provides a flag from the internal fuse parity check of registers 11_H and 13_H (bit 7). This parity check includes the FP bit. If 1_B parity is OK. If 0_B the parity is not correct. The sensor must be considered defective and must no longer be used. A sensor with an invalid fuse parity disconnects its SDA. It will automatically go to low-power mode and only uses the /INT signal to communicate the error (collision avoidance is enabled).
CF	5	r	**Configuration parity flag** Provides a flag from the internal configuration parity check of register 10_H. This parity check includes the CP bit. After startup or after reset the CP bit is true. If 1_B parity is OK. If 0_B parity is not OK.
T	4	r	**T bit** If 1_B data in registers 00_H till 05_H are invalid measurement data. If 0_B data in registers 00_H till 05_H are valid measurement data.
PD3	3	r	**Power-down flag 3** If 1_B ADC-conversion of Temp is completed and valid measurement data can be read out. Thus it must be 1_B at readout. If 0_B ADC-conversion of Temp is running and read measurement data are invalid. Any readout with PD3 bit = 0_B should be considered invalid. At startup, this is 0_B until one ADC conversion has been performed. The value then changes to 1_B.
PD0	2	r	**Power-down flag 0** If 1_B the ADC conversion of Bx is completed and valid measurement data can be read out. Thus it must be 1_B at readout. If 0_B the ADC conversion of Bx is running and read measurement data are invalid. Any readout with PD0 bit = 0_B should be considered invalid. At startup, this is 0_B until one ADC conversion has been performed. The value then changes to 1_B.
FRM	1:0	r	**Frame counter** Increments at every updated ADC-conversion, once a X/Y/Z/T or X/Y/Z or X/Y conversion is completed and the new measurement data have been stored in the registers 00_H till 05_H. The microcontroller shall check if bits change in consecutive conversion runs.

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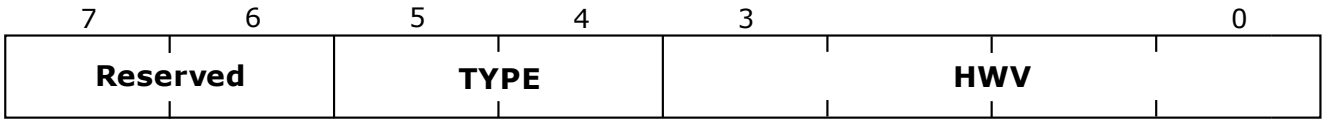
I²C Registers

Version register

Register name	Address	Reset Value
Ver	16_H	$C9_H$, $D9_H$ or $E9_H$



Field	Bits	Type	Description
Reserved	7:6		Factory settings
TYPE	5:4	r	Chip feature If 11_B: device without Wake Up feature.
HWV	3:0	r	Hardware revision If 9_H it is the B21 design step.

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2 I²C Interface

The TLI493D-A2B6 uses Inter-Integrated Circuit (I²C) as the communication interface with the microcontroller.

The I²C interface has three main functions:

- Sensor configuration.
- Transmit measurement data.
- Interrupt handling.

This sensor provides two I²C read protocols:

- 16-bit read frame (µC is driving data), so called **2-byte read command**.
- 8-bit read frame (µC is driving data), so called **1-byte read command**.

2.1 I²C protocol description

The TLI493D-A2B6 provides one I²C write protocol, based on 2 bytes and two I²C read protocols. Default is the 2-byte read protocol. With the **PR** bit it can be selected, if the 1-byte read protocol or the 2-byte read protocol is used.

2.1.1 General description

- The interface conforms to the I²C fast mode specification (400kBit/sec max.), but can be driven faster according to the data sheet.
- The TLI493D-A2B6 does not support “repeated starts”. Each addressing requires a start condition.
- The interface can be accessed in any power mode.
- The data transmission order is Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- A I²C communication is always initiated with a start condition and concluded with a stop condition by the master (microcontroller). During a start or stop condition the SCL line must stay “high” and the SDA line must change its state: SDA line falling = start condition and SDA line rising = stop condition.
- Bit transfer occur when the SCL line is “high”.
- Each byte is followed by one ACK bit. The ACK bit is always generated by the recipient of each data byte.
  - If no error occurs during the data transfer, the ACK bit will be set to “low”.
  - If an error occurs during the data transfer, the ACK bit will be set to “high”.
  - If the communication is finished (before the Stop condition), the ACK bit must be set to “high”.

2.1.2 I²C write command

Write I²C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- The register address identifies the register in the bitmap (according to **Figure 1**) with which the first data byte will be written.
- Data bytes are transmitted as long as the SCL line generates pulses. Each additional data byte increments the register address until the stop condition occurs.
- Bytes transmitted beyond the register address frame are ignored and the corresponding ACK bit is sent “high”, indicating an error.

The I²C write communication frame consists of:

- The start condition.
- The sensor address, according to Table 4.
- Write command bit = “low” (read = “high”).
- Acknowledge ACK.
- Trigger bits, according to Table 6.
- The register address, according to Figure 1.
- Acknowledge ACK.
- Writing of one or several bytes to the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

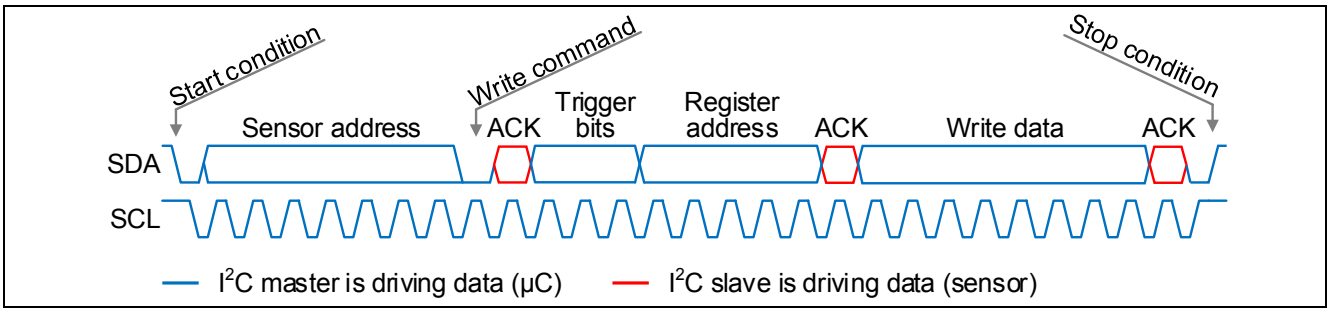

Figure 2 General I²C write frame format: Write data from microcontroller to sensor

Trigger bits in the I²C protocol

The trigger bits are used in Power Down Mode. The Power Down Mode is used in the Master Controlled Mode, when no measurement is running. Thus the trigger bits are relevant for the Master Controlled Mode as well.

For a more silent measurement environment it is recommended to separate the measurement and the communication as much as possible, by using the trigger bits = 001_B or trigger bits = 100_B and communicate between two measurements with reduced overlap of measurement and communication.

Table 6 I²C trigger bits

Read/Write command	Trigger-bit 7	Trigger-bit 6	Trigger-bit 5	Trigger command
0_B	0_B	0_B	0_B	no ADC trigger
0_B	0_B	0_B	1_B	ADC trigger after write frame is finished, Figure 4
0_B	0_B	1_B	0_B	no ADC trigger
0_B	0_B	1_B	1_B	ADC trigger after write frame is finished, Figure 4
0_B	1_B	0_B	0_B	no ADC trigger
0_B	1_B	0_B	1_B	ADC trigger after write frame is finished, Figure 4
0_B	1_B	1_B	0_B	no ADC trigger
0_B	1_B	1_B	1_B	must not be used
1_B	0_B	0_B	0_B	no ADC trigger
1_B	0_B	0_B	1_B	no ADC trigger
1_B	0_B	1_B	0_B	ADC trigger before first MSB, Figure 3
1_B	0_B	1_B	1_B	ADC trigger before first MSB, Figure 3

Table 6 I²C trigger bits (cont'd)

Read/Write command	Trigger-bit 7	Trigger-bit 6	Trigger-bit 5	Trigger command
1_B	1_B	0_B	0_B	ADC trigger after register 05_H, Figure 5
1_B	1_B	0_B	1_B	ADC trigger after register 05_H, Figure 5
1_B	1_B	1_B	0_B	ADC trigger after register 05_H, Figure 5
1_B	1_B	1_B	1_B	must not be used

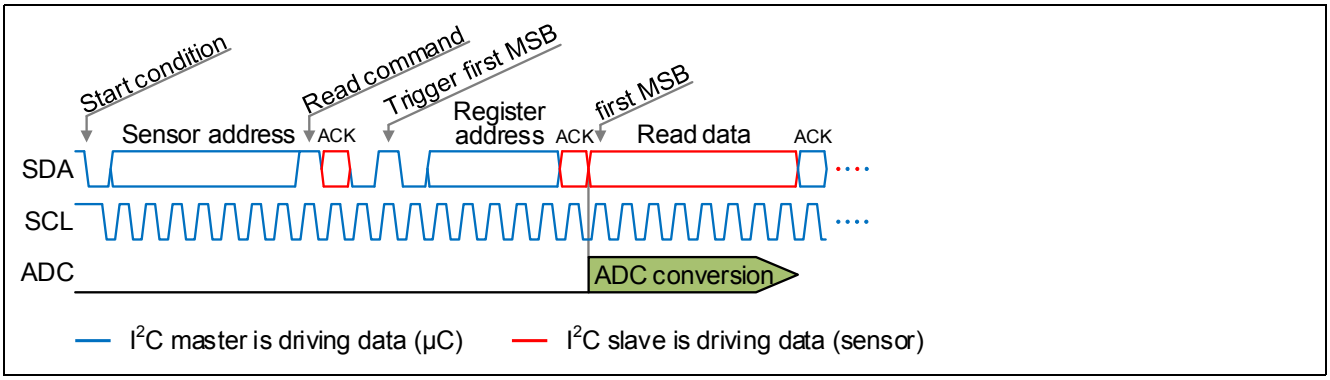

Figure 3 ADC trigger before sending first MSB of data registers, I²C trigger bits 010_B.

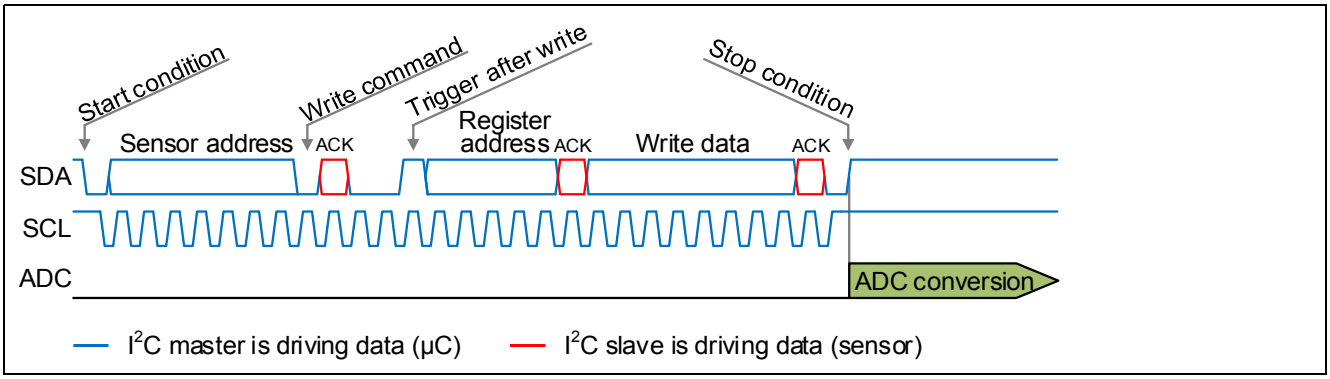

Figure 4 ADC trigger after write frame is finished, I²C trigger bits 001_B.

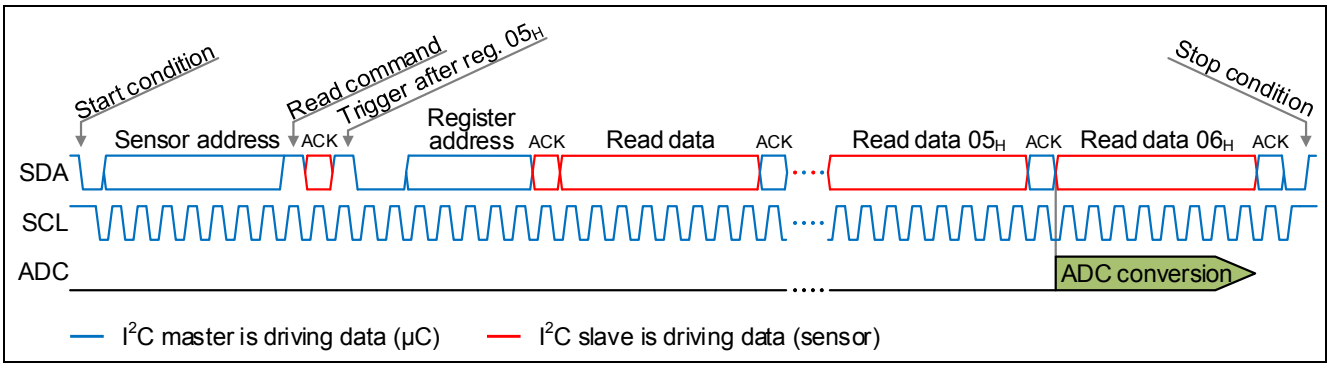

Figure 5 ADC trigger after register 05_H, I²C trigger bits 100_B.

Example I²C write communication

An example of a write communication is provided in Figure 6.

In this example the sensor with the address $6A_H$ / $6B_H$ (see Table 4) should be configured for:

- Master Controlled Mode,
- /INT disabled,
- Clock stretching enabled,
- No trigger of a measurement.
- Other settings should be kept as is.

Implementation:

- The microcontroller generates a start condition.
- Configuration changes can only be performed with a write command. The address for write operation of this sensor is $6A_H = 01101010_B$.
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller.
- No measurement is performed if the trigger bits = 000_B.
- The register to change the required settings is 11_H according the bitmap Figure 1 = 10001_B.
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller.
- The parity bit “FP” is the odd parity of the registers 11_H and 13_H (bits 7:5), see FP register, thus it is not possible to quantify it in this example.
- The sensor address should not be changed, i.e. the sensor address $6A_H$ / $6B_H$ should be kept. Thus the IICadr bits = 00_B, see IICadr registers.
- The 2-byte protocol should be kept as is. Thus the PR bit = 0_B.
- In order to enable clock stretching and disable /INT the CA bit must be set to 0_B and the INT bit must be set to 1_B (see Table 5).
- To use the Master Controlled Mode the MODE bits must be set to 01_B.
- If the sensor detects no error the ACK = 0_B is transmitted back to the microcontroller.
- The microcontroller generates the stop condition.

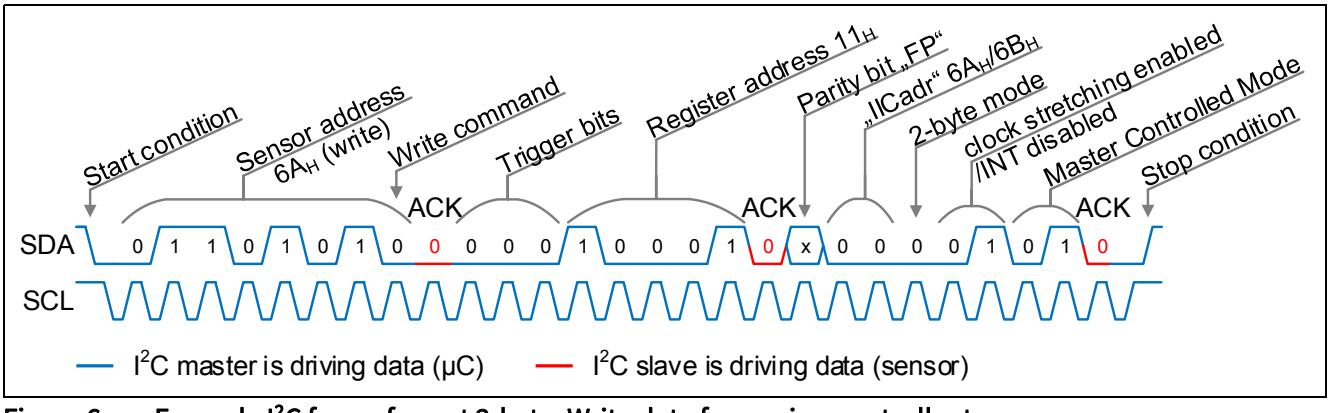

Figure 6 Example I²C frame format 2-byte: Write data from microcontroller to sensor

2.1.3 I²C read commands

Read I²C communication description:

- The purpose of the sensor address is to identify the sensor with which communication should occur. The sensor address byte is required independently of the number of sensors connected to the microcontroller.
- Only available in the 2-byte read command: The register address identifies the register in the bitmap (according **Figure 1**) from which the first data byte will be read.
  In the 1-byte read command the read out starts always at the register address 00_H.
- As many data bytes will be transferred as long as pulses are generated by the SCL line. Each additional data byte increments the register address. Until the stop condition occurs.
- If bytes are read beyond the register address frame the sensor keeps the SDA = 1_B.
- If the microcontroller reads data and does not acknowledge the sensor data (ACK = 1_B) the sensor keeps the SDA = 1_B until the next stop condition.

2.1.3.1 2-byte read command

The I²C read communication frame consists of:

- The start condition.
- The sensor address, according to **Table 4**.
- Read command bit = “high” (write = “low”).
- Acknowledge ACK.
- Trigger bits, according to **Table 6**.
- The register address, according to **Figure 1**.
- Acknowledge ACK.
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

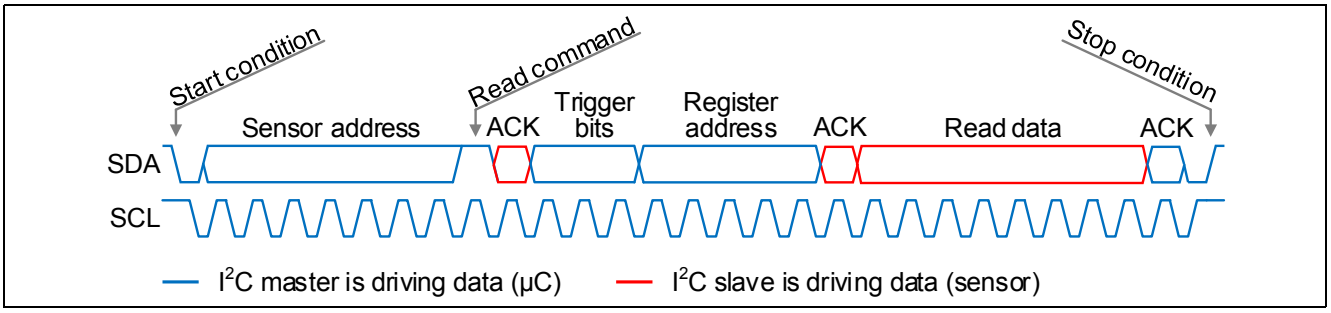

Figure 7 General I²C frame format 2-byte: Read data from sensor to microcontroller

2.1.3.2 1-byte read command

The 1-byte read mode can be entered, by configuring the **PR** bit with an write communication. E.g. with the write cycle:

- start condition
- $6A_H$ (sensor address)
- 11_H (register address)
- XXX1 $XXXX_B$ (**PR** bit = 1_B)
- stop condition

I²C Interface

The I²C communication frame consists of:

- The start condition.
- The sensor address, according to Table 4.
- Read command bit = “high” (write = “low”).
- Acknowledge ACK.
- Reading of one or several bytes from the sensor, each byte followed by an acknowledge ACK.
- The stop condition.

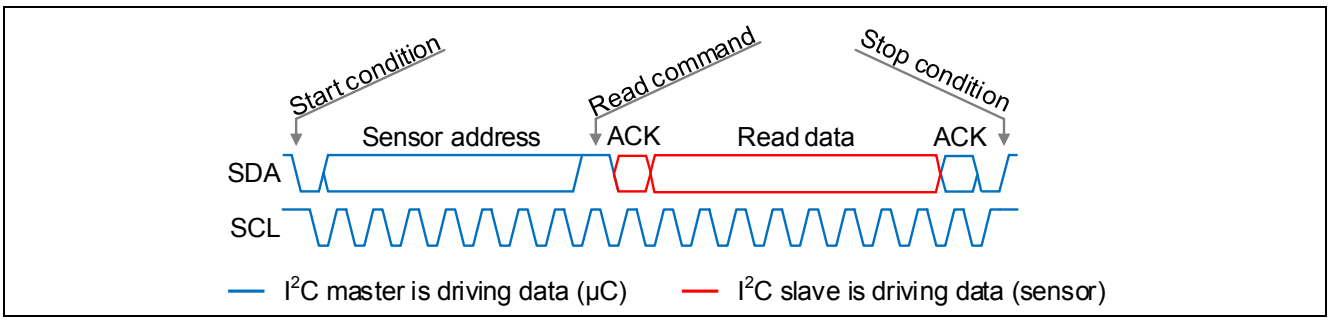

Figure 8 General I²C frame format 1-byte: Read data from sensor to microcontroller

Example I²C 1-byte read communication

An example of a read communication is provided in Figure 9.

In this example, the sensor with the address $6A_H$ / $6B_H$ (see Table 4) should read out the measurement values, registers 00_H - 05_H and the diagnostic register 06_H:

Implementation:

- The microcontroller generates a start condition.
- The address for read operation of this sensor is $6B_H = 01101011_B$. This address value must be transmitted by the microcontroller to the sensor.
- If the sensor detects no error, the ACK = 0_B is transmitted back to the microcontroller.
- The microcontroller must go on clocking the SCL line.
- The sensor transmits 8 data bits of register 00_H to the microcontroller.
- If the microcontroller detects no error the ACK = 0_B is transmitted back to the sensor.
- The microcontroller must go on clocking the SCL line.
- The sensor transmits 8 data bits of register 01_H to the microcontroller.
- ...
- After transmitting the register 06_H the microcontroller transmits a NACK.
- The microcontroller generates the stop condition.

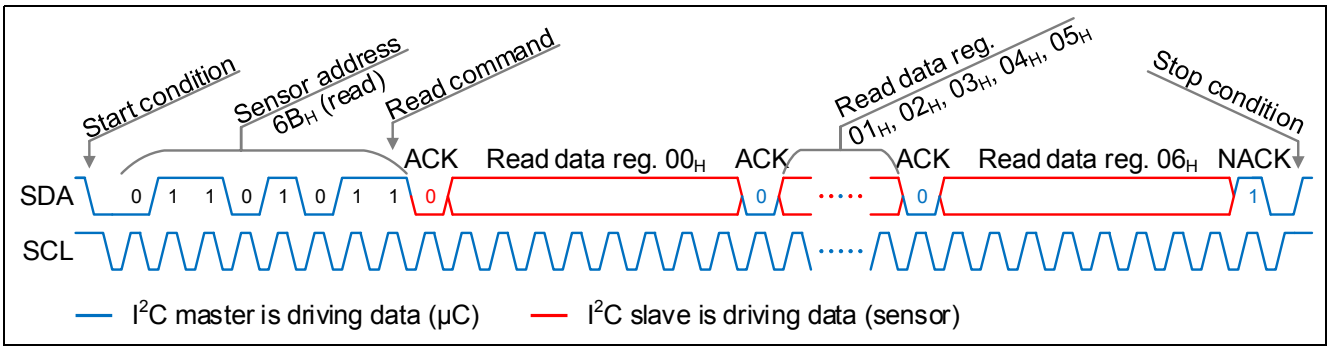

Figure 9 Example I²C frame format 1-byte: Read data from sensor to microcontroller

2.2 Collision avoidance and clock stretching

Using the configuration bits CA and INT, collision avoidance and clock stretching can be configured. An overview is given in Table 5. An example without collision avoidance and clock stretching is shown in Figure 10. In this example:

- the sensor interrupt disturbs the I²C clock, causing an additional SCL pulse which shifts the data read out by one bit.
- the data read out starts when the ADC conversion is running.

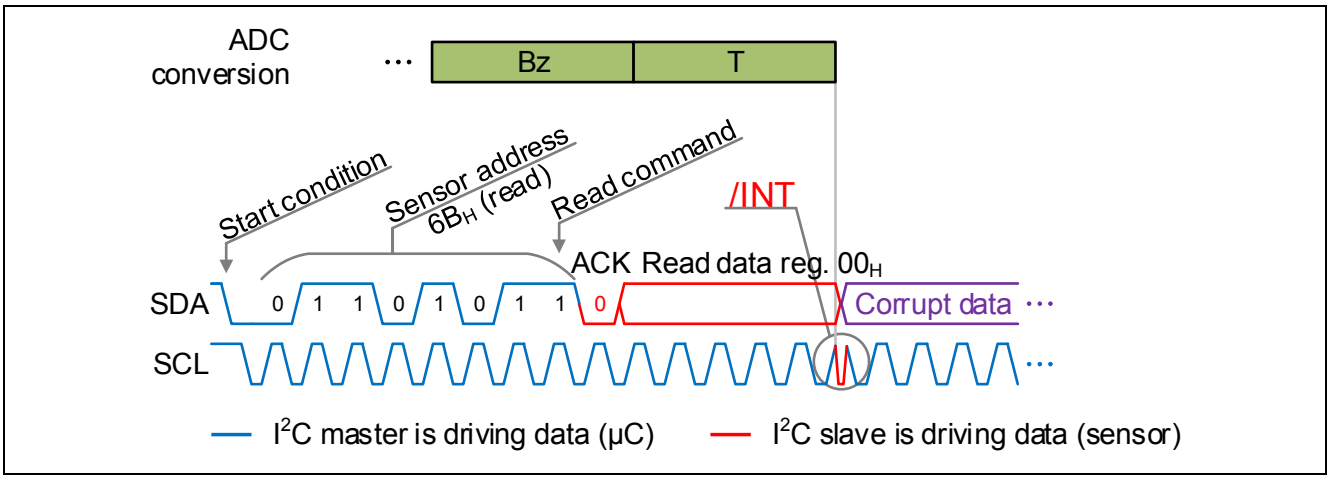

Figure 10 Example without collision avoidance CA bit =1$_B$ and INT bit = 0$_B$

2.2.1 Collision avoidance (CA bit = 0$_B$ and INT bit = 0$_B$)

In a bus configuration combined with an activated interrupt signal /INT it must be assured, that during any communication no interrupt /INT occurs. With collision avoidance enabled, the sensor monitors for any start/stop condition, even if it does not detect a valid bus address. The interrupt signal /INT is omitted whenever a start condition is detected, as shown in Figure 11, in contrast to Figure 10. Only after a stop condition is detected, the interrupt signal /INT is generated by the sensor.

It is strongly recommended to use the collision avoidance feature whenever the interrupt signal /INT is used.

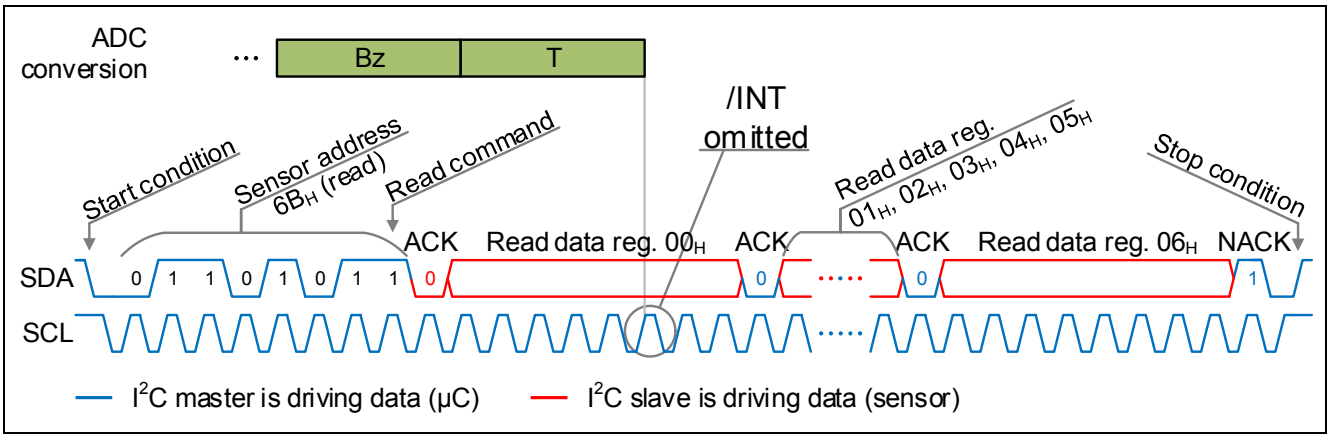

Figure 11 Example with collision avoidance CA bit =0_B and INT bit = 0_B

2.2.2 Clock stretching (CA bit = 0_B and INT bit = 1_B)

With the clock stretching feature, the data read out starts after the ADC conversion is finished. Thus it can be avoided that during an ADC conversion old or corrupted measurement results are read out, which may occur when the ADC is writing to a register while this is being read out by the microcontroller. The clock stretching feature is shown in Figure 12 in combination with a 1-byte read command. Clock stretching can also be used with a 2-byte read command.

The sensor pulls the SCL line to low during the following situation:

- An ADC conversion is in progress.
- The sensor is addressed for register read (writes are never affected by clock stretching).
- The sensor is about to transmit the valid ACK in response to the I²C addressing of the microcontroller.

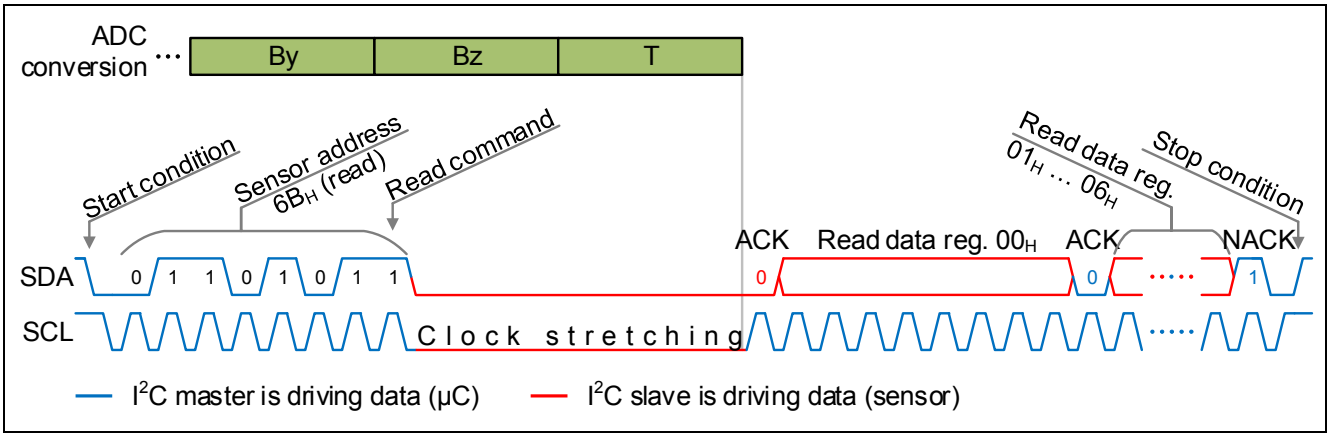

Figure 12 Example with clock stretching CA bit =0_B and INT bit = 1_B

2.3 Sensor reset by I²C

If the microcontroller is reset, the communication with the sensor may be corrupted, possibly causing the sensor to enter an incorrect state. The sensor can be reset via the I²C interface by sending the following command sequence from the microcontroller to the sensor:

- Start condition,
- sending FF_H,
- stop condition.
- Start condition,
- sending FF_H,
- stop condition.
- Start condition,
- sending 00_H,
- stop condition.
- Start condition,
- sending 00_H,
- stop condition.
- 30µs delay.

After a reset, the sensor must be reconfigured to the desired settings. The reset sequence uses twice the identical data to assure a proper reset, even when an unexpected /INT pulse occurs.

Spikes can be interpreted as bus signals causing an action. E.g. when the collision avoidance feature is active and if the SDA line spikes together with SCL line this could be interpreted as start condition, blocking further /INT pulses until a stop condition appears on the bus. In such a case the sensor must be reset in order to initialize it. If the sensor does not respond after the reset, it must be considered defective.

Such spikes may occur as the sensor powers up. Because of this we recommend to using the reset sequence after each power up before configuring the sensor.

If the microcontroller resets during an ongoing I²C communication, the SDA line could get stuck low. This would block the I²C bus and is a well-known limitation of the I²C interface. To recover from this situation please use the reset sequence described in this chapter.

2.4 Sensor Initialization and Readout example

To ensure that both the microcontroller and the sensor are synchronized and properly initialized, it is recommended to apply the I²C reset and upload the fuse register settings each time the microcontroller is reset, see Figure 13.

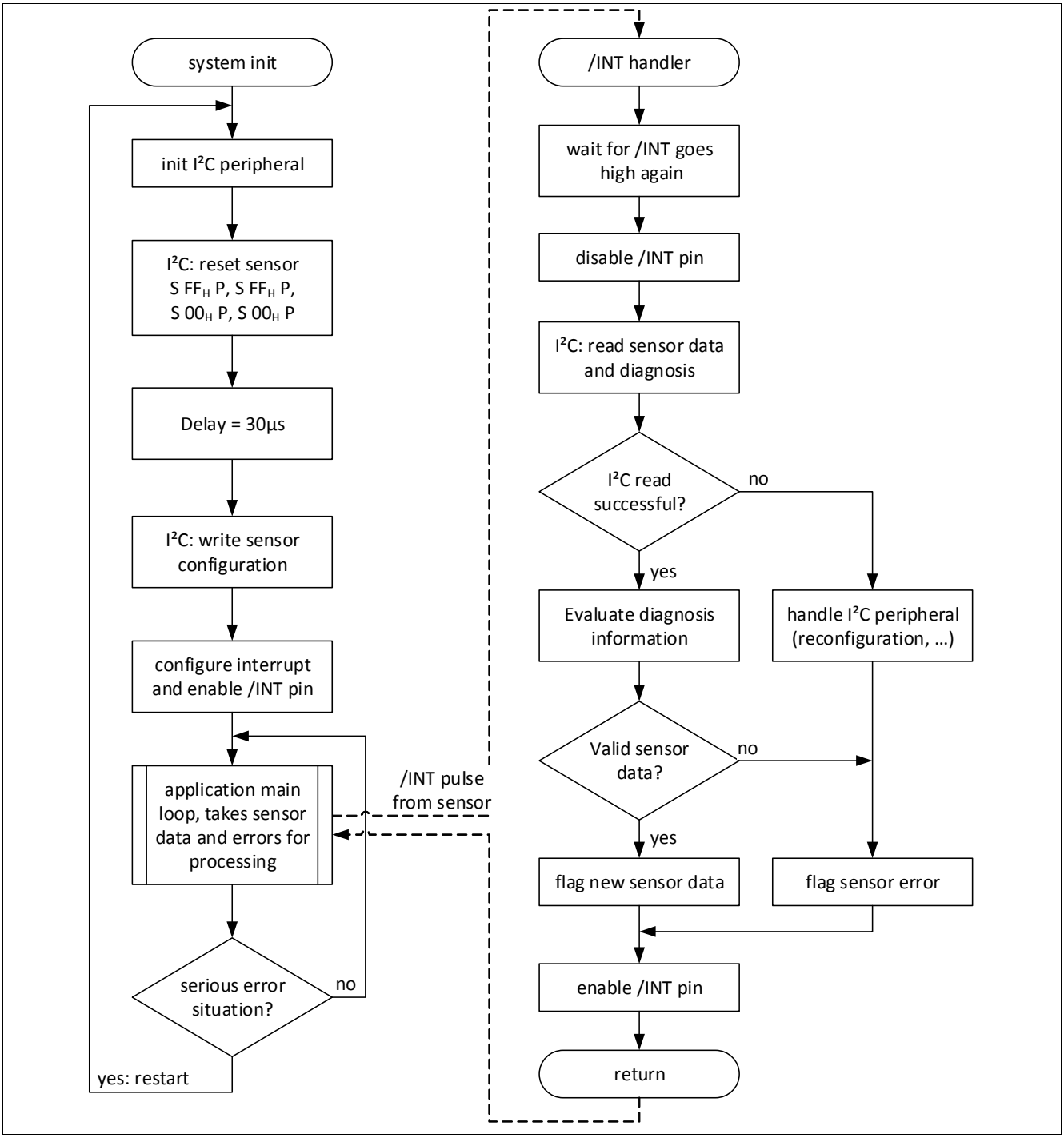

Figure 13 Microcontroller software flowchart for TLI493D-A2B6

2.5 Loss of V_{DD} impact on I²C bus

If the SDA or SCL line is pulled “low” and the sensor is disconnected from the V_{DD} supply line, the affected I²C line will most likely get a stuck in the Low state and will interfere with the communication on the bus.

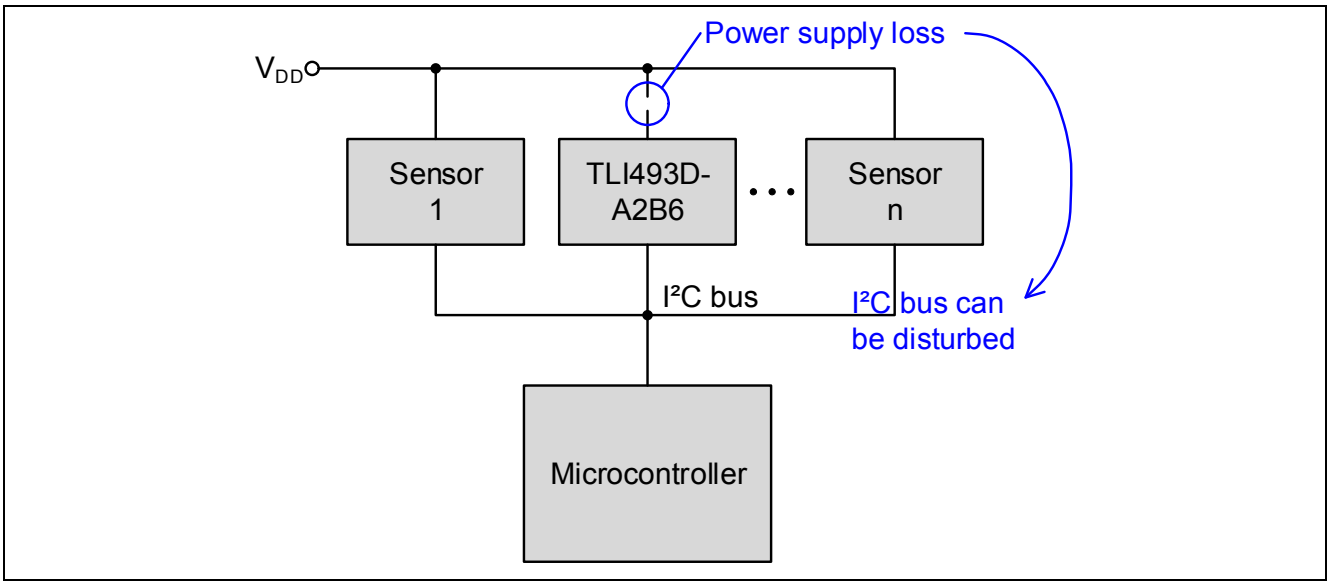

Figure 14 Example of I²C bus and a TLI493D-A2B6 with disconnected V_{DD}

When V_{DD} is pulled to GND the SDA and SCL line will not disturb the bus.

3 Diagnostic

The sensor TLI493D-A2B6 provides diagnostic functions. These functions are running in the background, providing results, which can be checked by the microcontroller for the verification of the measurement results.

To ensure the integrity of received data the following diagnostic functions are available.

3.1 Parity bits and parity flags

Parity bits:

- FP (mode parity bit)
- CP (configuration parity bit)
- P (bus parity bit)

Parity flags:

- FF (mode parity flag)
- CF (configuration parity flag)

3.2 Power-down flags

During measurements and during ADC conversion, the sensor monitors if the supply voltage is correct and if the conversion is finished. This is indicated by the PD3 and PD0 registers.

3.3 Frame Counter

The frame counter FRM registers are incremented by one when a conversion is completed.

4 Terminology

A	
ACK	Acknowledge
ADC	Analog/Digital Converter
adr	address
E	
EMC	Electromagnetic Compatibility
G	
GND	Ground
I	
ID	IDentification
I^2C (I2C)	Inter-Integrated Circuit
/INT	Interrupt pin, Interrupt signal
L	
LSB	Least Significant Bit
M	
Magnetic field	Magnetic flux density that the sensor measures.
min	minimum
MSB	Most Significant Bit
max	maximum
P	
PCB	Printed Circuit Board
R	
reg	register
S	
SCL	Clock pin
SDA	Data pin
Sensor	Refers to the TLI493D-A2B6 product
Sensor module	Refers to the TLI493D-A2B6 product and all the passive elements in the customer's module
Supply	Refers to the sensor supply pins V_{DD} and GND (the unused pins are assumed to be connected to GND as well).
V	
V_{DD}	Supply voltage
µ	
µC	Microcontroller

5 Revision history

Revision	Date	Changes
Ver. 1.11	2019-05-28	Register MODE updated.
Ver. 1.1	2018-09-20	TRIG updated. MOD2 updated. Table 5 updated. Trigger bits in the I²C protocol updated. Table 6 updated and Figure 4 accordingly. Figure 5 updated. At the end of a data read out a NACK is transferred before the stop condition (according to the standard and the product). This was updated: Chapter 2.1.1, Figure 9, Figure 11, Figure 12 Editorial changes.
Ver. 0.1	2018-04-20	Initial release.

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