ALLEGRO microsystems

A1365

Low-Noise, High-Precision, Programmable Linear Hall-Effect Sensor IC

with High-Bandwidth (120 kHz) Analog Output and Integrated Fault Comparator with Self-Test Diagnostic Mode

FEATURES AND BENEFITS

- Proprietary segmented linear temperature compensation (TC) technology provides a typical accuracy of 1% over the full operating temperature range
- Self-Test diagnostic mode can be used to achieve a high level of functional safety within a system
- 120 kHz nominal bandwidth achieved via proprietary packaging and chopper stabilization techniques
- Over Field Fault signal with 6-bit programmable trigger levels, 2-bit programmable hysteresis, and latching or non-latching behavior
- Over Field Fault response time < 4.5 µs (typ)
- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits
- Customer-programmable, high-resolution offset and sensitivity trim
- Available in a 1-mm-thick SIP through-hole package

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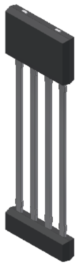
PACKAGE: 4-pin SIP (suffix KT)

TN Leadform



Not to scale

TH Leadform

Contact Allegro about legacy leadform options

DESCRIPTION

The A1365 linear output Hall-effect sensor IC is specifically designed to provide a highly accurate output with improved resolution at high bandwidth for use in current-sensing applications. This device employs a segmented, linearly interpolated temperature compensation technology, which provides greater accuracy in sensitivity and offset voltage trimming and hence virtually zero temperature drift. This improvement greatly reduces the total error of the device across the operating temperature range.

A user-activated Self-Test diagnostic mode verifies the A1365 Sensitivity and Over Field Fault functionality and can be used to achieve a high level of functional safety in application.

The highly programmable Over Field Fault signal ($\overline{\text{FAULT}}$ pin) can be used to detect a high magnetic field condition. Broken ground wire detection, undervoltage lockout for V_{CC} below specification, and user-selectable output voltage clamps are also included, which are important for high reliability in automotive applications. The sensor accuracy and diagnostic capability make it ideally suited for automotive sockets such as HEV inverter and DC-to-DC converter applications.

The A1365 Hall-effect sensor IC is extremely sensitive, fast, and temperature-stable. The accuracy and flexibility of this device is enhanced by user programmability, performed via the V_{CC} supply and the output pins, which allows the device to be optimized in the application.

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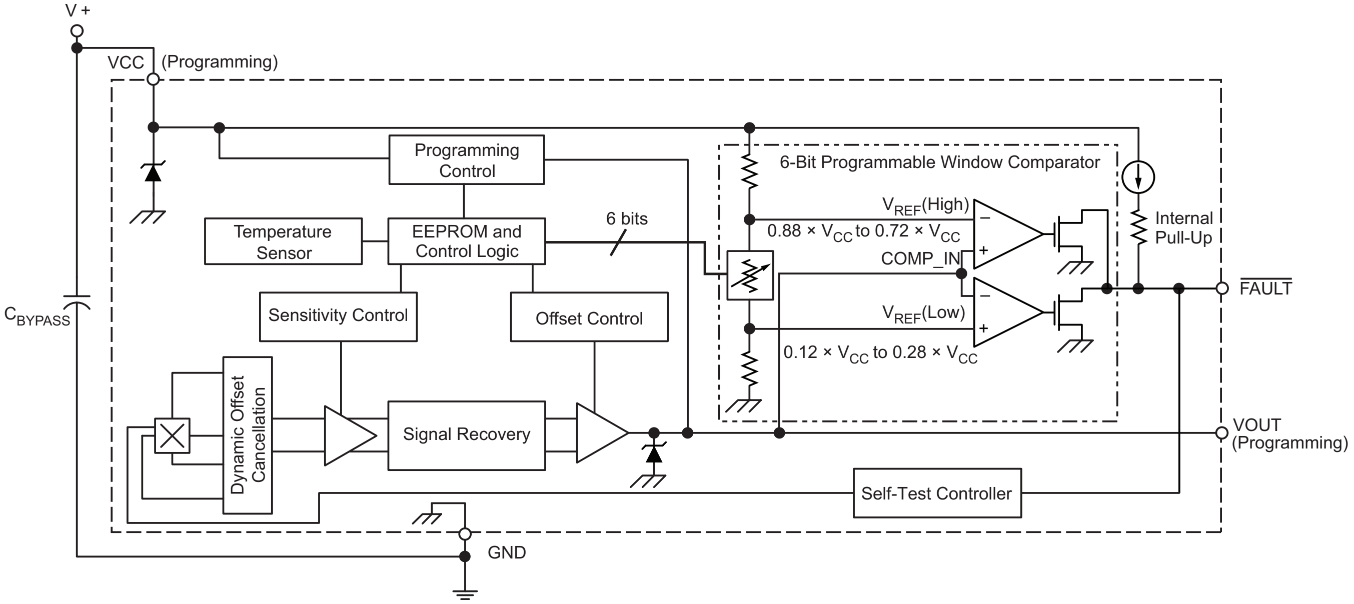


Functional Block Diagram

A1365-GS-DS, Rev. 8
MCO-0000334

September 28, 2020

FEATURES AND BENEFITS (CONTINUED)

- Factory-programmed sensitivity and quiescent output voltage TC with extremely stable temperature performance
- Selectable sensitivity range between 0.6 and 14 mV/G through use of coarse sensitivity program bits
- Ratiometric sensitivity, quiescent voltage output, and clamps enable simple interface with application A-to-D converter (ADC)
- Output voltage clamps provide short-circuit diagnostic capabilities
- Open-circuit detection on ground pin (broken wire)
- Undervoltage lockout for V_{CC} below specification
- Wide ambient temperature range: –40°C to 150°C

DESCRIPTION (CONTINUED)

This ratiometric Hall-effect sensor IC provides a voltage output that is proportional to the applied magnetic field. The quiescent output voltage is user-adjustable around 50% (bidirectional) of the supply voltage, V_{CC}. The device sensitivity is adjustable within the range of 0.6 to 14 mV/G.

The A1365 incorporates a highly sensitive Hall element with a BiCMOS interface integrated circuit that employs temperature-compensation circuitry to reduce the intrinsic sensitivity and offset drift of the Hall element. The IC also includes a small-signal high-gain amplifier, a clamped low-impedance output stage, and a proprietary high-bandwidth dynamic offset cancellation technique.

Device specifications apply across an extended ambient temperature range: –40°C to 150°C. The A1365 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single inline package, suffix KT) that is lead (Pb) free, with 100% matte-tin leadframe plating. The thin package allows for better magnetic coupling because the smaller the air gap in the core is, the higher the coupling from current to magnetic field will be.

Table of Contents

SELECTION GUIDE

Part Number [1]	Leadform	Package	Packing [2]	Sensitivity Range [3] (mV/G)
A1365LKTTN-1-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	0.6 to 1.3
A1365LKTTN-2-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	1.3 to 2.9
A1365LKTTN-5-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	2.9 to 6.4
A1365LKTTN-10-T	TN (Straight)	4-pin SIP	4000 pieces per 13-inch reel	6.4 to 14

[1] TH package leadform options available.
[2] Contact Allegro for additional packing options.
[3] Allegro recommends against changing Coarse Sensitivity settings when programming devices that will be used in production. Each A1365 has been factory temperature compensated at a specific sensitivity range, and changing the coarse bits setting could cause sensitivity drift through temperature range (ΔSens_{TC}) to exceed specified limits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

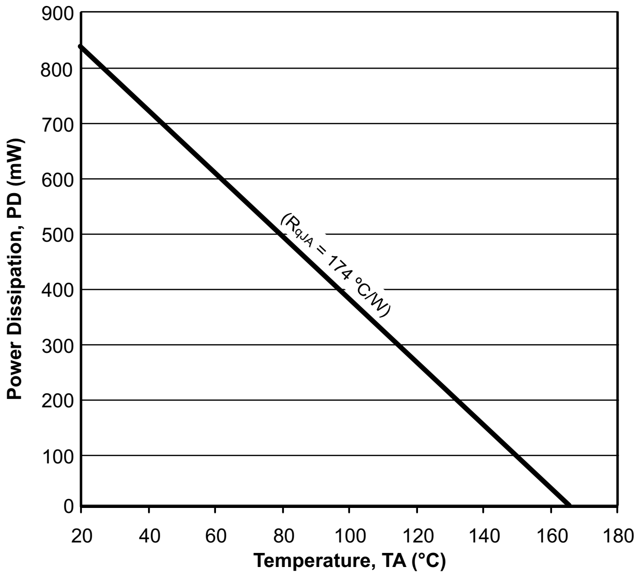
Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6	V
Reverse Supply Voltage	V_{RCC}		–0.1	V
Forward Output Voltage	V_{OUT}		25	V
Reverse Output Voltage	V_{ROUT}		–0.1	V
Forward Fault Voltage	$V_{\overline{FAULT}}$		6	V
Reverse Fault Voltage	$V_{R\overline{FAULT}}$		–0.1	V
Output Source Current	$I_{OUT(source)}$	VOUT to GND	2.8	mA
Output Sink Current	$I_{OUT(sink)}$	VCC to VOUT	10	mA
Maximum Number of EEPROM Write Cycles	$EEPROM_{w(max)}$		100	cycles
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	T_J(max)		165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

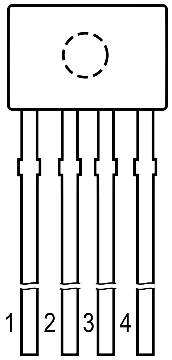
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 1-layer PCB with exposed copper limited to solder pads	174	°C/W

*Additional thermal information available on the Allegro website

Power Dissipation versus Ambient Temperature



PINOUT DIAGRAM AND TERMINAL LIST TABLE



KT Package Pinout Diagram

(Ejector pin mark on opposite side)

Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply, use bypass capacitor to connect to ground; also used for programming
2	VOUT	Output Signal, also used for programming
3	$\overline{\text{FAULT}}$	Over Field Fault Detection Flag
4	GND	Ground

OPERATING CHARACTERISTICS: Valid through the full operating temperature range T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT, $\overline{\text{FAULT}}$ pin in high-impedance state, connected through a 10 kΩ resistor to VCC	–	10	15	mA
Power-On Time [2]	t_{PO}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	100	–	µs
Temperature Compensation Power-On Time [2]	t_{TC}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	90	–	µs
Undervoltage Lockout (UVLO) Threshold [2]	V_{UVLOH}	V_{CC} rising and device function enabled	–	4	4.3	V
	V_{UVLOL}	V_{CC} falling and device function disabled	3.05	3.2	–	V
UVLO Enable/Disable Delay Time [2]	t_{UVLOE}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF, V_{CC} fall time (5 V to 3 V) = 1.5 µs	–	67	–	µs
	t_{UVLOD}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF, V_{CC} recover time (3 V to 5 V) = 1.5 µs	–	6	–	µs
Power-On Reset Voltage [2]	V_{PORH}	T_A = 25°C, V_{CC} rising	–	2.9	–	V
	V_{PORL}	T_A = 25°C, V_{CC} falling	–	2.5	–	V
Power-On Reset Release Time [2]	t_{PORR}	T_A = 25°C, V_{CC} rising	–	85	–	µs
Supply Zener Clamp Voltage	V_z	T_A = 25°C, I_{CC} = 30 mA	6.5	7.5	–	V
Internal Bandwidth	BW_i	Small signal –3 dB, C_L = 1 nF, T_A = 25°C	–	120	–	kHz
Chopping Frequency [3]	f_C	T_A = 25°C	–	500	–	kHz
V_{OUT} CHARACTERISTICS						
Propagation Delay Time [2]	t_{pd}	T_A = 25°C, step magnetic field of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	2.2	–	µs
Rise Time [2]	t_r	T_A = 25°C, step magnetic field of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	3.6	–	µs
Response Time [2]	$t_{RESPONSE}$	T_A = 25°C, step magnetic field of 400 G, C_L = 1 nF, Sens = 2 mV/G	–	3.7	–	µs
Delay to Clamp [2][4]	t_{CLP}	T_A = 25°C, step magnetic field from 160 to 240 G, C_L = 1 nF, Sens = 10 mV/G	–	10	–	µs
Output Voltage Clamp [5]	$V_{CLP(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.55	–	4.85	V
	$V_{CLP(LOW)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	0.15	–	0.45	V
Output Saturation Voltage [2]	$V_{SAT(HIGH)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	4.8	–	–	V
	$V_{SAT(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to VCC	–	–	300	mV
Broken Wire Voltage [2]	$V_{BRK(HIGH)}$	T_A = 25°C, $R_{L(PULLUP)}$ = 10 kΩ to VCC	–	V_{CC}	–	V
	$V_{BRK(LOW)}$	T_A = 25°C, $R_{L(PULLDWN)}$ = 10 kΩ to GND	–	200	–	mV
Noise [6]	V_N	T_A = 25°C, CL = 1 nF	–	1.1	–	mG/√(Hz)
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, bandwidth = BW_i	–	6.3	–	mV_{p-p}
		T_A = 25°C, CL = 1 nF, Sens = 2 mV/G, bandwidth = BW_i	–	1	–	mV_{RMS}

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OPERATING CHARACTERISTICS (continued): Valid through the full operating temperature range T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
V_{OUT} CHARACTERISTICS (continued)						
DC Output Resistance	R_{OUT}	T_A = 25°C	–	< 10	–	Ω
Output Load Resistance	$R_{L(PULLUP)}$	VOUT to VCC	4.7	–	–	kΩ
	$R_{L(PULLDWN)}$	VOUT to GND	4.7	–	–	kΩ
Output Load Capacitance [7]	C_L	VOUT to GND	–	1	10	nF
Output Slew Rate [8]	SR	Sens = 2 mV/G, C_L = 1 nF, T_A = 25°C; step magnetic field of 400 G	–	230	–	V/ms
OVER FIELD FAULT CHARACTERISTICS						
Fault Switch Point Programming Bits	FAULT_ THRESH		–	6	–	bit
Positive Field Fault Switch Point Range [9]	V_{FPSP}	T_A = 25°C, programmable using FAULT_THRESH bits	0.72 × V_{CC}	–	0.88 × V_{CC}	V
Negative Field Fault Switch Point Range [9]	V_{FNSP}	T_A = 25°C, programmable using FAULT_THRESH bits	0.12 × V_{CC}	–	0.28 × V_{CC}	V
Fault Switch Point Step Size	$Step_{FAULT}$	T_A = 25°C, Average Fault Switch Point step size, V_{CC} = 5 V	–	16	–	mV
Fault Hysteresis Programming Bits	FAULT_HYST		–	2	–	bit
Fault Hysteresis Level Range [9]	V_{FHYST}	T_A = 25°C, FAULT_HYST = 0 (decimal), FAULT_THRESH = 0, no hysteresis	–	0	–	mV
		T_A = 25°C, FAULT_HYST = 1 (decimal), FAULT_THRESH = 0, V_{CC} = 5 V	–	30	–	mV
		T_A = 25°C, FAULT_HYST = 2 (decimal), FAULT_THRESH = 0, V_{CC} = 5 V	–	60	–	mV
		T_A = 25°C, FAULT_HYST = 3 (decimal), FAULT_THRESH = 0, maximum hysteresis value, V_{CC} = 5 V	–	120	–	mV
Enable Latched Fault Bit	FAULT_ LATCH		–	1	–	bit
DC Fault Switch Point Error	Err_{DFS}	FAULT_THRESH = 0 (decimal), $R_{F(PULLUP)}$ = 10 kΩ from $\overline{\text{FAULT}}$ to VCC; measured under DC conditions, V_{FHYST} = 60 mV	–	±40	–	mV
DC Fault Switch Point Symmetry Error	Err_{DFSS}	FAULT_THRESH = 0 (decimal), $R_{F(PULLUP)}$ = 10 kΩ from $\overline{\text{FAULT}}$ to VCC; measured under DC conditions, V_{FHYST} = 60 mV	–	±60	–	mV
$\overline{\text{FAULT}}$ Pin Low Output Voltage	$V_{\overline{FAULT}L}$	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{\text{FAULT}}$ to VCC	–	–	0.3	V
Transient Fault Response Time [10]	t_{TFR}	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{\text{FAULT}}$ to VCC, C_F = Open, FAULT_THRESH = 0, VOUT step from $V_{OUT(Q)}$ to V_{OUT} = 1.3 × (V_{FPSP} – $V_{OUT(Q)}$) + $V_{OUT(Q)}$	–	4.5	–	µs
Transient Fault Release Time	t_{TFRL}	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{\text{FAULT}}$ to VCC, C_F = Open, FAULT_THRESH = 0, V_{FHYST} = 0 mV, VOUT step from VOUT = 1.1 × (V_{FPSP} – $V_{OUT(Q)}$) + $V_{OUT(Q)}$	–	2.5	–	µs

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OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
FAULT CHARACTERISTICS (continued)						
Fault Delay Due to Load Capacitance	t_{FDC}	$R_{F(PULLUP)}$ = 10 kΩ from $\overline{\text{FAULT}}$ to VCC	–	0.5	–	µs/nF
External Pull-Up Supply Voltage	$V_{F(PULLUP)}$		1.65	V_{CC}	V_{CC}	V
External $\overline{\text{FAULT}}$ Pull-Up Resistor	$R_{F(PULLUP)}$		4.7	–	–	kΩ
External $\overline{\text{FAULT}}$ Capacitance	C_F		–	–	10	nF
Internal $\overline{\text{FAULT}}$ Pull-Up Resistor	$R_{IF(PULLUP)}$		–	10	–	kΩ
Internal $\overline{\text{FAULT}}$ Pull-Up Current	$I_{IF(PULLUP)}$		–	40	–	µA
QUIESCENT VOLTAGE OUTPUT ($V_{OUT(Q)}$) [2]						
Initial Unprogrammed Quiescent Voltage Output [2][11]	$V_{OUT(Q)init}$	T_A = 25°C	2.4	2.5	2.6	V
Quiescent Voltage Output Programming Range [2][5][12]	$V_{OUT(Q)PR}$	T_A = 25°C	2.3	–	2.7	V
Quiescent Voltage Output Programming Bits [13]	QVO		–	9	–	bit
Average Quiescent Voltage Output Programming Step Size [2][14][15]	$Step_{VOUT(Q)}$	T_A = 25°C	1.9	2.3	2.8	mV
Quiescent Voltage Output Programming Resolution [2][16]	$Err_{PGVOUT(Q)}$	T_A = 25°C	–	±0.5 × $Step_{VOUT(Q)}$	–	mV
SENSITIVITY (Sens) [2]						
Initial Unprogrammed Sensitivity [11]	$Sens_{init}$	SENS_COARSE = 00, T_A = 25°C	–	1	–	mV/G
		SENS_COARSE = 01, T_A = 25°C	–	2.2	–	mV/G
		SENS_COARSE = 10, T_A = 25°C	–	4.7	–	mV/G
		SENS_COARSE = 11, T_A = 25°C	–	9.6	–	mV/G
Sensitivity Programming Range [5][12]	$Sens_{PR}$	SENS_COARSE = 00, T_A = 25°C	0.6	–	1.3	mV/G
		SENS_COARSE = 01, T_A = 25°C	1.3	–	2.9	mV/G
		SENS_COARSE = 10, T_A = 25°C	2.9	–	6.4	mV/G
		SENS_COARSE = 11, T_A = 25°C	6.4	–	14	mV/G
Coarse Sensitivity Programming Bits [17]	SENS_ COARSE		–	2	–	bit
Fine Sensitivity Programming Bits [13]	SENS_FINE		–	9	–	bit
Average Fine Sensitivity and Temperature Compensation Programming Step Size [2][14][15]	$Step_{SENS}$	SENS_COARSE = 00, T_A = 25°C	2.4	3.2	4.1	µV/G
		SENS_COARSE = 01, T_A = 25°C	5	6.6	8.5	µV/G
		SENS_COARSE = 10, T_A = 25°C	11	14.2	18	µV/G
		SENS_COARSE = 11, T_A = 25°C	22	29	38	µV/G
Sensitivity Programming Resolution [2][16]	Err_{PGSENS}	T_A = 25°C	–	±0.5 × $Step_{SENS}$	–	µV/G
FACTORY-PROGRAMMED SENSITIVITY TEMPERATURE COEFFICIENT						
Sensitivity Temperature Coefficient [2]	TC_{SENS}	T_A=150°C, T_A= –40°C, calculated relative to 25°C	–	0	–	%/°C
Sensitivity Drift Through Temperature Range [2][12][18][23]	$\Delta Sens_{TC}$	T_A = 25°C to 150°C	–2.5	–	2.5	%
		T_A = –40°C to 25°C	–3	–	3	%

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OPERATING CHARACTERISTICS (continued): valid through the full operating temperature range, T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
FACTORY-PROGRAMMED QUIESCENT VOLTAGE OUTPUT TEMPERATURE COEFFICIENT						
Quiescent Voltage Output Temperature Coefficient [2]	TC_{QVO}	T_A = 150°C, T_A = –40°C, calculated relative to 25°C	–	0	–	mV/°C
Quiescent Voltage Output Drift Through Temperature Range [2][12][18]	$\Delta V_{OUT(Q)TC}$	SENS_COARSE = 00, SENS_COARSE = 01, or SENS_COARSE = 10, T_A = 25°C to 150°C	–10	–	10	mV
		SENS_COARSE = 11, T_A = 25°C to 150°C	–15	–	15	mV
		T_A = –40°C to 25°C	–30	–	30	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$Step_{QVOTC}$		–	2.3	–	mV
LOCK BIT PROGRAMMING						
EEPROM Lock Bit	EELOCK		–	1	–	bit
ERROR COMPONENTS						
Linearity Sensitivity Error [2][19]	Lin_{ERR}		–1	< ±0.25	1	%
Symmetry Sensitivity Error [2]	Sym_{ERR}		–0.5	< ±0.25	0.5	%
Ratiometry Quiescent Voltage Output Error [2][20]	$Rat_{ERRVOUT(Q)}$	Relative to V_{CC} = 5 V ±5%	–0.3	0	0.3	%
Ratiometry Sensitivity Error [2][20]	$Rat_{ERRSens}$	Relative to V_{CC} = 5 V ±5%	–1	< ±0.5	1	%
Ratiometry Clamp Error [2][21]	Rat_{ERRCLP}	T_A = 25°C, Relative to V_{CC} = 5 V ±5%	–	< ±1	–	%
Sensitivity Drift Due to Package Hysteresis [2]	$\Delta Sens_{PKG}$	T_A = 25°C, after temperature cycling, 25°C to 150°C and back to 25°C	–	-1.25 ±1.25	–	%
Sensitivity Drift Over Lifetime [22]	$\Delta Sens_{LIFE}$	T_A = 25°C, shift after AEC Q100 grade 0 qualification testing	–	±1%	–	%

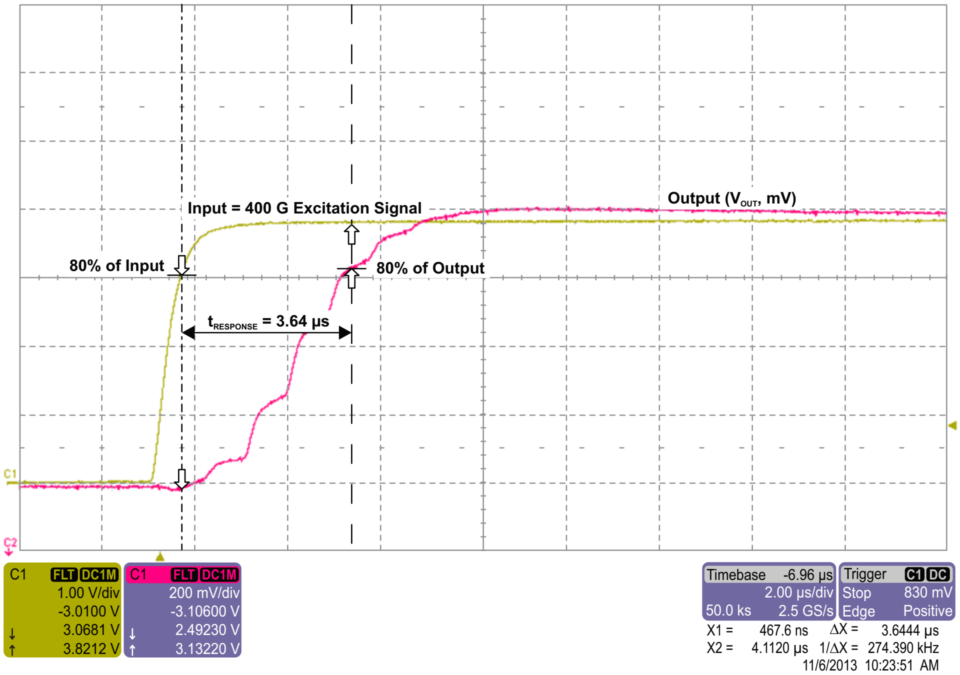
[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] See Characteristic Definitions section.
[3] f_C varies up to approximately ±5% over the full operating ambient temperature range, T_A.
[4] If the programmed Fault Switch Point exceeds the clamp voltage, Fault operation will have priority over clamp operation.
[5] Sens, $V_{OUT(Q)}$, $V_{CLP(LOW)}$, and $V_{CLP(HIGH)}$ scale with V_{CC} due to ratiometry.
[6] Noise, measured in mV_{PP} and in mV_{RMS}, is dependent on the sensitivity of the device.
[7] Output stability is maintained for capacitive loads as large as 10 nF.
[8] High-to-low transition of output voltage is a function of external load components and device sensitivity.
[9] Fault Switch Point and Fault Hysteresis are ratiometric.
[10] Refer to Fault Characteristics section for the impact of load circuit and different Fault switch Point settings on Transient Fault Response Time.
[11] Raw device characteristic values before any programming.
[12] Exceeding the specified ranges will cause sensitivity and Quiescent Voltage Output drift through the temperature range to deteriorate beyond the specified values.
[13] Refer to Functional Description section.
[14] Step size is larger than required, in order to provide for manufacturing spread. See Characteristic Definitions section.
[15] Non-ideal behavior in the programming DAC can cause the step size at each significant bit rollover code to be greater than twice the maximum specified value of $Step_{VOUT(Q)}$ or $Step_{SENS}$.
[16] Overall programming value accuracy. See Characteristic Definitions section.
[17] Each A1365 part number is factory-programmed and temperature compensated at a different coarse sensitivity setting. Changing coarse bits setting could cause sensitivity drift through temperature range ,$\Delta Sens_{TC}$, to exceed specified limits.
[18] Allegro will be testing and temperature compensating each device at 150°C. Allegro will not be testing devices at –40°C. Temperature compensation codes will be applied based on characterization data.
[19] Linearity applies to output voltage ranges of ±2 V from the quiescent output for bidirectional devices.
[20] Percent change from actual value at V_{CC} = 5 V, for a given temperature, through the supply voltage operating range.
[21] Percent change from actual value at V_{CC} = 5 V, T_A = 25°C, through the supply voltage operating range.
[22] Based on characterization data obtained during standardized stress test for Qualification of Integrated Circuits. Cannot be guaranteed. Drift is a function of customer application conditions. Contact Allegro MicroSystems for further information.
[23] Includes sensitivity drift due to package hysteresis after exposing the sensor to a temperature of 150°C for 60 seconds during test.

CHARACTERISTIC PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

400 G Excitation Signal with 10% to 90% rise time = 1 μs

Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 μF, C_L = 1 nF



C1 FLT DC1M
1.00 V/div
-3.0100 V
↓ 3.0681 V
↑ 3.8212 V

C1 FLT DC1M
200 mV/div
-3.10600 V
↓ 2.49230 V
↑ 3.13220 V

Timebase -6.96 μs
2.00 μs/div
50.0 ks 2.5 GS/s

Trigger C1 DC
Stop 830 mV
Edge Positive

X1 = 467.6 ns ΔX = 3.6444 μs
X2 = 4.1120 μs 1/ΔX = 274.390 kHz
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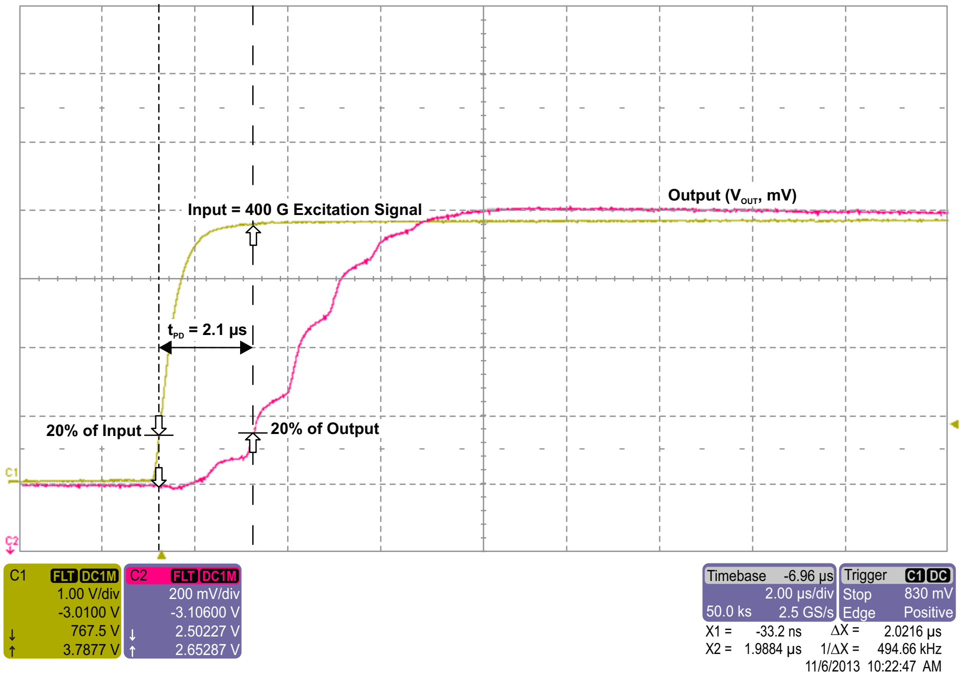
Propagation Delay (t_{PD})

400 G Excitation Signal with 10% to 90% rise time = 1 μs

Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 μF, C_L = 1 nF



C1 FLT DC1M
1.00 V/div
-3.0100 V
↓ 767.5 V
↑ 3.7877 V

C2 FLT DC1M
200 mV/div
-3.10600 V
↓ 2.50227 V
↑ 2.65287 V

Timebase -6.96 μs
2.00 μs/div
50.0 ks 2.5 GS/s

Trigger C1 DC
Stop 830 mV
Edge Positive

X1 = -33.2 ns ΔX = 2.0216 μs
X2 = 1.9884 μs 1/ΔX = 494.66 kHz
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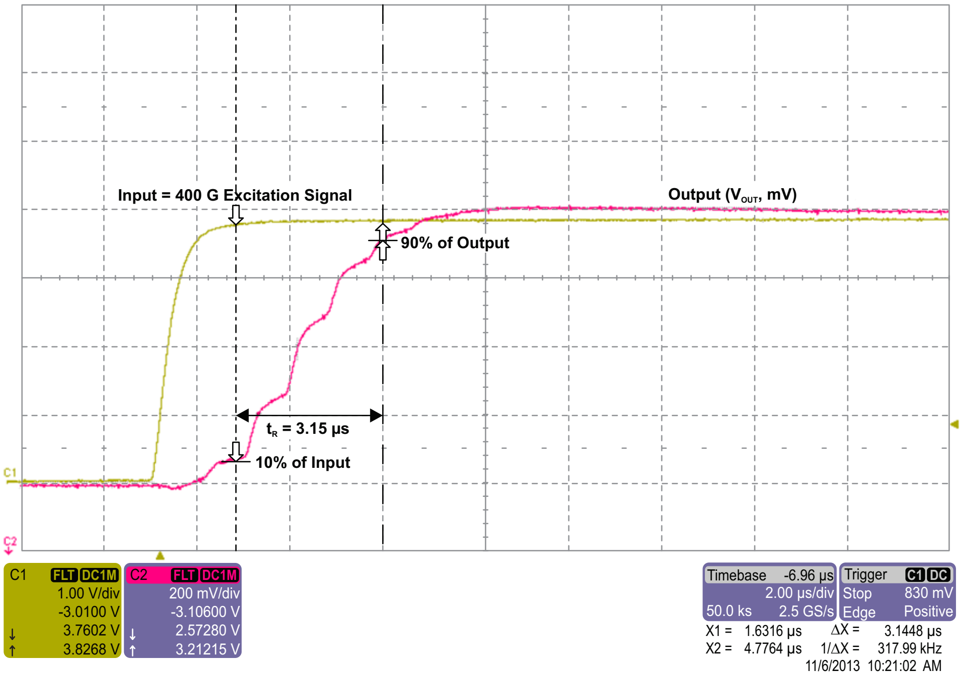
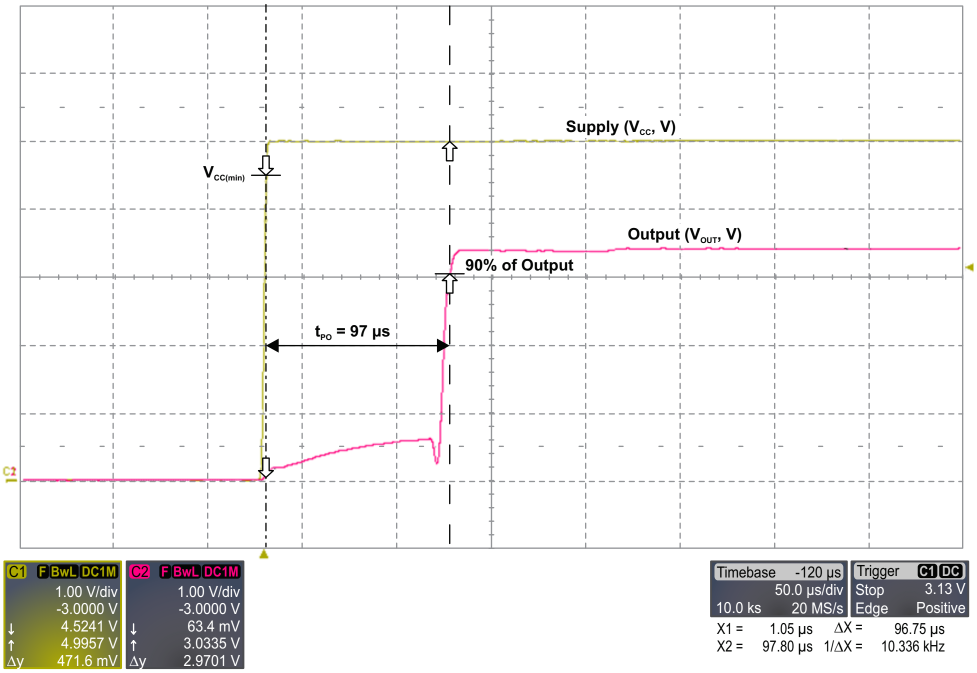
Rise Time (t_r)

400 G Excitation Signal with 10% to 90% rise time = 1 µs
Sensitivity = 2 mV/G, C_{BYPASS} = 0.1 µF, C_L = 1 nF



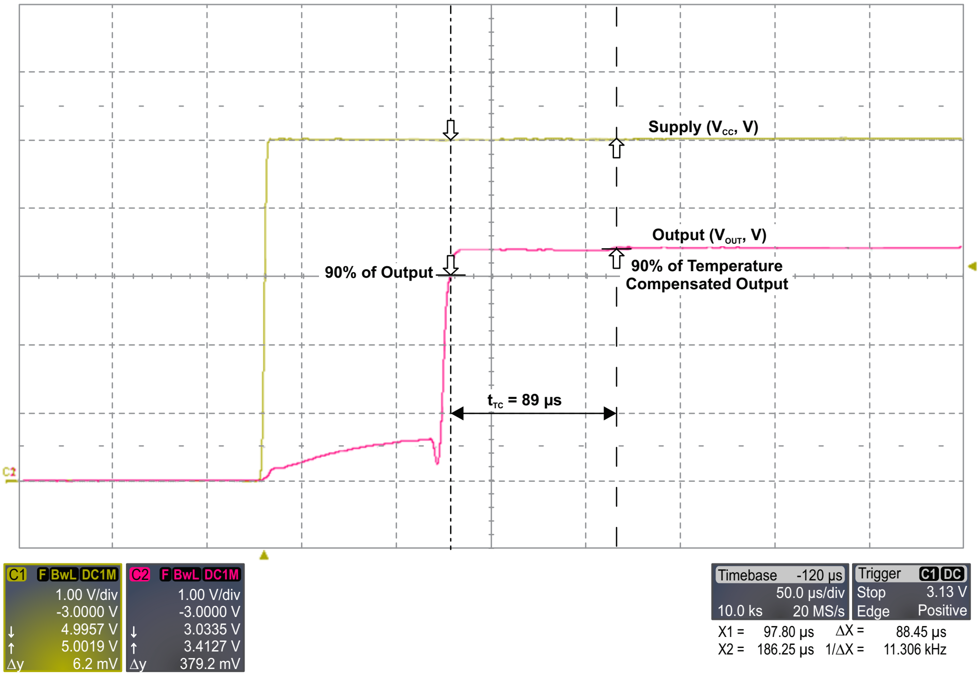
Power-On Time (t_{PO})

400 G Constant Excitation Signal with V_{CC} 10% to 90% rise time = 1 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



Temperature Compensation Power-On Time (t_{TC})

400G Constant Excitation Signal, with V_{CC} 10% to 90% rise time = 1.5 µs
Sensitivity = 2mV/G, C_{BYPASS} = Open, C_L = 1 nF



C1 F BwL DC1M
1.00 V/div
-3.0000 V
↓ 4.9957 V
↑ 5.0019 V
Δy 6.2 mV

C2 F BwL DC1M
1.00 V/div
-3.0000 V
↓ 3.0335 V
↑ 3.4127 V
Δy 379.2 mV

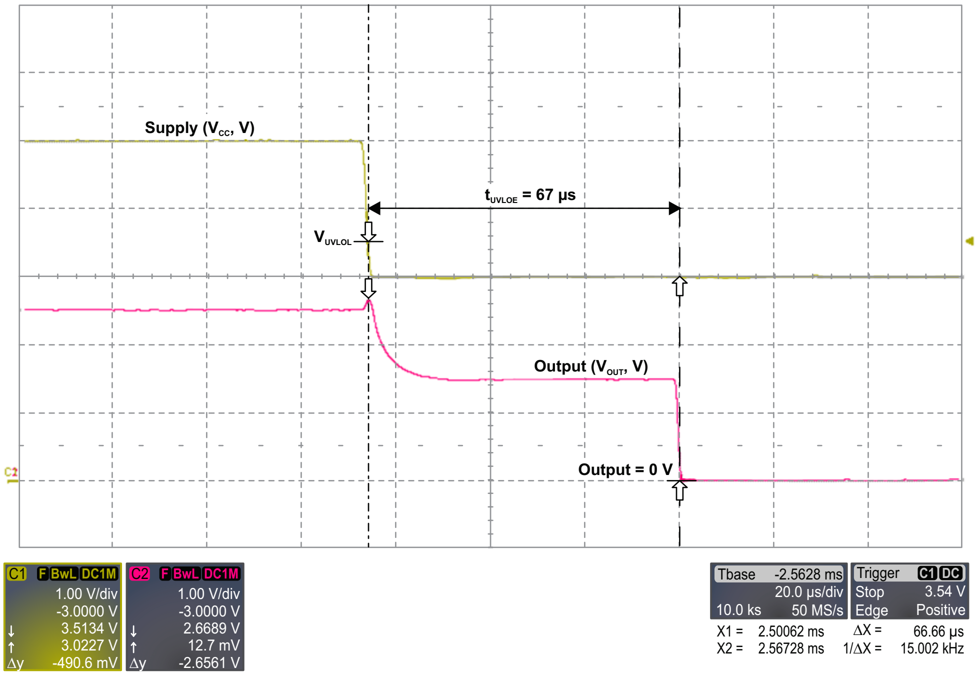
Timebase -120 µs
50.0 µs/div
10.0 ks 20 MS/s

Trigger C1 DC
Stop 3.13 V
Edge Positive

X1 = 97.80 µs ΔX = 88.45 µs
X2 = 186.25 µs 1/ΔX = 11.306 kHz

UVLO Enable Time (t_{UVLOE})

V_{CC} 5 V to 3 V fall time = 1.5 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



C1 F BwL DC1M
1.00 V/div
-3.0000 V
↓ 3.5134 V
↑ 3.0227 V
Δy -490.6 mV

C2 F BwL DC1M
1.00 V/div
-3.0000 V
↓ 2.6689 V
↑ 12.7 mV
Δy -2.6561 V

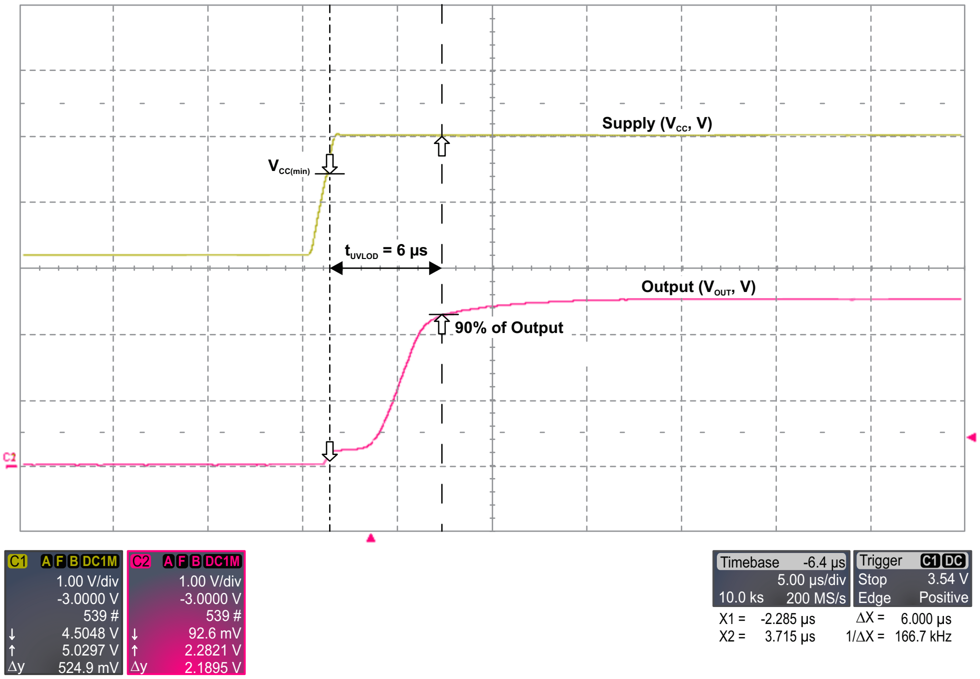
Tbase -2.5628 ms
20.0 µs/div
10.0 ks 50 MS/s

Trigger C1 DC
Stop 3.54 V
Edge Positive

X1 = 2.50062 ms ΔX = 66.66 µs
X2 = 2.56728 ms 1/ΔX = 15.002 kHz

UVLO Disable Time (t_{UVLOD})

V_{CC} 3.2 V to 5 V Recovery Time = 1.5 µs
Sensitivity = 2 mV/G, C_{BYPASS} = Open, C_L = 1 nF



CHARACTERISTIC DEFINITIONS

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time (t_{PO}) is defined as: the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 1.

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time (t_{PO}) elapses, t_{TC} is also required before a valid temperature compensated output.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 2).

Rise Time (t_r)

The time interval between a) when the sensor IC reaches 10% of its final value, and b) when it reaches 90% of its final value (see Figure 2). Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied magnetic field (see Figure 3).

Delay to Clamp (t_{CLP})

A large magnetic input step may cause the clamp to overshoot its steady-state value. The Delay to Clamp (t_{CLP}) is defined as: the time it takes for the output voltage to settle within steady-state clamp voltage ±1% of Clamp Voltage Dynamic Range, after initially passing through its steady-state voltage, as shown in Figure 4. Clamp Voltage Dynamic Range is defined as $V_{CLP(HIGH)(min)} – V_{CLP(LOW)(max)}$.

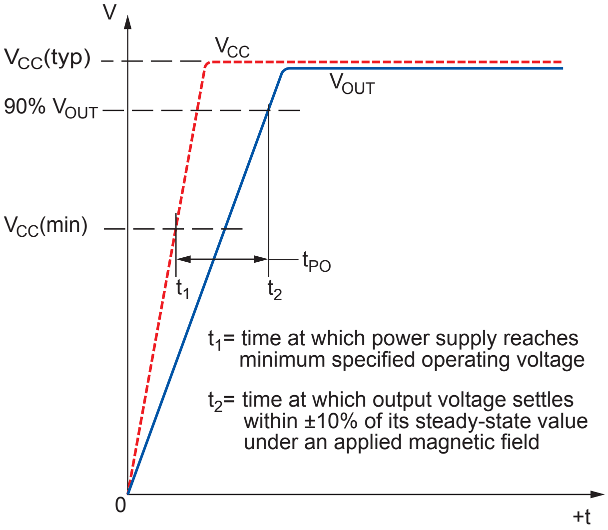


Figure 1: Power-On Time Definition

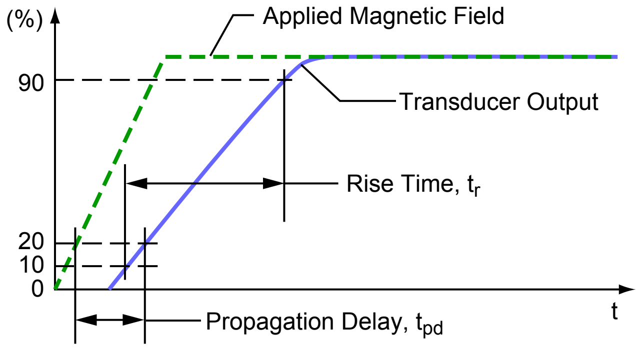


Figure 2: Propagation Delay and Rise Time Definitions

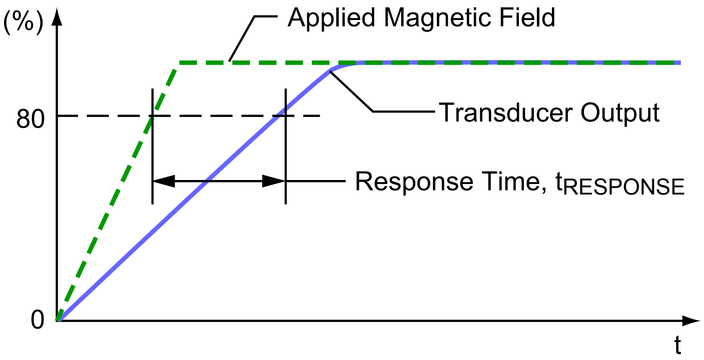


Figure 3: Response Time Definition

Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(Q)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A).

Initial Unprogrammed Quiescent Voltage Output ($V_{OUT(Q)init}$)

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of $V_{CC}/2$, as shown in Figure 5.

Quiescent Voltage Output Programming Range ($V_{OUT(Q)PR}$)

The Quiescent Voltage Output ($V_{OUT(Q)}$) can be programmed within the Quiescent Voltage Output Range limits: $V_{OUT(Q)PR(min)}$ and $V_{OUT(Q)PR(max)}$. Exceeding the specified Quiescent Voltage Output Range will cause Quiescent Voltage Output Drift Through Temperature Range $\Delta V_{OUT(Q)TC}$ to deteriorate beyond the specified values, as shown in Figure 5.

Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$)

The Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$) is determined using the following calculation:

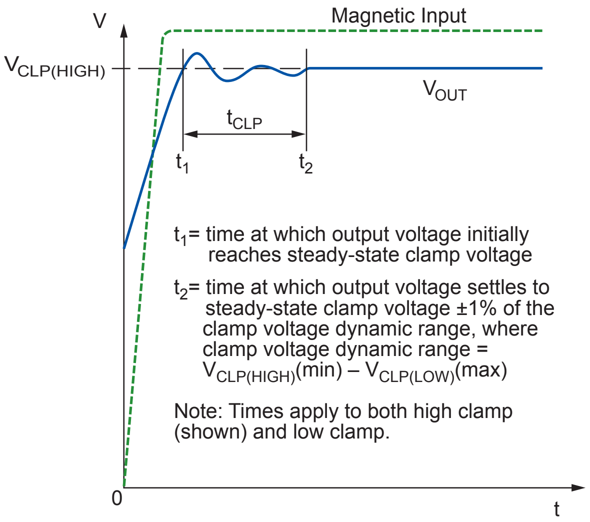


Figure 4: Delay to Clamp Definition

$$Step_{VOUT(Q)} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1} , \qquad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution ($Err_{PGVOUT(Q)}$)

The programming resolution for any device is half of its programming step size. Therefore, the typical programming resolution will be:

$$Err_{PGVOUT(Q)}(typ) = 0.5 \times Step_{VOUT(Q)}(typ) \qquad (2)$$

Quiescent Voltage Output Temperature Coefficient (TC_{QVO})

Device $V_{OUT(Q)}$ changes as temperature changes, with respect to its programmed Quiescent Voltage Output Temperature Coefficient, TC_{QVO}. TC_{QVO} is programmed at 150°C and is calculated relative to the nominal $V_{OUT(Q)}$ programming temperature of 25°C. TC_{QVO} (mV/°C) is defined as:

$$TC_{QVO} = [V_{OUT(Q)T2} - V_{OUT(Q)T1}][1/(T2 - T1)] \qquad (3)$$

where T1 is the nominal $V_{OUT(Q)}$ programming temperature of 25°C, and T2 is the TC_{QVO} programming temperature of 150°C. The expected $V_{OUT(Q)}$ through the full ambient temperature range ($V_{OUT(Q)EXPECTED(TA)}$) is defined as:

$$V_{OUT(Q)EXPECTED}(T_A) = V_{OUT(Q)T1} + TC_{QVO}(T_A - T1) \qquad (4)$$

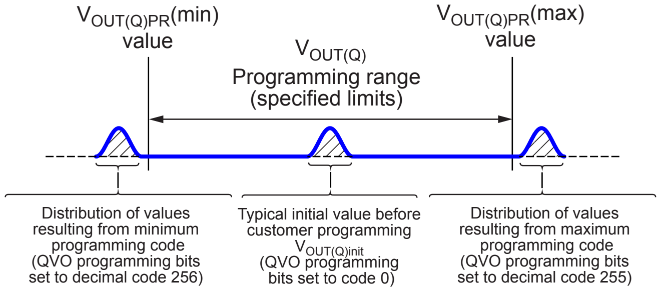


Figure 5: Quiescent Voltage Output Range Definition

$V_{OUT(Q)EXPECTED(TA)}$ should be calculated using the actual measured values of $V_{OUT(Q)T1}$ and TC_{QVO} rather than programming target values.

Quiescent Voltage Output Drift Through Temperature Range ($\Delta V_{OUT(Q)TC}$)

Due to internal component tolerances and thermal considerations, the Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The Quiescent Voltage Output Drift Through Temperature Range ($\Delta_{VOUT(Q)TC}$) is defined as:

$$D_{VOUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)EXPECTED(TA)} \qquad (5)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the actual measured values of $\Delta V_{OUT(Q)(TA)}$ and $\Delta V_{OUT(Q)EXPECTED(TA)}$ rather than programming target values.

Sensitivity (Sens)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}\ , \qquad (6)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

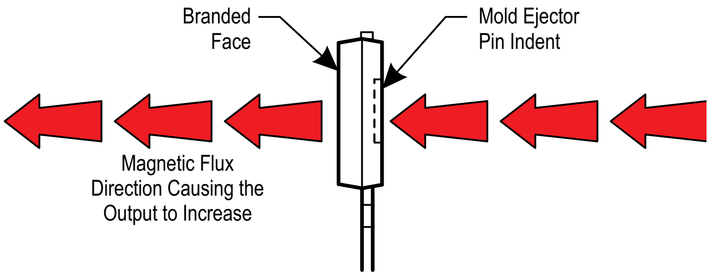


Figure 6: Magnetic Flux Polarity

Initial Unprogrammed Sensitivity ($Sens_{init}$)

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each A1365 variant has a different SENS_COARSE setting.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified Sensitivity Range will cause Sensitivity Drift Through Temperature Range $\Delta Sens_{TC}$ to deteriorate beyond the specified values. Refer to the Quiescent Voltage Output Range section for a conceptual explanation of how value distributions and ranges are related.

Average Fine Sensitivity Programming Step Size ($Step_{SENS}$)

Refer to the Average Quiescent Voltage Output Programming Step Size section for a conceptual explanation.

Sensitivity Programming Resolution (Err_{PGSENS})

Refer to the Quiescent Voltage Output Programming Resolution section for a conceptual explanation.

Sensitivity Temperature Coefficient (TC_{SENS})

Device sensitivity changes as temperature changes, with respect to its programmed sensitivity temperature coefficient, TC_{SENS}. TC_{SENS} is programmed at 150°C, and calculated relative to the nominal sensitivity programming temperature of 25°C. TC_{SENS} (%/°C) is defined as:

$$TC_{SENS} = \left(\frac{Sens_{T2} - Sens_{T1}}{Sens_{T1}} \times 100\% \right) \left(\frac{1}{T2 - T1} \right), \qquad (7)$$

where T1 is the nominal Sens programming temperature of 25°C, and T2 is the TC_{SENS} programming temperature of 150°C. The expected value of Sens over the full ambient temperature range, $Sens_{EXPECTED(TA)}$, is defined as:

$$Sens_{EXPECTED(TA)} = Sens_{T1} \times \left[100\% + \frac{TC_{SENS}\ (T_A - T1)}{100} \right] \qquad (8)$$

$Sens_{EXPECTED(TA)}$ should be calculated using the actual measured values of $Sens_{T1}$ rather than programming target values.

Sensitivity Drift Through Temperature Range ($\Delta \mathrm{Sens}_{TC}$)

Second-order-sensitivity temperature-coefficient effects cause the magnetic sensitivity, Sens, to drift from its expected value over the operating ambient temperature range (T_A). The Sensitivity Drift Through Temperature Range ($\Delta \mathrm{Sens}_{TC}$) is defined as:

$$\Delta \mathrm{Sens}_{TC} = \frac{\mathrm{Sens}_{TA} - \mathrm{Sens}_{EXPECTED(TA)}}{\mathrm{Sens}_{EXPECTED(TA)}} \times 100\% \quad . \qquad (9)$$

Sensitivity Drift Due to Package Hysteresis ($\Delta \mathrm{Sens}_{PKG}$)

Package stress and relaxation can cause the device sensitivity at $T_A = 25°C$ to change during and after temperature cycling. The sensitivity drift due to package hysteresis ($\Delta \mathrm{Sens}_{PKG}$) is defined as:

$$\Delta \mathrm{Sens}_{PKG} = \frac{\mathrm{Sens}_{(25°C)2} - \mathrm{Sens}_{(25°C)1}}{\mathrm{Sens}_{(25°C)1}} \times 100\% \quad , \qquad (10)$$

where $\mathrm{Sens}_{(25°C)1}$ is the programmed value of sensitivity at $T_A = 25°C$, and $\mathrm{Sens}_{(25°C)2}$ is the value of sensitivity at $T_A = 25°C$, after temperature cycling T_A up to 150°C and back to 25°C.

Linearity Sensitivity Error (Lin_{ERR})

The A1365 is designed to provide a linear output in response to a ramping applied magnetic field. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error

Linearity error is calculated separately for the positive (Lin_{ERRPOS}) and negative (Lin_{ERRNEG}) applied magnetic fields. Linearity Error (%) is measured and defined as:

$$\mathrm{Lin}_{ERRPOS} = \left(1 - \frac{\mathrm{Sens}_{BPOS2}}{\mathrm{Sens}_{BPOS1}}\right) \times 100\% \quad ,$$

$$\mathrm{Lin}_{ERRNEG} = \left(1 - \frac{\mathrm{Sens}_{BNEG2}}{\mathrm{Sens}_{BNEG1}}\right) \times 100\% \quad , \qquad (11)$$

where:

$$\mathrm{Sens}_{Bx} = \frac{|V_{OUT(Bx)} - V_{OUT(Q)}|}{B_x} \quad , \qquad (12)$$

and BPOSx and BNEGx are positive and negative magnetic fields, with respect to the quiescent voltage output such that |BPOS2| = 2 × |BPOS1| and |BNEG2| = 2 × |BNEG1|.

Then:

$$\mathrm{Lin}_{ERR} = \max(\mathrm{Lin}_{ERRPOS}, \mathrm{Lin}_{ERRNEG}) \quad . \qquad (13)$$

Symmetry Sensitivity Error (Sym_{ERR})

The magnetic sensitivity of an A1365 device is constant for any two applied magnetic fields of equal magnitude and opposite polarities. Symmetry Error, Sym_{ERR} (%), is measured and defined as:

$$\mathrm{Sym}_{ERR} = \left(1 - \frac{\mathrm{Sens}_{BPOS}}{\mathrm{Sens}_{BNEG}}\right) \times 100\% \quad , \qquad (14)$$

where Sens_{Bx} is as defined in equation 12, and BPOSx and BNEGx are positive and negative magnetic fields such that |BPOSx| = |BNEGx|.

Ratiometry Error (Rat_{ERR})

The A1365 device features ratiometric output. This means that the Quiescent Voltage Output ($V_{OUT(Q)}$) magnetic sensitivity, Sens, and Output Voltage Clamp ($V_{CLP(HIGH)}$ and $V_{CLP(LOW)}$) are proportional to the Supply Voltage (V_{CC}). In other words, when the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The ratiometric error in Quiescent Voltage Output, $\mathrm{Rat}_{ERRVOUT(Q)}$ (%), for a given supply voltage (V_{CC}) is defined as:

$$\mathrm{Rat}_{ERRVOUT(Q)} = \left(1 - \frac{V_{OUT(Q)(VCC)} / V_{OUT(Q)(5V)}}{V_{CC} / 5\ \mathrm{V}}\right) \times 100\% \qquad (15)$$

The ratiometric error in magnetic sensitivity, $\mathrm{Rat}_{ERRSens}$ (%), for a given Supply Voltage (V_{CC}) is defined as:

$$\mathrm{Rat}_{ERRSens} = \left(1 - \frac{\mathrm{Sens}_{(VCC)} / \mathrm{Sens}_{(5V)}}{V_{CC} / 5\ \mathrm{V}}\right) \times 100\% \quad . \qquad (16)$$

The ratiometric error in the clamp voltages, Rat_{ERRCLP} (%), for a given supply voltage (V_{CC}) is defined as:

$$\mathrm{Rat}_{ERRCLP} = \left(1 - \frac{V_{CLP(VCC)} / V_{CLP(5V)}}{V_{CC} / 5\ \mathrm{V}}\right) \times 100\% \;, \qquad (17)$$

where V_{CLP} is either $V_{CLP(HIGH)}$ or $V_{CLP(LOW)}$.

Power-On Reset Voltage (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the A1365 is held in Reset state. The Reset signal is disabled when V_{CC} reaches V_{UVLOH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the Reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to go into a high-impedance state. (Note that a detailed description of POR and UVLO operation can be found in the Functional Description section).

Power-On Reset Release Time (t_{PORR})

When V_{CC} rises to V_{PORH}, the Power-On Reset Counter starts. The A1365 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has exceeded V_{UVLOH}.

Undervoltage Lockout Threshold (V_{UVLO})

If V_{CC} drops below V_{UVLOL}, the output voltage will be pulled to GND. If V_{CC} starts rising, the A1365 will come out of this lock state when V_{CC} reaches V_{UVLOH}.

UVLO Enable/Disable Delay Time (t_{UVLO})

When a falling V_{CC} reaches V_{UVLOL}, time t_{UVLOE} is required to engage the Undervoltage Lockout state. When V_{CC} rises above V_{UVLOH}, time t_{UVLOD} is required to disable UVLO and to have a valid output voltage.

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken wire event), output voltage will go to $V_{BRK(HIGH)}$ if a load resistor is connected to VCC, or to $V_{BRK(LOW)}$ if a load resistor is connected to GND.

DC Fault Switch Point Error (Err_{DFS})

The Over Field Fault Switch Point is user-programmable with a step size of $Step_{FAULT}$. DC Fault Switch Point Error is a deviation from the user-programmed value that occurs over the operating temperature range.

DC Fault Switch Point Symmetry Error (Err_{DFSS})

Writing FLT_THRESH bits sets the DC Fault Switch Point for positive and negative magnetic fields as follows:

Positive Field Fault Switch Point (V_{FPSP}) = Xpos × V_{CC} and Negative Field Fault Switch Point (V_{FNSP}) = Xneg × V_{CC} where Xpos + Xneg = 1. For example, programming $V_{FPSP} = 0.8 \times V_{CC}$ should automatically set $V_{FNSP} = 0.2 \times V_{CC}$. For a measured V_{FPSP} ,the DC Fault Switch Point Symmetry error is the delta between the expected V_{FNSP} and the measured one.

Transient Fault Response Time (t_{TFR})

The time interval between a) when the input crosses the DC Fault Switch Point and b) when the $\overline{\text{FAULT}}$ pin reaches 20% of its final value.

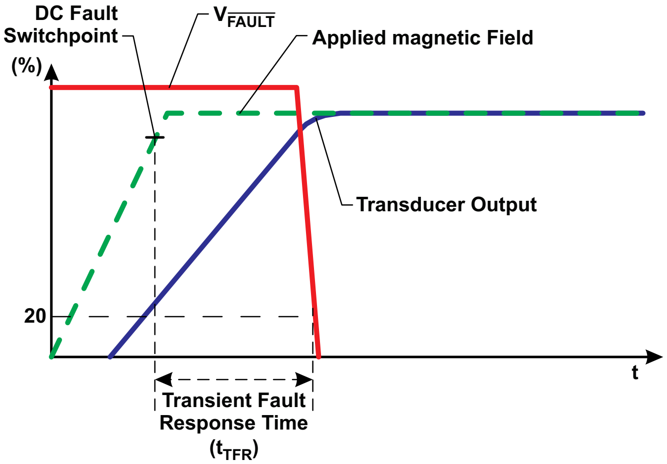


Figure 7: Transient Fault Response Time (t_{TFR})

Transient Fault Release Time (t_{TFRL})

As the Over Field Fault condition goes away, t_{TFRL} is the time interval between a) when the recovering input crosses the DC Fault Switch Point and when the $\overline{\text{FAULT}}$ pin reaches 80% of its final value. Note that the DC Fault Switch Point will be impacted by the programmed Fault Hysteresis Level (V_{FHSYT}).

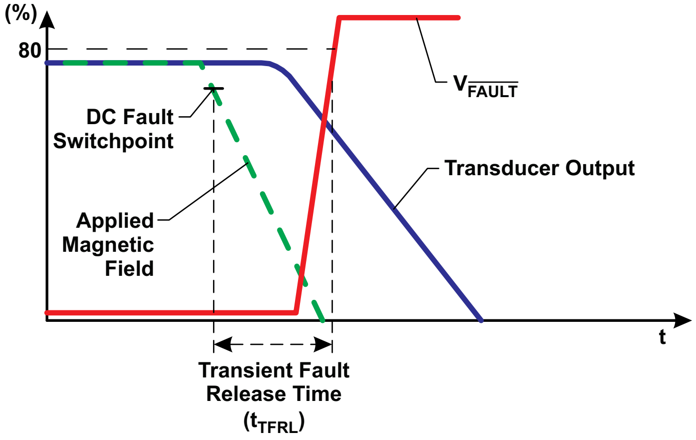


Figure 8: Transient Fault Release Time (t_{TFRL})

FUNCTIONAL DESCRIPTION

Programming Sensitivity and Quiescent Voltage Output

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming SENS_FINE and QVO bits, as illustrated in Figure 9 and Figure 10.

Users should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause the sensitivity and $V_{OUT(Q)}$ drift over the temperature range ($\Delta Sens_{TC}$ and $\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, Allegro recommends programming sensitivity first, then $V_{OUT(Q)}$.

Coarse Sensitivity

Each A1365 variant is programmed to a different coarse sensitivity setting. Devices are tested, and temperature compensation is factory-programmed under that specific coarse sensitivity setting. If the coarse sensitivity setting is changed, by programming SENS_COARSE bits, Allegro cannot guarantee the specified sensitivity drift through temperature range limits ($\Delta Sens_{TC}$).

Memory-Locking Mechanisms

The A1365 is equipped with two distinct memory-locking mechanisms:

- ***Default Lock*** At power-up, all registers of the A1365 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 30-bit customer access code must be written to address 0x24 within Access Code Timeout (t_{ACC} = 8 ms) from power-up. After doing so, registers can be accessed. If VCC is power-cycled, the Default Lock will automatically be re-enabled. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the output pin.
- ***Lock Bit*** After EEPROM has been programmed by the user, the EELOCK bit can be set high and VCC power-cycled to permanently disable the ability to read or write any register. This will prevent the ability to disable Default Lock using the method described above. Note that after the EELOCK bit is set high and the VCC pin is power-cycled, you will not have the ability to clear the EELOCK bit or read/write any register.

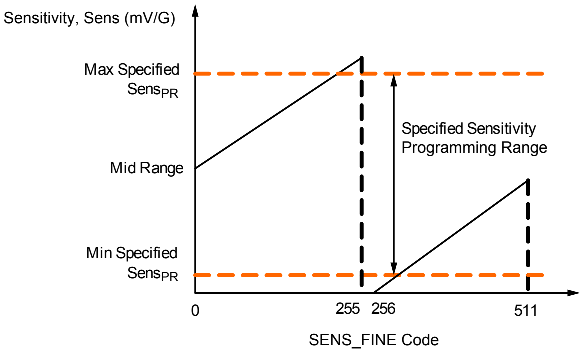


Figure 9: Device Sensitivity versus SENS_FINE Programmed Value

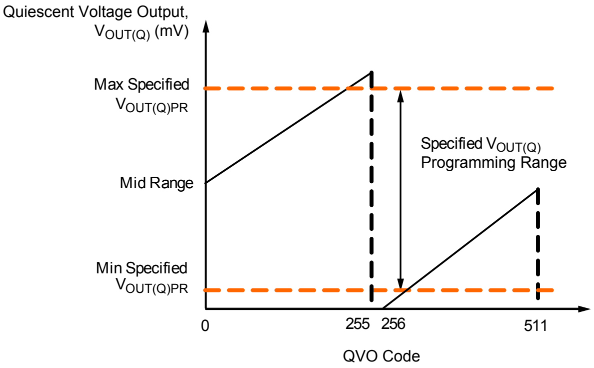


Figure 10: Device $V_{OUT(Q)}$ versus QVO Programmed Value

Power-On Reset (POR) and Undervoltage Lockout (UVLO) Operation

The descriptions in this section assume: T_A = 25°C, no output load (R_L, C_L), and no significant magnetic field is present.

- ***Power-Up*** At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 11 and [1'] in Figure 12), the POR Release counter starts counting for t_{PORR}. At this point, if V_{CC} exceeds V_{UVLOH} [2'], the output will go to V_{CC} / 2 after t_{UVLOD} [3']. If V_{CC} does not exceed V_{UVLOH} [2], the output will stay in the high-impedance state until V_{CC} reaches V_{UVLOH} [3] and then go to V_{CC} / 2 after t_{UVLOD} [4].
- ***V_{CC} drops below V_{CC}(min)= 4.5 V*** If V_{CC} drops below V_{UVLOL} [4', 5], the UVLO Enable Counter starts counting. If V_{CC} is still below V_{UVLOL} when the counter reaches t_{UVLOE}, the UVLO function will be enabled and the output will be pulled near GND [6]. If V_{CC} exceeds V_{UVLOL} before the UVLO Enable Counter reaches 64 µs [5'], the output will continue to be V_{CC}/2.
- ***Coming out of UVLO*** While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOH} [7], UVLO will be disabled after t_{UVLOD}, and the output will be V_{CC} / 2 [8].
- ***Power-Down*** As V_{CC} ramps down below V_{UVLOL} [6', 9], the UVLO Enable Counter will start counting. If V_{CC} is higher than V_{PORL} when the counter reaches t_{UVLOE}, the UVLO function will be enabled and the output will be pulled near GND [10]. The output will enter a high-impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO Enable Counter reaches t_{UVLOE}, the output will transition directly into a high-impedance state [7'].

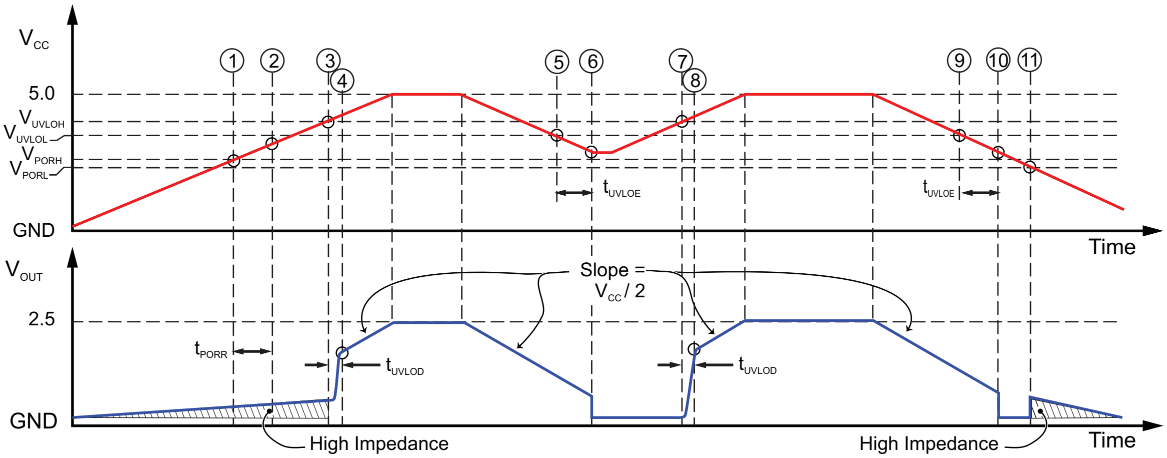


Figure 11: POR and UVLO Operation – Slow Rise Time Case

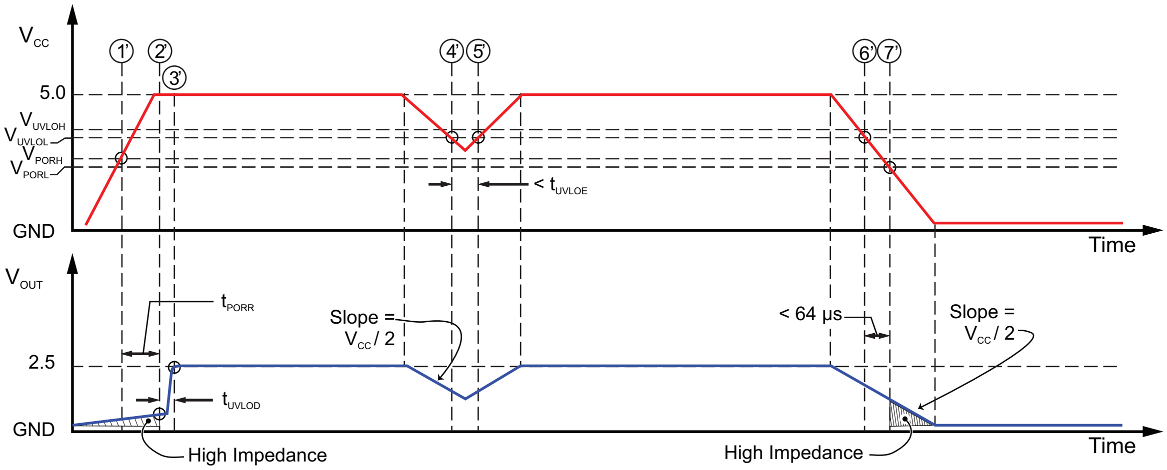


Figure 12: POR and UVLO Operation – Fast Rise Time Case

Detecting Broken Ground Wire

If the GND pin is disconnected, node A becoming open (see Figure 14), the VOUT pin will go to a high-impedance state. The output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDWN)}$ is connected to GND. The device will not respond to any applied magnetic field.

If the ground wire is reconnected, the A1365 will resume normal operation.

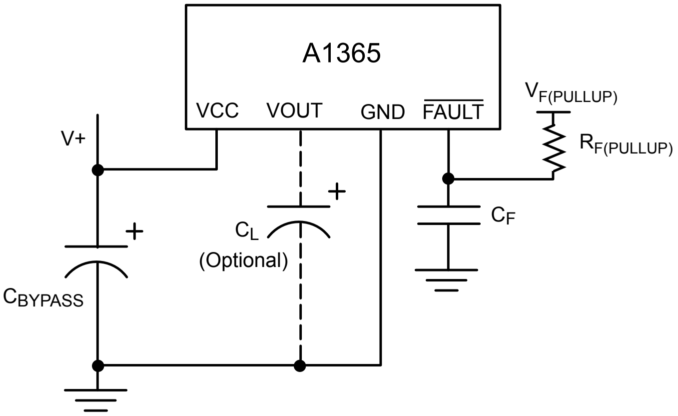
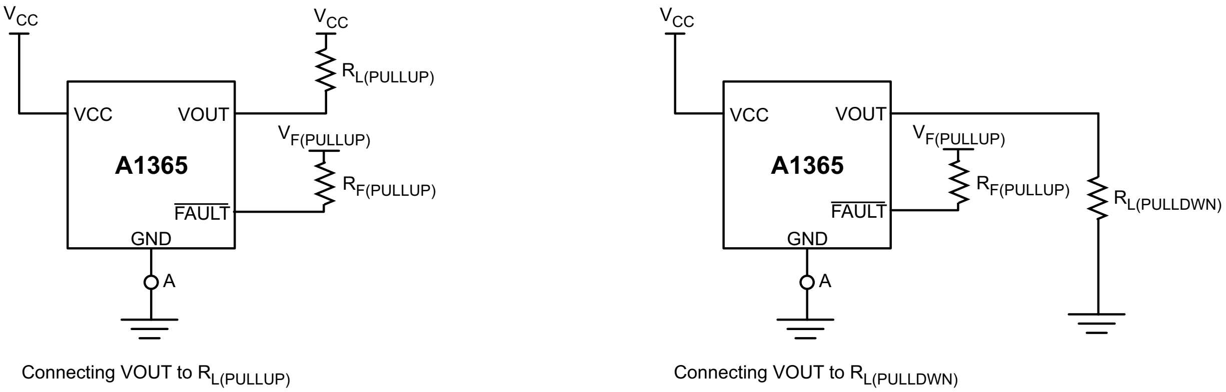


Figure 13: Typical Application Drawing



Connecting VOUT to $R_{L(PULLUP)}$

Connecting VOUT to $R_{L(PULLDWN)}$

Figure 14: Connections for Detecting Broken Ground Wire

Self-Test Diagnostic Operation after Power-Up

The A1365 has a Self-Test Diagnostics operating mode, allowing the user to verify at any point: connectivity of the Analog Signal path, drifts in sensitivity and quiescent output voltage, and connectivity and functionality of the Over Field Fault Signal path. Timing of various parts of the self-test sequence are user programmable.

Self-Test Start Mode

After power-up is complete, the VOUT pin responds to the applied magnetic field, and the Over Field $\overline{\text{FAULT}}$ pin responds to a magnetic field exceeding the programmed fault threshold. Self-Test Diagnostic mode can be started at any point after power-up by pulling $V_{\overline{FAULT}}$ below V_{STTH} level (location [1] in Figure 15), causing the sensor IC to enter the Self-Test Start mode and the self-test counter to start. The VOUT pin will continue responding to the magnetic field during this mode, but if the sensor IC is exposed to a magnetic field exceeding the fault threshold, the self-test counter will be reset. After the counter reaches the programmed Self-Test Start Time (t_{STS} [2]), the VOUT pin will go to V_{STL}, indicating that the sensor IC has entered Self-Test Sens mode.

Self-Test Sens Mode

Self-Test Sens mode allows the user to verify the sensitivity of the sensor IC. Setting $V_{\overline{FAULT}} > V_{STTH}$ [4] causes VOUT to respond by going to V_{STH}, [6]. Setting $V_{\overline{FAULT}} < V_{STTH}$ [7] causes VOUT to become equal to V_{STL} [9]. By measuring VOUT and comparing it to the specified values, the user can detect failures in the Analog Signal path as well as drifts in sensitivity. Quiescent voltage can be measured during the Self-Test Start waiting period as long as no external magnetic fields are present. When the $V_{\overline{FAULT}}$ value is changed in either direction [4, 7], Self-Test Sens Output Propagation Delay Time (t_{STSOPD}) is required before a change is observed on VOUT [5, 8]. VOUT will settle to a stable value after Self-Test Sens Output Rise Time (t_{STSORT} [6]) or Self-Test Sens Output Fall Time (t_{STSOFT} [9]). The sensor IC can stay in Self-Test Sens mode as long as required by the user. To exit, the $\overline{\text{FAULT}}$ pin should be released, causing $V_{\overline{FAULT}}$ to exceed V_{STTH} [10] and to be pulled near V_{CC} by the pull-up resistor. When the programmed Self-Test Fault Request Time (t_{STFR}) expires [11], the device will enter Self-Test Fault mode.

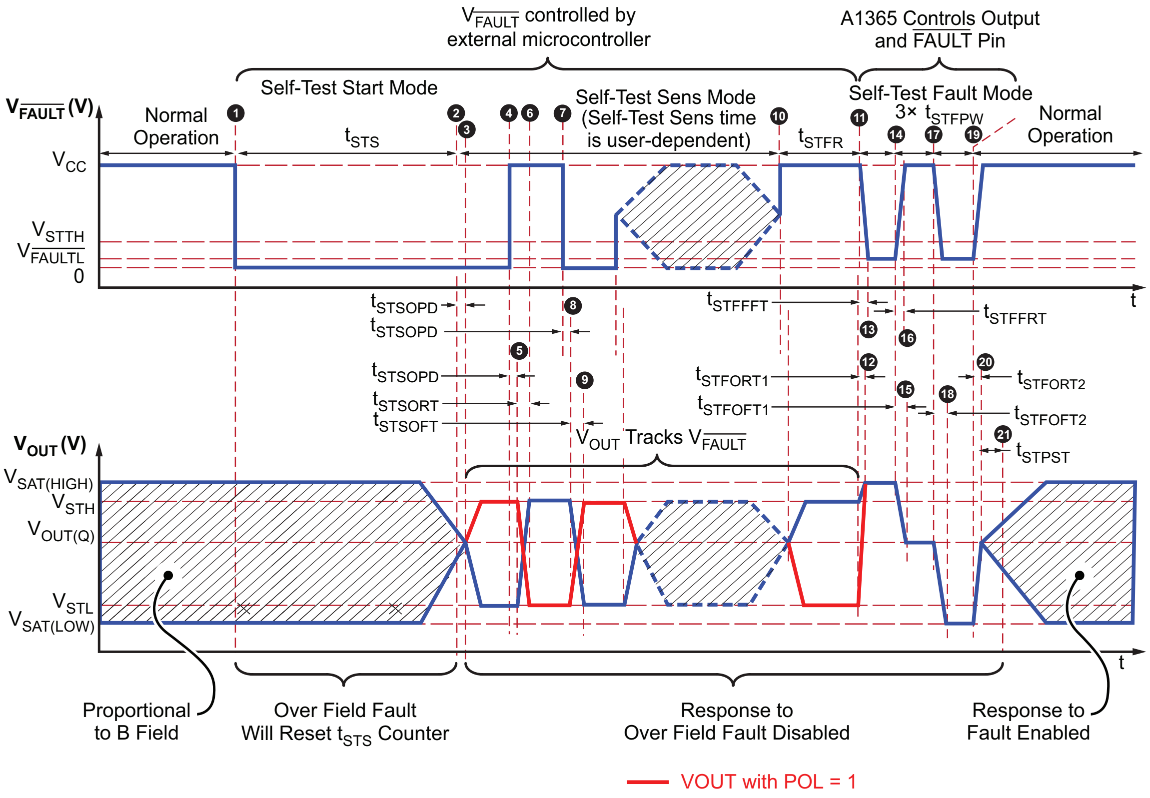


Figure 15: Self-Test Diagnostic Mode Fault Behavior

Self-Test Fault Mode

During Self-Test Fault mode, the $\overline{\text{FAULT}}$ pin should be released by the user. The A1365 will automatically apply an internal positive stimulus to the internal signal path, causing the output to reach $V_{SAT(HIGH)}$ [12]. After V_{OUT} crosses the programmed fault threshold, the $\overline{\text{FAULT}}$ pin will be pulled to $V_{\overline{FAULT}L}$ [13]. After the programmed Self-Test Fault Pulse Width time (t_{STFPW}) has expired [14], the positive internal stimulus will be removed, causing the output to settle at $V_{OUT(Q)}$ [15], which in turn will cause the $\overline{\text{FAULT}}$ pin to be released and pulled to V_{CC} [16].

After the Self-Test Fault Pulse Width time (t_{STFPW}) has expired [17], a negative internal stimulus will be applied to the signal path, causing the output to reach $V_{SAT(LOW)}$ [18]. After V_{OUT} crosses the programmed fault threshold, the $\overline{\text{FAULT}}$ pin will be pulled to GND. After the Self-Test Fault Pulse Width time (t_{STFPW}) has expired [19], the output will be released and should reach $V_{OUT(Q)}$ in the absence of an external magnetic field [20]. The A1365 will then automatically exit Self-Test mode, release the $\overline{\text{FAULT}}$ pin, and resume normal operation after the Post Self-Test Settling Time (t_{STPST} [21]). The user can determine if the Over Fault Signal path is functional by ensuring the VOUT pin and the $\overline{\text{FAULT}}$ pin toggle as described in Figure 13 and reach the appropriate voltage levels.

Self-Test Operating Conditions

For proper functionality, no magnetic field should be present during any Self-Test mode. If a read/write transaction is received during any Self-Test mode, the sensor IC will exit Self-Test and service the transaction. A Self-Test Start request is ignored during a read/write transaction. If V_{CC} drops below V_{UVLOL}, the sensor IC will exit Self-Test mode.

Table 1: Self-Test Operating Characteristics: Valid through the full operating temperature range T_A, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V, and no magnetic field is present, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SELF-TEST START MODE						
Self-Test Start Time [1]	t_{STS}	Programmable	0.05	–	200	ms
Self-Test Threshold Voltage [2]	V_{STTH}		0.85	1	1.15	V
Self-Test Comparator Hysteresis	V_{STHYST}		–	75	–	mV
Self-Test Sens Mode						
Self-Test Sens Output Propagation Delay	t_{STSOPD}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	4	–	µs
Self-Test Sens Output Rise Time	t_{STSORT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	8	–	µs
Self-Test Sens Output Fall Time	t_{STSOFT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	8	–	µs
Self-Test Fault Request Time [1]	t_{STFR}	Programmable	0.05	–	10	ms
Self-Test High Output Voltage [2]	V_{STH}		$V_{OUT(Q)}$ + 1.275	$V_{OUT(Q)}$ + 1.5	$V_{OUT(Q)}$ + 1.725	V
Self-Test Low Output Voltage [2]	V_{STL}		$V_{OUT(Q)}$ – 1.725	$V_{OUT(Q)}$ – 1.5	$V_{OUT(Q)}$ – 1.275	V
Ratiometry Self-Test Sensitivity Error	$Rat_{ERRSTSens}$	T_A = 25°C to 150°C relative to V_{CC} = 5 V ±5%	–4	–	4	%
		T_A = –40°C to 25°C relative to V_{CC} = 5 V ±5%	–5	–	5	%
SELF-TEST FAULT MODE						
Self-Test Fault Pulse Width Time [1]	t_{STFPW}	Programmable	0.05	–	10	ms
Self-Test Fault Fault Fall Time	t_{STFFFT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	0.7	–	µs
Self-Test Fault Fault Rise Time	t_{STFFRT}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	17	–	µs
Self-Test Fault Output Rise Time	$t_{STFORT1}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	0.1	–	µs
	$t_{STFORT2}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	1	–	µs
Self-Test Fault Output Fall Time	$t_{STFOFT1}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	1	–	µs
	$t_{STFOFT2}$	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	1	–	µs
Post Self-Test Settling Time	t_{STPST}	$R_{F(PULLUP)}$ = 10 kΩ, C_F = 1 nF, C_L = 1 nF, $R_{L(PULLDOWN)}$ = 4.7 kΩ	–	5	–	µs

[1] Programmed timer could have a typical error of ±5%.
[2] Ratiometric with V_{CC}.

Table 2: Self-Test Timers DAC Profiles

Self-Test Start Time		Self-Test Fault Request Time		Self-Test Fault Pulse Width Time	
4-Bit Code (Decimal Equivalent)	t_{STS} (ms)	3-Bit Code (Decimal Equivalent)	t_{STFR} (ms)	3-Bit Code (Decimal Equivalent)	t_{STFPW} (ms)
0	0.05	0	0.05	0	0.05
1	0.1	1	0.1	1	0.1
2	0.2	2	0.2	2	0.2
3	0.5	3	0.5	3	0.5
4	1	4	1	4	1
5	2	5	2	5	2
6	5	6	5	6	5
7	10	7	10	7	10
8	20				
9	50				
10	100				
11	200				
12	200				
13	200				
14	200				
15	200				

Over Magnetic Field Fault

During normal operation, the $\overline{\text{FAULT}}$ pin is in a high-impedance state. The combination of an internal pull-up resistance with an internal current source enables the $\overline{\text{FAULT}}$ pin to be pulled high. After the $\overline{\text{FAULT}}$ pin reaches $V_{SAT(HIGH)}$, the current source is shut down.

The user could install an external pull-up resistor on the $\overline{\text{FAULT}}$ pin to reduce the amount of time required by the $\overline{\text{FAULT}}$ pin to reach $V_{SAT(HIGH)}$ after a fault event passes. An external pull-up resistor can be connected to a voltage ($V_{F(PULLUP)}$) different from VCC as long as it remains within the $V_{F(PULLUP)}$ limits. If $V_{F(PULLUP)}$ is less than VCC, the current provided by the internal current source, $I_{IF(PULLUP)}$, will flow through the external pull-up resistance causing a small voltage drop.

The A1365 offers a 6-bit programmable Ratiometric Fault as well as a 2-bit programmable Ratiometric Fault Hysteresis.

Figure 17 illustrates the impact of programming 60 mV of Fault Hysteresis on the Fault Switch Point:

- FAULT_THRESH = 0, setting Positive and Negative Field Fault Switch Point (V_{FPSP}, V_{FNSP}) to the middle of their programmable range.
- FAULT_HYST = 2, setting Fault Hysteresis Level to 60 mV.

The Fault Switch Point is not affected by the selected Fault Hysteresis Level.

The speed and accuracy with which a fault is triggered are characterized by the Transient Fault Response Time (t_{TFR}), the DC Fault Switch Point Error (err_{DFS}), and the Fault Delay Due to Load Capacitance (t_{FDC}).

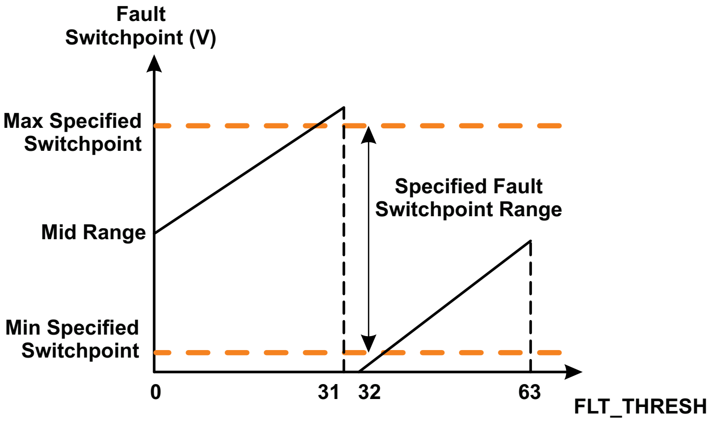


Figure 16: Fault Switch Point Programming Profile

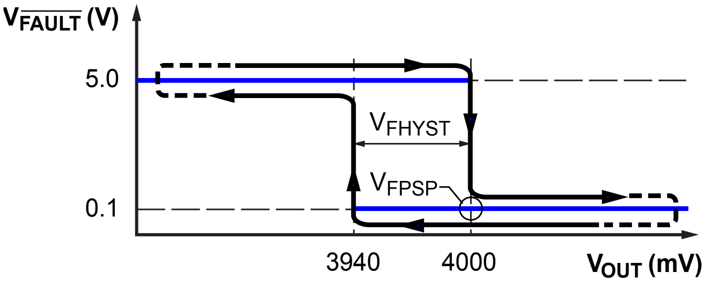


Figure 17: Fault Hysteresis Behavior at FAULT_THRESH = 0, FAULT_HYST = 2

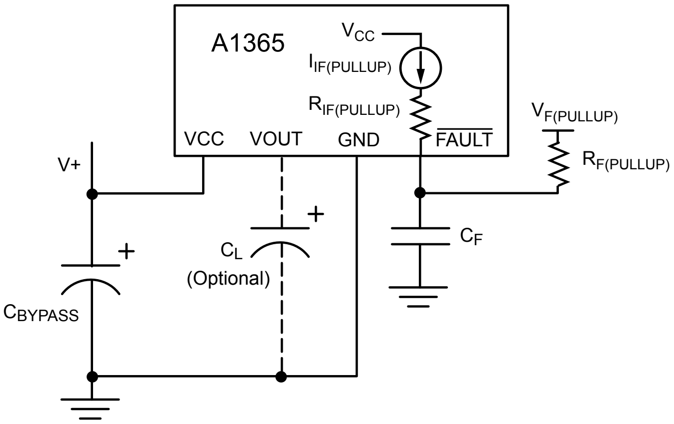


Figure 18: Fault Functional Circuit

A *Fault Overstep* is defined as the amount by which the output voltage exceeds the delta between $V_{OUT(Q)}$ and the DC Fault Switch Point (V_{FPSP} and V_{FNSP}). The larger the overstep caused by an input magnetic field is, the faster t_{TFR} will be. When V_{FPSP} and V_{FNSP} are programmed near their limits, the maximum Fault Overstep will be limited because V_{OUT} will be reaching saturation levels (see Figure 19).

Faults can be latched by setting the FAULT_LATCH bit high. After a fault occurs, the $\overline{\text{FAULT}}$ pin will be held low. To reset the $\overline{\text{FAULT}}$ pin, the A1365 must be powered down.

Over Magnetic Field Fault can be disabled by setting the FLT_DIS bit.

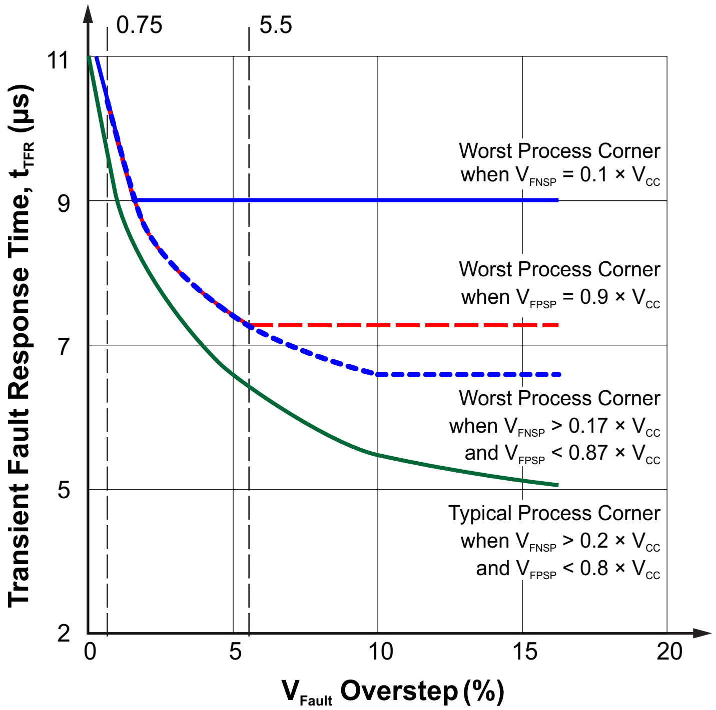


Figure 19: Transient Fault Response Time versus Fault Overstep Voltage at V_{CC} = 5 V, C_F = 0 F, R_L = Open.

PROGRAMMING SERIAL INTERFACE

The A1365 incorporates a serial interface that allows an external controller to read and write registers in the EEPROM and volatile memory. The A1365 uses a point-to-point communication protocol, based on Manchester encoding per G. E. Thomas (a rising edge indicates 0 and a falling edge indicates 1), with address and data transmitted MSB first.

Transaction Types

Each transaction is initiated by a command from the controller; the A1365 does not initiate any transactions. Three commands are recognized by the A1365: Write Access Code, Write, and Read. One response frame type is generated by the A1365, Read Acknowledge. If the command is Read, the A1365 responds by transmitting the requested data in a Read Acknowledge frame. If the command is any other type, the A1365 does not acknowledge. As shown in Figure 20, the A1365 receives all commands via the VCC pin. It responds to Read commands via the VOUT pin. This implementation of Manchester encoding requires the communication pulses be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages for the VCC line and the VOUT line. The Write command to EEPROM is supported by two high-voltage pulses on the VOUT line.

Writing the Access Code

In order for the external controller to write or read from the A1365 memory during the current session, it must establish serial communication with the A1365 by sending a Write command including the Access Code within Access Code Timeout (t_{ACC}) from power-up. If this deadline is missed, all write and read access is disabled until the next power-up.

Writing to Volatile Memory

In order for the external controller to write to volatile memory, a Write command must be transmitted on the VCC pin. Successive Write commands to volatile memory must be separated by t_{WRITE}. The required sequence is shown in Figure 21.

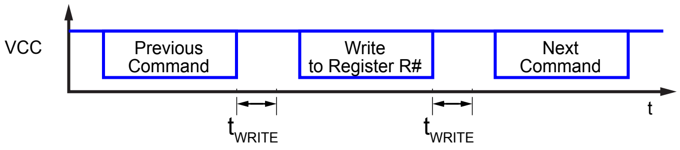


Figure 21: Writing to Volatile Memory

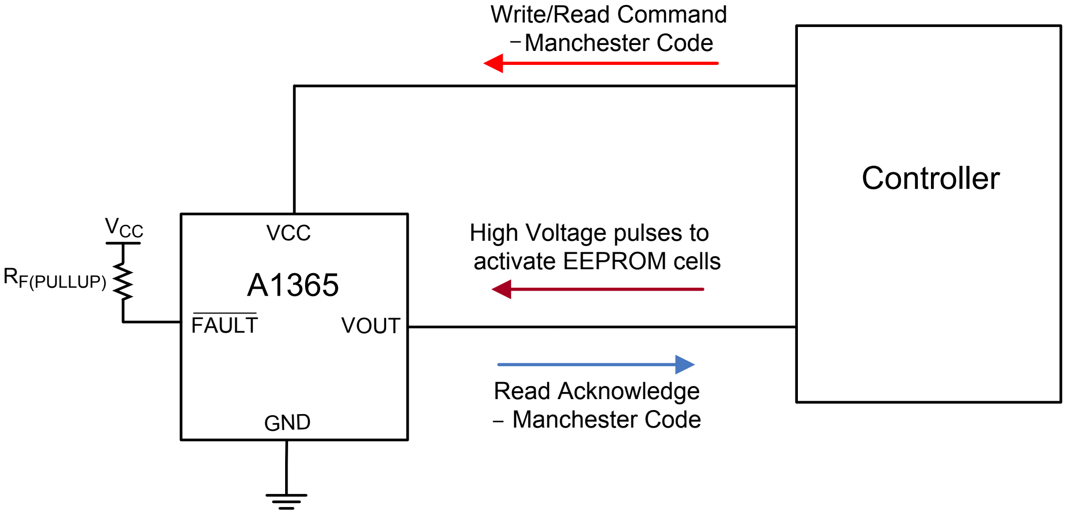


Figure 20: Top-Level Programming Interface

Writing to EEPROM

In order for the external controller to write to non-volatile EEPROM, a Write command must be transmitted on the VCC pin. The controller must also send two Programming pulses, long high-voltage strobes, via the VOUT pin. These strobes are detected internally, allowing the A1365 to boost the voltage on the EEPROM gates. The required sequence is shown in Figure 22 and Figure 23.

To ensure EEPROM integrity over lifetime, EEPROM should not be exposed to more than 100 Write cycles.

Reading from EEPROM or Volatile Memory

In order for the external controller to read from EEPROM or volatile memory, a Read command must be transmitted on the VCC line. Within time t_{start_read}, the VOUT line will stop responding to the magnetic field and the Read Acknowledge frame will be transmitted on the VOUT line. The Read Acknowledge frame contains Read data.

After the Read Acknowledge frame has been received from the A1365, the VOUT line resumes normal operation after time t_{READ}. The required sequence is shown in Figure 24.

Error Checking

The serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored during the check). The CRC algorithm is based on the polynomial g(x) = x3 + x + 1, and the calculation is represented graphically in Figure 25. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 111. If the serial interface receives a command with a CRC error, the command is ignored.

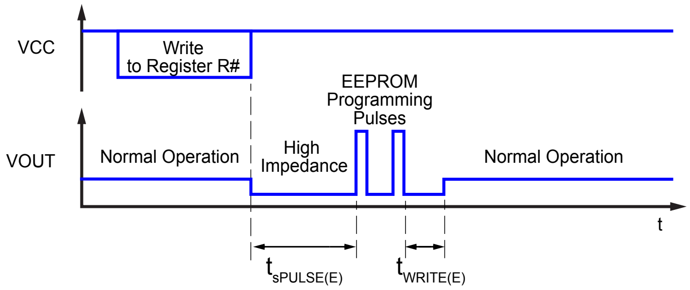


Figure 22: Writing to EEPROM

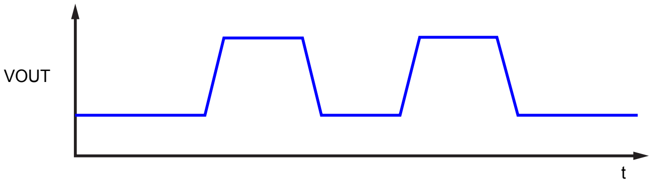


Figure 23: EEPROM Programming Pulses

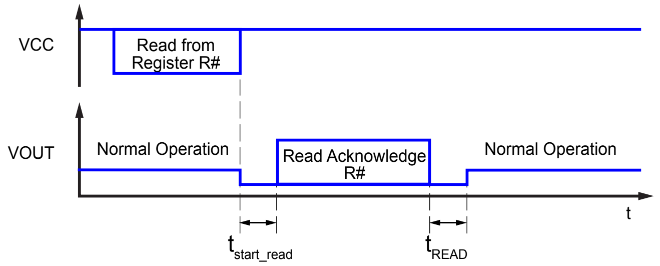


Figure 24: Reading from EEPROM or Volatile Memory

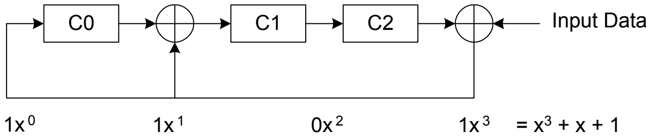


Figure 25: CRC Calculation

Serial Interface Reference

Required timing parameters for successful serial communication with A1365 device are given in table below.

Table 3: Required Serial Interface Timing Parameters

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Access Code Timeout	t_{ACC}	Customer Access Code should be fully entered in less than t_{ACC}, measured from when V_{CC} crosses V_{UVLOH}.	–	–	8	ms
Bit Rate	t_{BITR}	Defined by the input message bit rate sent from the external controller	32	–	80	kbps
Bit Time	t_{BIT}	Data bit pulse width at 70 kbps	13.6	14.3	15	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+ 11	%
Volatile Memory Write Delay	t_{WRITE}	Required delay from the trailing edge of certain Write command frames to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Non-Volatile Memory Write Delay	$t_{WRITE(E)}$	Required delay from the trailing edge of the second EEPROM Programming pulse to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Read Acknowledge Delay	t_{READ}	Required delay from the trailing edge of a Read Acknowledge frame to the leading edge of a following command frame	2 × t_{BIT}	–	–	µs
Read Delay	t_{start_read}	Delay from the trailing edge of a Read command frame to the leading edge of the Read Acknowledge frame	25 µs – 0.25 × t_{BIT}	50 µs –0.25 × t_{BIT}	150 µs – 0.25 × t_{BIT}	µs
EEPROM PROGRAMMING PULSE						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last edge of write command to start of EEPROM programming pulse	40	–	–	µs
INPUT/OUTPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	5.1	–	–	V
		Read from VOUT line	V_{CC} – 0.2 V	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	3.9	V
		Read from VOUT line	–	–	0.2	V
Manchester Level to VCC Delay	t_{MAN_VCC}		–	–	15	µs

Serial Interface Message Structure

The general format of a command message frame is shown in Figure 26. Note that, in the Manchester coding used, a bit value of one is indicated by a falling edge within the bit boundary, and a bit value of zero is indicated by a rising edge within the bit boundary.

V_{CC} Levels During Manchester Communication

For all devices with UVLO functionality, after power-up, it is important that the VCC pin be held at V_{CC} until the first Synchronization pulse of a read/write transaction is sent (see Figure 27). During the transaction, the VCC pin varies between $V_{MAN(H)}$ and $V_{MAN(L)}$, but after the last CRC bit has been sent, the controller must bring the VCC pin back to the V_{CC} level in less than t_{MAN_VCC}. This is important in order to avoid triggering the UVLO functionality during EEPROM read/write.

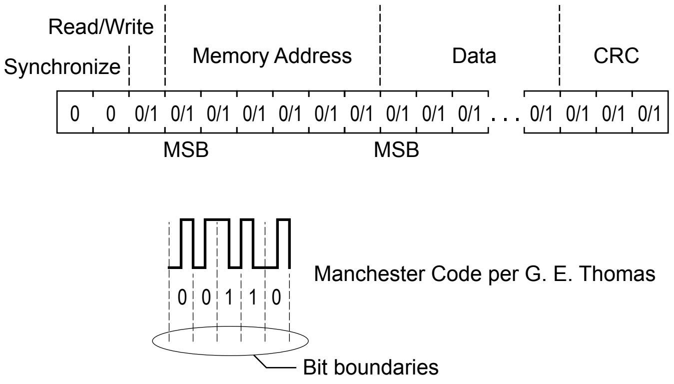


Figure 26: General Format for Serial Interface Commands

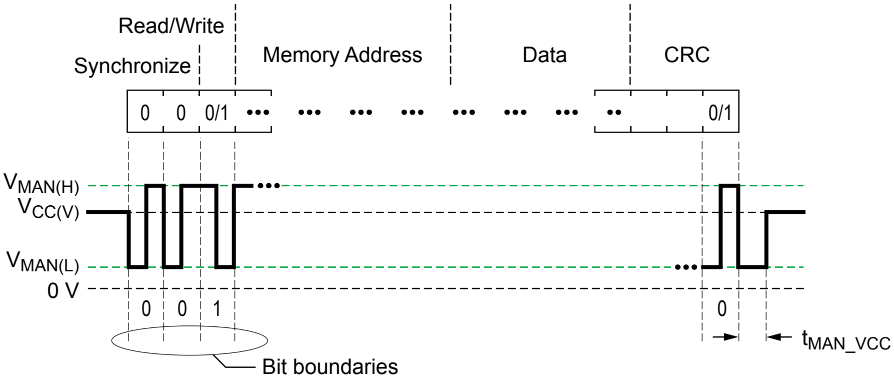


Figure 27: V_{CC} Levels During Manchester Communication

Table 4: Serial Interface Command General Format

Quantity of Bits	Parameter Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
30	Data	0/1	24 data bits and 6 ECC bits
3	CRC	0/1	Incorrect value indicates errors

Read (Controller to A1365)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- Address (6 bits) (ADDR[5] is 0 for EEPROM, 1 for register)
- CRC (3 bits)

Figure 28 shows the sequence for a Read command.

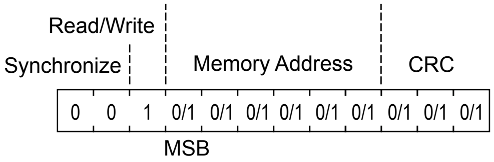


Figure 28: Read Sequence

Read Acknowledge (A1365 to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (30 bits: [29:26] Don't Care, [25:24] ECC Pass/Fail, [23:0] Data)
- CRC (3 bits)

Figure 29 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect and ECC failure.

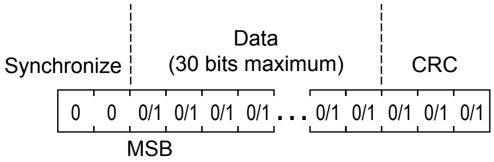


Figure 29: Read Acknowledge Sequence

Write (Controller to A1365)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits) (ADDR[5] is 0 for EEPROM, 1 for register; refer to the address map)
- Data (30 bits: [29:24] Don't Care, [23:0] Data)
- CRC (3 bits)

Figure 30 shows the sequence for a Write command. Bits [29:24] are Don't Care because the A1365 automatically generates 6 ECC bits based on the content of bits [23:0]. These ECC bits will be stored in EEPROM at locations [29:24].

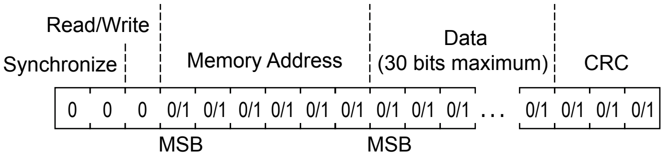


Figure 30: Write Sequence

Write Access Code (Controller to A1365)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits) (Address 0X24 for Customer Access)
- Data (30 bits) (0x2781_1F77 for Customer Access)
- CRC (3 bits)

Figure 31 shows the sequence for an Access Code command.

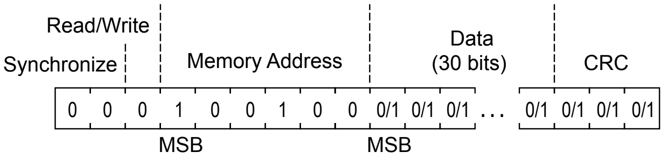


Figure 31: Access Code Write Sequence

The controller must open the serial communication with the A1365 device by sending an Access Code. It must be sent within Access Code Timeout (t_{ACC}) from power-up or the device will be disabled for read and write access.

Access Codes Information

Name	Serial Interface Format	
	Register Address (Hex)	Data (Hex)
Customer	0x24	0x2781_1F77

Shadow Mode

For faster programming, Shadow Mode puts the sensor in a try mode where one can write to the EEPROM registers as if they are volatile registers. This is especially useful when searching for Sensitivity, QVO, and Over Field Fault codes. Once the desired codes are identified, the user should exit Shadow Mode and execute an EEPROM Write. If a power-cycle is executed during Shadow Mode, the registers will reset to their initial state. SHADOW_ENABLE bit should be set to enter Shadow Mode.

EEPROM Margining

Allegro factory-tests the capacity of each EEPROM bit to retain a “0” or a “1” state. After the user has completed EEPROM programming, the two VREAD bits could be set to “01” to change the EEPROM margin setting. EEPROM registers that were written by the user should be read and compared to the user-programmed value. The procedure should be repeated using VREAD = “10”. It is not mandatory for the user to execute EEPROM Margining.

Table 5: Memory Address Map

Register Name		Address	Description	r/w	Bits	Location
Customer Read-Only EEPROM	FAC_LOT_NUM	0x00*	Factory Lot (uses 3rd to 7th digits of the lot number)	r/w	16	15:0
	WAFER_NUM		Factory Wafer (stores up to 64 wafers)	r/w	6	21:16
	SCRATCH		Factory use only	r/w	2	23:22
	X_DIE_LOC	0x01*	8 bits X die location (accommodates up to 256 die in X)	r/w	8	7:0
	Y_DIE_LOC		8 bits Y die location (accommodates up to 256 die in Y)	r/w	8	15:8
	SCRATCH		Factory use only	r/w	8	23:16
Customer R/W EEPROM	SENS_FINE	0x02	Sensitivity	r/w	9	8:0
	SENS_COARSE		Coarse Sensitivity	r/w	2	10:9
	QVO		Quiescent Output Voltage	r/w	9	19:11
	FACTORY_RES1		Factory use only	r/w	1	20
	POL		Reverses output polarity	r/w	1	21
	CLAMP_EN		Clamp Enable	r/w	1	22
	EELOCK		EEPROM LOCK	w	1	23
	FLT_THRESH	0x03	Sets the DC Fault Switch Point, two’s complement DAC profile	r/w	6	5:0
	FLT_HYST		Fault Hysteresis Adjust, [00] = 0 V, [01] = 30 mV, [10] = 60 mV, [11] = 120 mV	r/w	2	7:6
	FLT_LATCH		Enables Fault Latch	r/w	1	8
	FLT_DIS		Disables Fault	r/w	1	9
	ST_DIS		Disables Self-Test (Halts Self-Test sequence if written while Self-Test is in progress)	r/w	1	10
	ST_START_TIME		Self-Test start time, range 50 µs to 200 ms	r/w	4	14:11
	ST_FR_TIME		Self-Test Fault Request time, range 50 µs to 10 ms	r/w	3	17:15
	ST_FPW_TIME		Self-Test Fault Pulse Width time, range 50 µs to 10 ms	r/w	3	20:18
	MISC3_1		Factory-reserved (unused)	r/w	3	23:21
	CUSTOMER_RES	0x04*	Customer-reserved	r/w	24	23:0
Volatile Memory Customer Debug Register	Disable Analog Output	0x10	Sets the output pin to a high-impedance state	r/w	1	0
	SHADOW_ENABLE		Enables register shadowing to bypass shadowed EEPROM registers	r/w	1	1
	CUSTOMER_ACCESS		Customer write access enabled	r	1	2
	Factory Reserved		Reserved for factory use. Do not change default state.	r/w	2	4:3
	OVERF_FLT		0 = No Over Field Fault 1 = Over Field Fault occurred, clears on read	r	1	5
	Factory Reserved		Reserved for factory use; do not change default state.	r/w	2	8:7
	VREAD		Change EEPROM read voltage for margining; [00] = 1.2 V (default), [01] = 0 V, [10] = 4.3 V, [11] = undefined	r/w	2	10:9
	–		Reserved for factory use (unused)	n/a	13	23:11
ACCESS_CODE		0x24	Customer code (not addressable)		30	29:0

* EEPROM registers or bits that are not shadowed.

EEPROM Cell Organization

Programming coefficients are stored in non-volatile EEPROM, which is separate from the digital subsystem, and accessed by the digital subsystem EEPROM Controller module. The EEPROM is organized as 30-bit-wide words, each word is made up of 24 data bits and 6 ECC (Error Checking and Correction) check bits, stored as shown in figure below.

EEPROM Bit	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Contents	C5	C4	C3	C2	C1	C0	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

External EEPROM Word Bit Sequence; C# – Check Bit, D# – Data Bit

EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 30 bits.

The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first 6 received bits from device to controller are dedicated to ECC.

Detecting ECC Error

If an uncorrectable error has occurred, bits 25:24 are set to 10, the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field. Output voltage will go to $V_{BRK(HIGH)}$ if a load resistor $R_{L(PULLUP)}$ is connected to V_{CC} or to $V_{BRK(LOW)}$ if a load resistor $R_{L(PULLDWN)}$ is connected to GND.

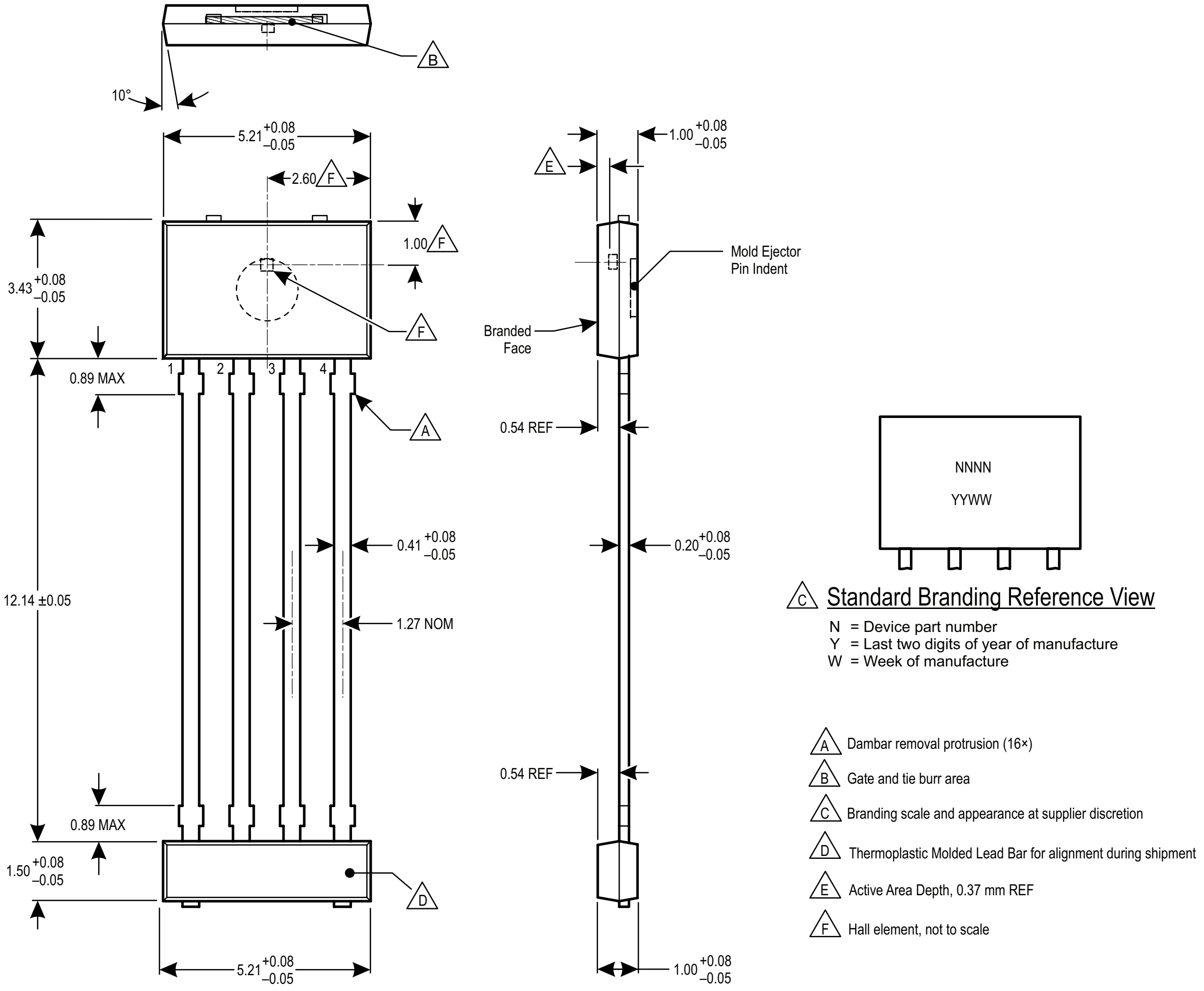
EEPROM ECC Errors

Bits	Name	Description
29:26	–	No meaning
25:24	ECC	00 = No error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
23:0	D[23:0]	EEPROM data

PACKAGE OUTLINE DRAWING

For Reference Only - Not for Tooling Use

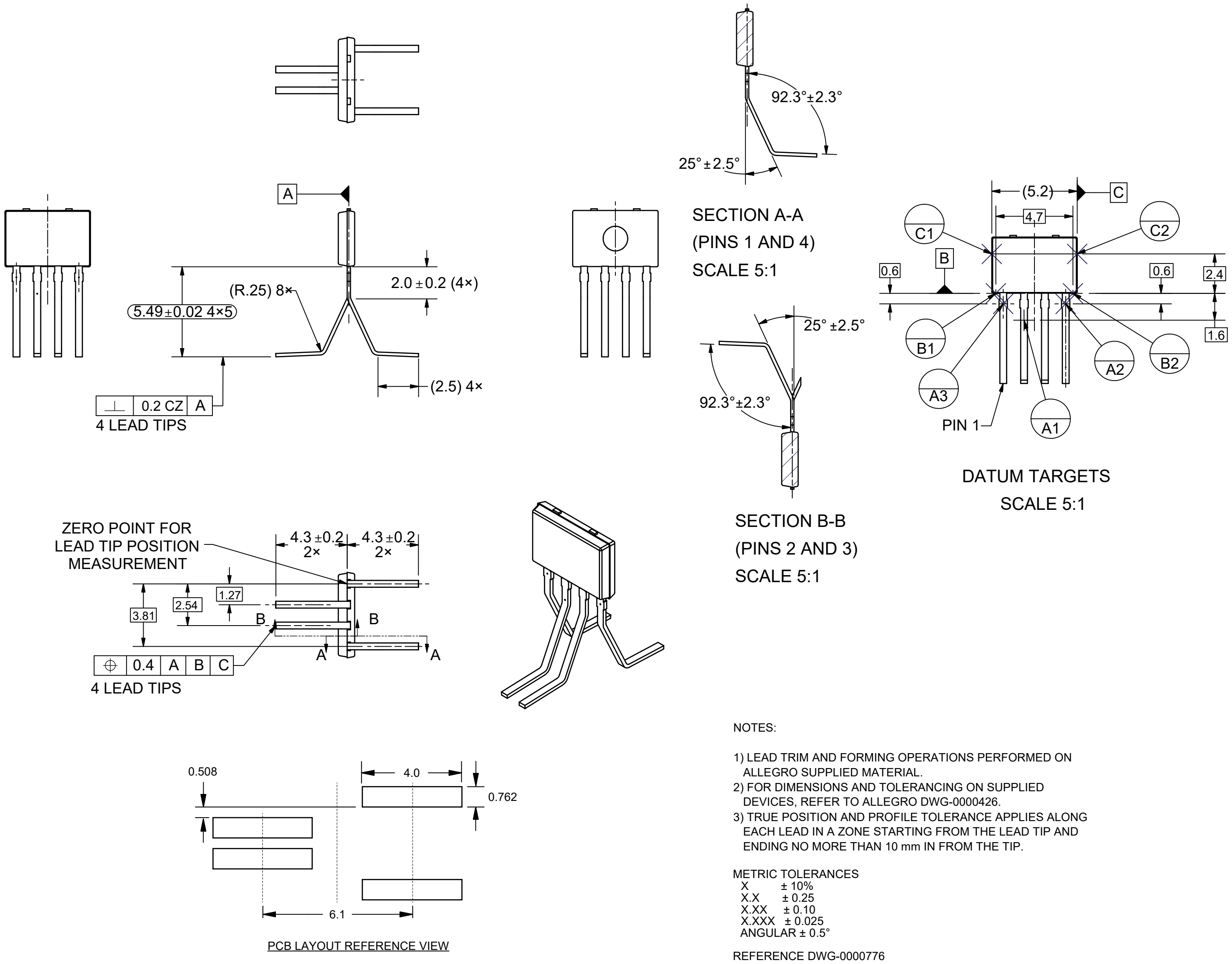
(Reference DWG-9202)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



N = Device part number
Y = Last two digits of year of manufacture
W = Week of manufacture

A Dambar removal protrusion (16×)
B Gate and tie burr area
C Branding scale and appearance at supplier discretion
D Thermoplastic Molded Lead Bar for alignment during shipment
E Active Area Depth, 0.37 mm REF
F Hall element, not to scale

Figure 32: Package KT, 4-Pin SIP, TN Leadform



NOTES:

1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000426.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES

X	± 10%
X.X	± 0.25
X.XX	± 0.10
X.XXX	± 0.025
ANGULAR ± 0.5°	

REFERENCE DWG-0000776

Figure 33: Package KT, 4-Pin SIP, TH Leadform

Revision History

Number	Date	Description
–	January 7, 2016	Initial release
1	November 2, 2017	Corrected Package Outline Drawing Standard Branding label
2	November 16, 2017	Added Self-Test functionality information
3	December 6, 2017	Added Self-Test registers to Memory Address Map (p. 33)
4	January 3, 2018	Updated Features and Benefits, Description sections (p. 1)
5	January 14, 2019	Updated Figure 15 (p. 22)
6	March 14, 2019	Added TF and TG leadforms
7	April 9, 2020	Minor editorial updates
8	September 28, 2020	Removed TF/TG leadforms and footprints (pages 1-2, 37-38); added TH leadform and footprint (pages 1, 37); updated package outline drawing (page 36)