

NB4N441MNGEVB

NB4N441MNGEVB Evaluation Board User's Manual

Device Name: NB4N441MN



ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Description

The NB4N441MNG is a precision clock PLL based synthesizer which generates select differential LVPECL clock output frequencies from 12.5 MHz to 425 MHz. A Serial Peripheral Interface (SPI) is used to configure the device to produce output frequencies from a single 27 MHz crystal input reference by programming three internal registers, P (pre-scale), M (PLL Feedback Divider), and N (Output Divider) using a three line LVTTTL/LVCMOS Serial Data Interface (SDI) consisting of a SERIAL DATA (SDATA) input, a SERIAL CLOCK (SCLOCK) input, and a SERIAL LOAD (SLOAD).

The NB4N441MNGEVB Evaluation board is designed to provide a flexible and convenient platform to quickly program, evaluate and verify the performance and operation of the NB4N441MNG device under test: With the device removed, this NB4N441MNGEVB Evaluation board is designed accept a 24 LD QFN GCI socket (M&M Specialties, Inc., 1-800-892-8760, www.mmspec.com, Dwg No.50-000-00306) to permit use as an insertion test fixture.

Board Features

- On board 27 MHz crystal source, or input external clock source (SMA)
- On board serial data loader with 16-bit DIP switches, or externally serial program through SMA connectors.
- PLL In Lock LED status indicator.
- 3.3 V split-power supply operation (banana jack and anvil supply connectors for V_{CC}, SMAGND, and DUTGND)
- LVPECL differential output signals via SMA connectors with provision for termination resistors.

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Appendix 3: Bill Of Materials, Lamination Stackup

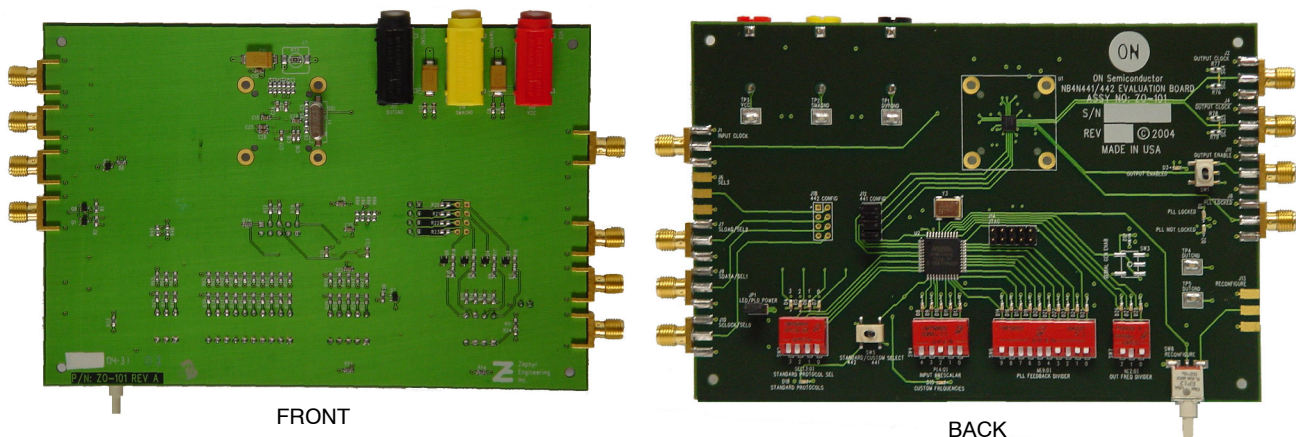
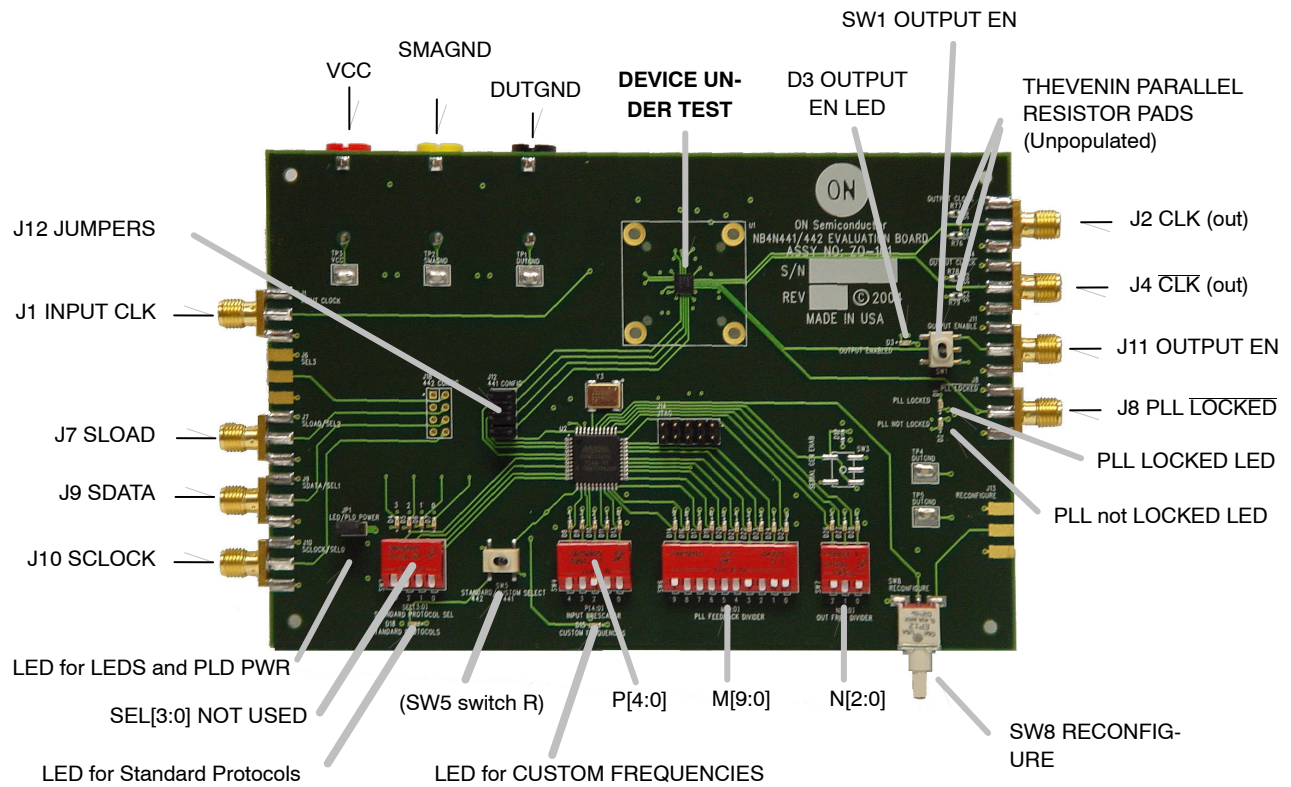


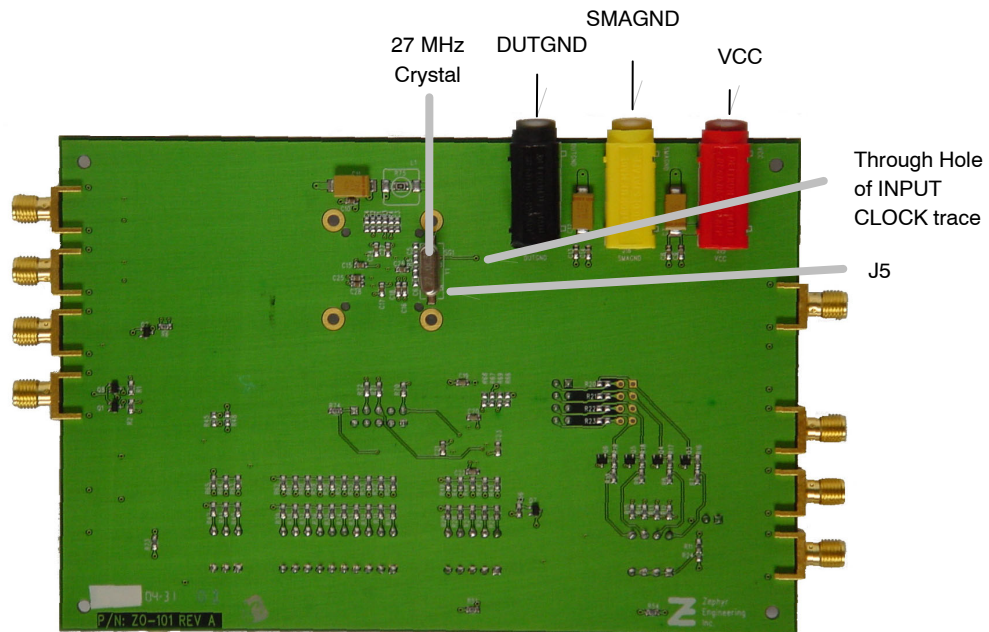
Figure 1. NB4N441MNGEVB Evaluation Board

NB4N441MNGEVB

BOARD LAYOUT MAP



FRONT



BACK

Figure 2. Board Layout Map

TEST AND MEASUREMENT SETUP AND PROCEDURE

Step 1: Equipment (or equivalent)

1. Agilent Signal Generator #33250A for CLK input
2. Tektronix TDS8000 Oscilloscope or Frequency Counter
3. Agilent #6624A DC Power Supply
4. Digital Voltmeter
5. Matched high-speed cables with SMA connectors

Step 2: Lab Setup Procedure for Split Supplies (into LOW impedance 50 Ω equipment or probes)

1. **Output Enable OFF:** Switch SW1 (UP) or externally LOW through J11 (offset LVCMOS/LVTTL of 2.0 V HIGH and -1.3 V LOW) to disable the output during setup. LED D3 indicator will be off to indicate disabled output.
2. **Supplies:** Connect a “split” power supply to the evaluation board for 3.3 V operation as follows:
 - V_{CC} (RED banana jack or clip anvil) at +2.0 V
 - SMAGND (YELLOW banana jack or clip anvil) at 0 V
 - DUTGND (BLACK banana jack or clip anvil) -1.3 V

3. **Output:** Connect LVPECL Output CLOCK and Output $\overline{\text{CLOCK}}$ outputs to the oscilloscope with matched cables.
 NOTE: The readings of the output voltage levels will be offset by -1.3 V from standard LVPECL levels. With this split supply, the device outputs will be parallel terminated by the oscilloscope (or frequency counter) input module’s internal 50 Ω to GND impedance. See the data sheet Figure 10, where $\text{SMAGND} = \text{V}_{\text{TT}} = \text{V}_{\text{CC}} - 2.0 \text{ V} = 0 \text{ V} = \text{OSCILLOSCOPE GND}$.

An alternative thevenin parallel termination scheme can be accommodated by using the unpopulated Resistor Pads (R76, R77, R78, and R79) provided on the OUTPUT CLOCK and OUTPUT $\overline{\text{CLOCK}}$ lines near the SMA connectors. See AND8020 for additional details. Do not use both thevenin parallel termination scheme and LOW IMPEDANCE (50 Ω) termination schemes on the same output at the same time (double termination).

4. **Trigger:** Ensure the oscilloscope trigger input is properly setup and adjusted and has a 50 Ω termination to ground. The board does not provide 50 Ω source termination resistors. Two possible oscilloscope trigger methods might be
 1. “T” connector from CLKOUT to the trigger of the scope,
 2. Use $\overline{\text{CLKOUT}}$ directly to the trigger.
3. **XTAL/CLK Input:** Determine if the onboard crystal or an external signal reference will be used. Onboard Crystal signal source (27 MHz) is default

ready for use.

NOTE: If an external clock reference is used, then dismount the crystal and connect a clock signal (10 MHz – 50 MHz, 3.3 V_{PP} amplitude) with LEVELS OFFSET -1.3 V: as +2.0 V HIGH and -1.3 V LOW into CLK/XTAL1 (J1). Also short from the bottom side “through hole trace” of INPUT CLOCK to J5 (not J3). Do not drive XTAL2. Termination of the signal generator may be needed with 50 Ω to SMA ground.

4. **Program SDI:** The P, M, and N internal registers may be programmed by (A) the onboard PLD or (B) by using the three line 3.3 V_{PP} amplitude (offset LVTTL/LVCMOS) Serial Data Interface (SDI) consisting of a SERIAL DATA (SDATA) input, a SERIAL CLOCK (SCLOCK) input, and a SERIAL LOAD (SLOAD) as follows:

A. Onboard PLD

1. Insure all 4 of the J12 (441 CONFIG) jumpers are all installed connecting the PLD output to the Device
2. Insure JP1 LED/PLD indicates power is applied to the PLD (LED on);
3. Insure J3 (external CLOCK line from J1) is open, not LOADED, DRIVEN, or shorted;
4. Insure SW5 (LEFT: CUSTOM 441, RIGHT:STANDARD 442) select is set to the LEFT (bypassing SW2, SEL[3:0]). Note LED will light for “CUSTOM FREQUENCIES”.
5. Set SW4, SW6, and SW7 rocker switches to desired P, M, and N programming values: UP =0 LOGIC LOW (LED indicator OFF); DOWN = 1 LOGIC HIGH (LED indicator ON).
6. Load program values by depressing momentary switch SW8, or send a pulse signal (125 ns min) through J13 SMA connector (when installed) with OFFSET LVCMOS/LVTTL LEVELS of +2.0 V HIGH and -1.3 V LOW.

B. External SDI

1. See datasheet DC Table, AC Table, as well as Figures 5 and 6.
2. To use the SDI (serial data input) port, generate and input SCLOCK, SDATA, and SLOAD signals with OFFSET LVCMOS/LVTTL LEVELS of +2.0 V HIGH and -1.3 V LOW. The SCLOCK signal will sample the information presented on SDATA line. Values are loaded and indexed into a 18 bit shift register. The register shifts once per rising edge of the SCLOCK input. The serial input SDATA bits must each meet setup and

hold timing to the respective SCLOCK rising edge as specified in the AC Characteristics section of the datasheet document. The MOST Significant Bit (MSB), P4, is indexed in first followed by P3, P2, P1, N2, N1, N0, M9 through the LEAST Significant Bit (LSB), M0, indexed in last. A Pulse on the SLOAD pin after the SHIFT register is fully indexed (18 clocks) will load and latch the data values for the internal P, M, and N registers. The SLOAD pulse Low to HIGH rising edge transition transfers the data from the SHIFT register to the LATCH register. The SLOAD Pulse HIGH to LOW transition will lock the new data values into the LATCH register.

- Output Enable ON:** Switch SW1 (DOWN) or externally HIGH through J11 (offset LVCMOS/LVTTL of 2.0V HIGH and -1.3 V LOW) to enable the output after setup. LED D3 indicator will be ON to indicate an enabled output.

ALTERNATE STEP 2: LAB SET-UP PROCEDURE FOR SINGLE SUPPLY (INTO HIGH IMPEDANCE PROBES)

- Output Enable OFF:** Switch SW1 (UP) or externally LOW through J11 (standard LVCMOS/LVTTL of 2.0V HIGH and 0.8 V LOW) to disable the output during setup. LED D3 indicator will be off to indicate disabled output.
- Supplies:** Connect a “single” power supply to the evaluation board for 3.3 V operation as follows:
 - VCC (RED banana jack or clip anvil) at +3.3 V
 - SMAGND (YELLOW banana jack or clip anvil) at 0 V
 - DUTGND (BLACK banana jack or clip anvil) 0 V
- Output:** Connect LVPECL OUTPUT CLOCK and OUTPUT $\overline{\text{CLOCK}}$ outputs to the oscilloscope with matched cables. The device outputs will require proper termination. A thevenin parallel termination scheme can be accomplished by populating Resistor Pads (R76, R77, R78, and R79) provided on the OUTPUT CLOCK and OUTPUT $\overline{\text{CLOCK}}$ lines near the SMA connectors. Install 127 Ohm resistors R77 at SG4 and R78 at SG5. Install 83 Ohm resistors R76 at SG2 and R79 at SG2. See AND8020 for additional details. Use HIGH IMPEDANCE (FET) Probes or equipment only. Do not use LOW IMPEDANCE (50 Ω) equipment or probes when using thevenin parallel termination or the signal will be double terminated.
- Trigger:** Ensure the oscilloscope trigger input is setup and adjusted properly. A self triggered

real-time high impedance input scope will not require an external trigger connection.

- XTAL/CLK Input:** Determine if the onboard crystal or an external signal reference will be used. Onboard Crystal signal source is default ready for use.

NOTE: If an external clock reference is used, then dismount crystal and connect a clock signal (10 MHz – 50 MHz) with standard LVTTL/LVCMOS into INPUT CLOCK (J1). Also short from the bottom side “through hole trace” of INPUT CLOCK to J5 (not J3). Do not drive XTAL2. Termination of the signal generator may be needed with 50 Ω to SMA ground.

- Program SDI:** The P, M, and N internal registers may be programmed by (A) the onboard PLD or (B) by using the three line LVTTL/LVCMOS Serial Data Interface (SDI) consisting of a SERIAL DATA (SDATA) input, a SERIAL CLOCK (SCLOCK) input, and a SERIAL LOAD (SLOAD) as follows:

A. Onboard PLD

- Insure all 4 of the J12 (441 CONFIG) jumpers are all installed connecting the PLD output to the Device
- Insure JP1 LED/PLD indicates power is applied to the PLD (LED on)
- Insure J3 (external CLOCK line from J1) is open, not LOADED, DRIVEN, or shorted;
- Insure SW5 (LEFT: CUSTOM 441, RIGHT:STANDARD 442) select is set to the LEFT (bypassing SW2, SEL[3:0]. Note LED will light for “CUSTOM FREQUENCIES”.
- Set SW4, SW6, and SW7 rocker switches to desired P, M, and N programming values: UP =0 LOGIC LOW (LED indicator OFF); DOWN = 1 LOGIC HIGH (LED indicator ON).
- Load program values by depressing momentary switch SW8, or send a pulse signal through J13 SMA connector (when installed) with standard LVTTL/LVCMOS levels.

B. External SDI

- See datasheet DC Table, AC Table, as well as Figures 5 and 6.
- To use the SDI serial data input port, generate and input SCLOCK, SDATA, and SLOAD signals with standard LVTTL/LVCMOS levels. The SCLOCK signal will sample the information presented on SDATA line. Values are loaded and indexed into a 18 bit shift register. The register shifts once per rising edge of the SCLOCK input. The serial input SDATA bits must each meet setup and hold

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SLOAD pulse Low to HIGH rising edge transition transfers the data from the SHIFT register to the LATCH register. The SLOAD Pulse HIGH to LOW transition will lock the new data values into the LATCH register.

7. **Output Enable ON:** Switch SW1 (DOWN) or externally HIGH through J11 to enable the output after setup. LED D3 indicator will be ON to indicate an enabled output.

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APPENDIX 1: DEVICE AND BOARD INFORMATION

SEE CURRENT DATASHEET

DEVICE PINS:

| Pin # | Pin Name | I/O | Open Pin Default | Type | Function |
|-------|-----------|--------|------------------|----------|--|
| | 441 | | | | |
| 1 | GND | Supply | | | Negative Power Supply (Ground) |
| 2 | NC | | | | No Connect |
| 3 | VCCPLL | Supply | | | Positive supply for the PLL and is connected to +3.3 V |
| 4 | NC | | | | No Connect |
| 5 | NC | | | | No Connect |
| 6 | GND | Supply | | | Negative Power Supply (Ground) |
| 7 | XTAL2 | Input | | | Crystal Oscillator Interface – Crystal Input |
| 8 | CLK/XTAL1 | Input | | CMOS/TTL | Crystal Oscillator Interface – Crystal Input or External Clock Input |
| 9 | GND | Supply | | | Negative Power Supply (Ground) |
| 10 | NC | | | | No Connect |
| 11 | VCC | Supply | | | Positive Power Supply |
| 12 | VCC | Supply | | | Positive Power Supply |
| 13 | VCC | Supply | | | Positive Power Supply |
| 14 | NC | | | | No Connect |
| 15 | SLOAD | Input | L | CMOS/TTL | Serial Load Input |
| 16 | SDATA | Input | L | CMOS/TTL | Serial Data Input |
| 17 | SCLOCK | Input | L | CMOS/TTL | Serial Clock Input |
| 18 | GND | Supply | | | Negative Power Supply (Ground) |
| 19 | GND | Supply | | | Negative Power Supply (Ground) |
| 20 | LOCKED | Output | | CMOS/TTL | PLL Locked Indicator |
| 21 | OE | Input | H | CMOS/TTL | Synchronous Output Enable. Active HIGH. The Enable is synchronous to the output clock to eliminate the possibility of runt pulses on the CLKOUT outputs. |
| 22 | CLKOUT | Output | | LVPECL | Differential Clock Output |
| 23 | CLKOUT | Output | | LVPECL | Differential Clock Output |
| 24 | VCC | Supply | | | Positive Power Supply |

Board Pins

Input Clock: An SMA connector (J1) board trace to CLK/XTAL1 device pin contains a gap placed on the board trace at the crystal pin (J5). This board trace and connector are open and not connected to the crystal pin and has no impedance affect on the crystal pin. A short must bridge this gap to connect the INPUT CLOCK SMA to the device CLK/XTAL1 pin. A 50 Ω termination resistor may be added from the board trace from CLK to SMAGND at the SMA connector, or, install a 50 Ω resistor in place of C6.

SW4, 6 and 7 are the M, N, and P SELECT: DIP switches JP1 is an LED power supply jumper provided to disable the LED's and their current. Disabling the LEDs will allow measuring only the device power supply current.

Output CLOCK and Output CLOCK: The outputs have equal length board traces with SMA connectors, J2 & J4. Use matched cables to connect the outputs to an oscilloscope or frequency counter. Alternative connection pads are supplied for installation of a Thevenin termination scheme.

Serial Pins (NB4N441) SCLOCK, SDATA and SLOAD pins have board traces connected to SMA connectors J10, J9 and J7 for external control. There are no 50 Ω termination resistors on these nodes. If signal sources requiring output termination are needed to drive SCLOCK, SDATA and SLOAD, a 50 Ω resistor can be added, from the board trace at the SMA conductor to SMA ground.

Output Enable: The Output Enable function is carried out manually with the switch, SW1, or externally via SMA connector J11, and observing the OUTPUT CLOCK & OUTPUT CLOCK CLKOUT pins.

PLL LOCKED There are two convenient PLL indicator LEDs, green for when the device is PLL LOCKED and red for PLL not LOCKED.

LED/PLD Power: The LED and PLD power can be disabled by leaving JP1 open or removing shunt from JP1.

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APPENDIX 2: SCHEMATICS

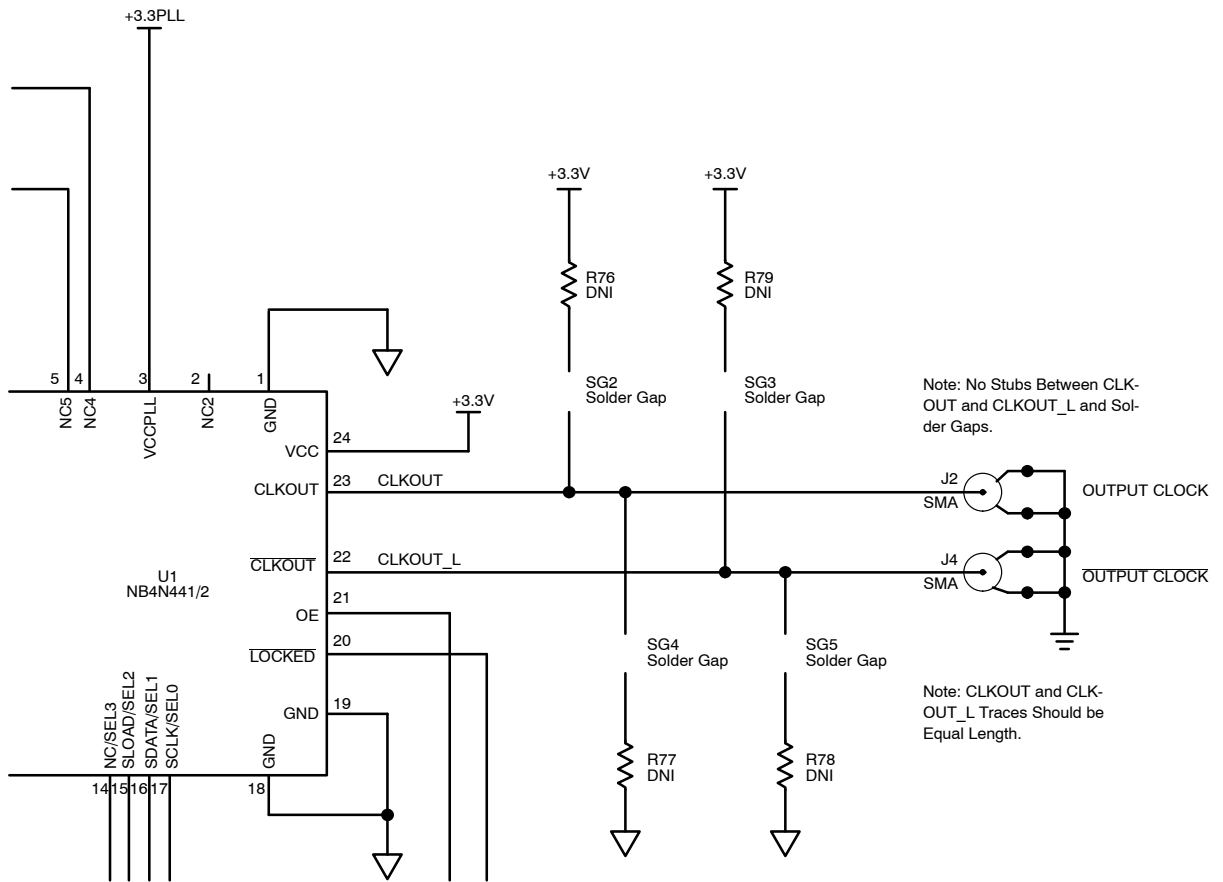


Figure 3. Outputs

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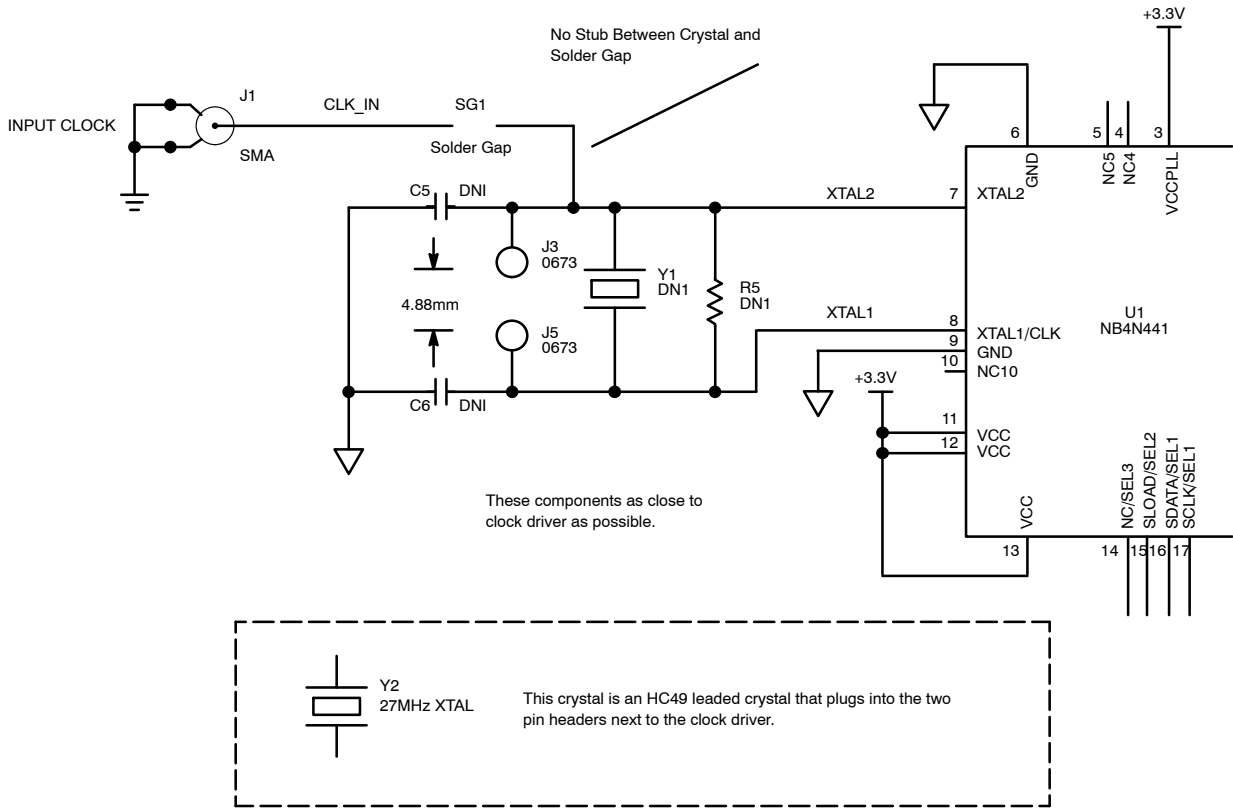


Figure 4. Input Clock and Crystal

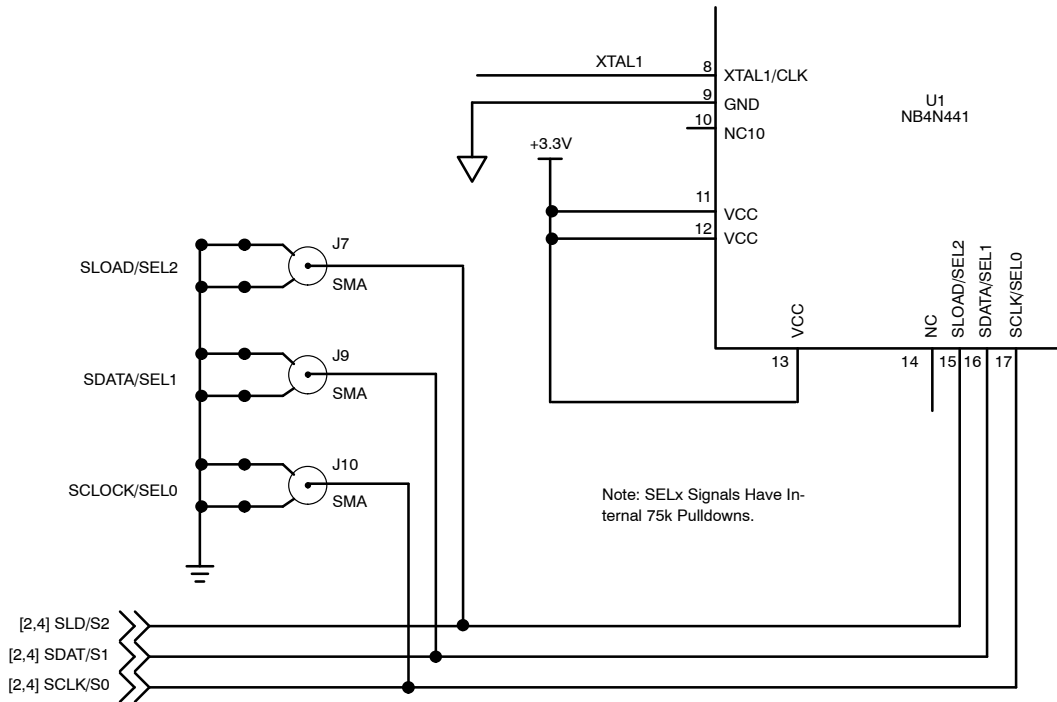


Figure 5. SDI Inputs

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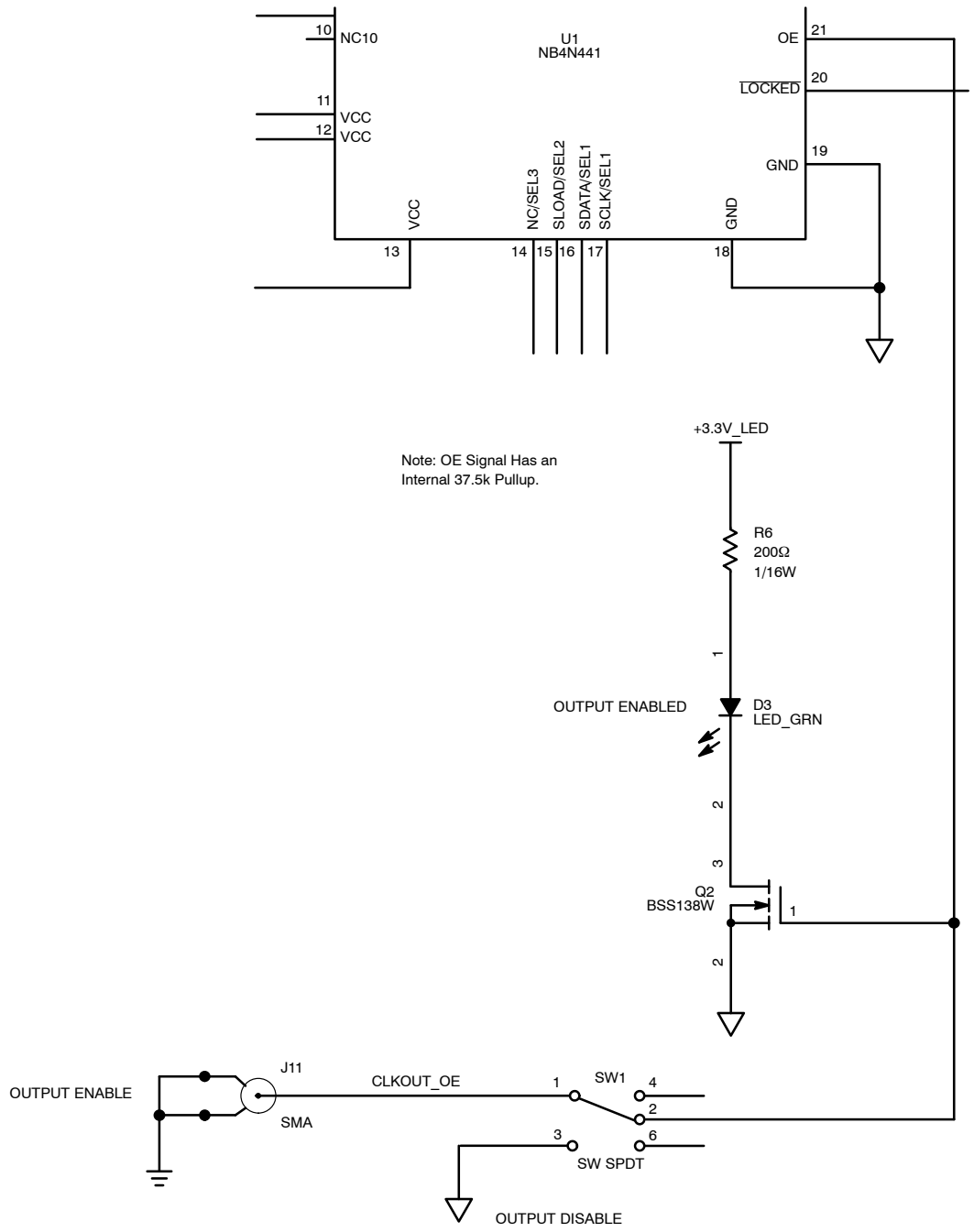


Figure 6. Output Enable

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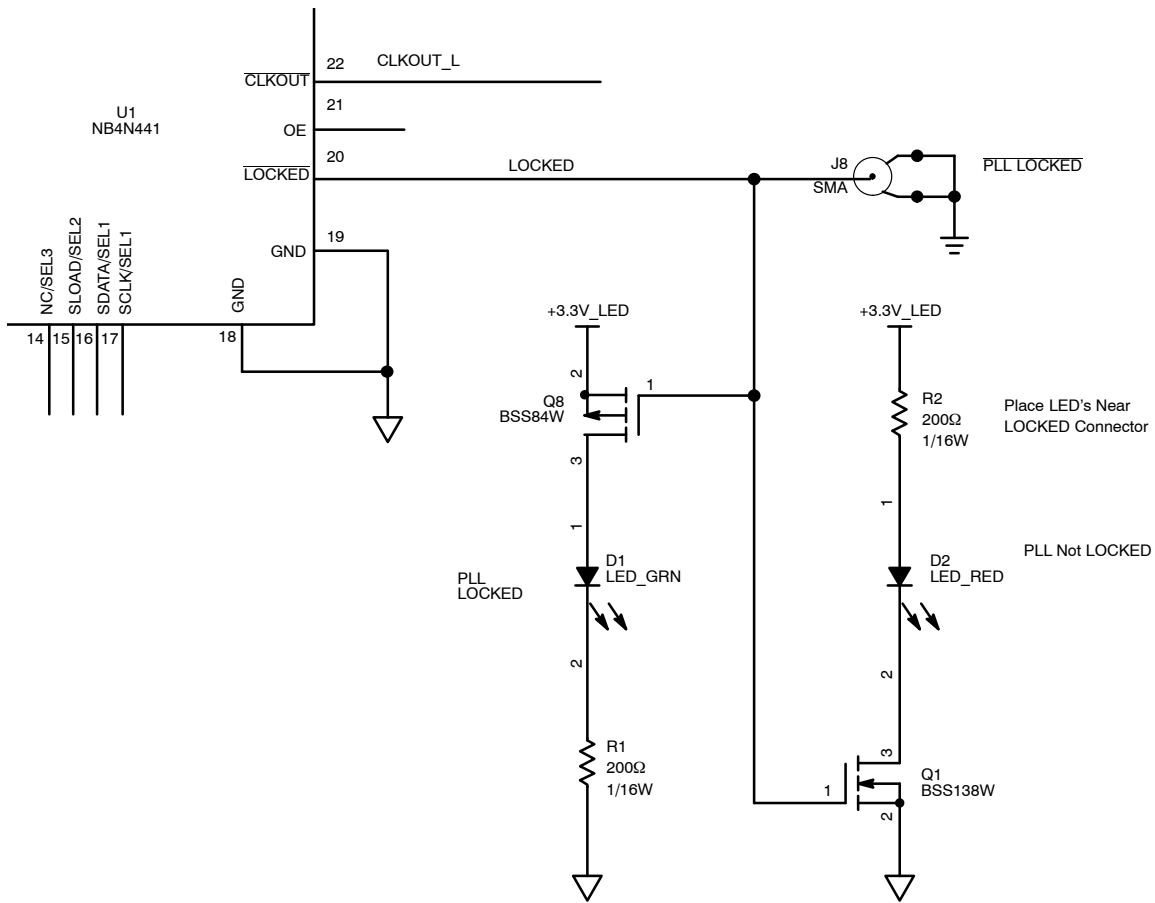


Figure 7. Output LOCKED/Not LOCKED

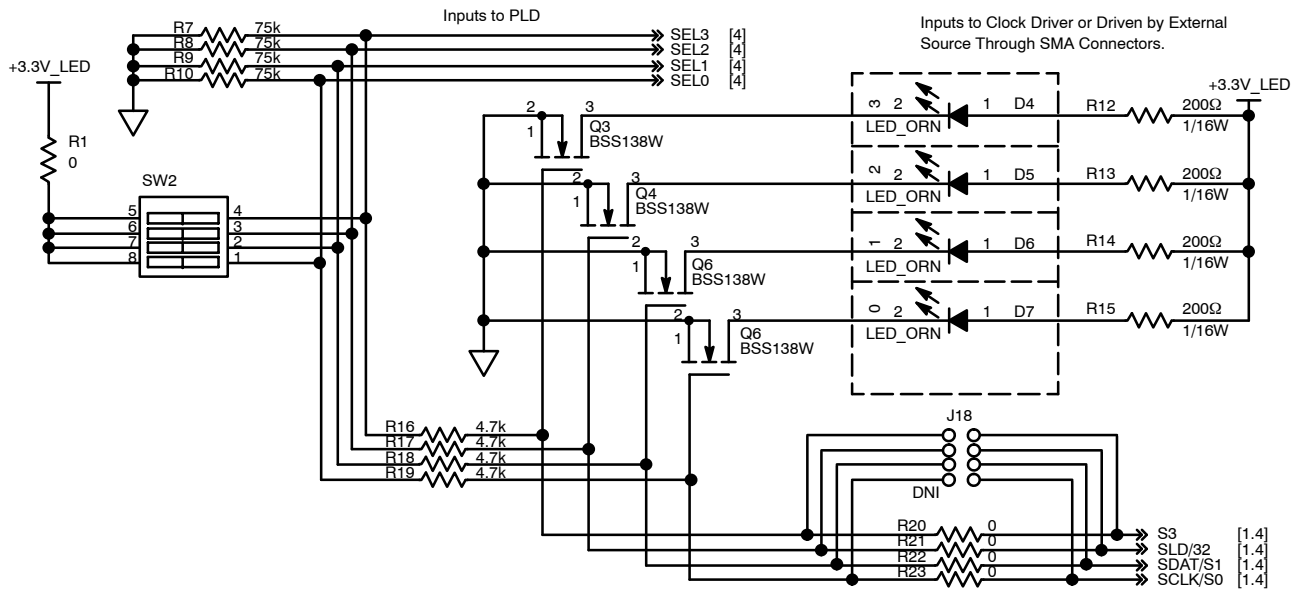


Figure 8. Inputs to PLD

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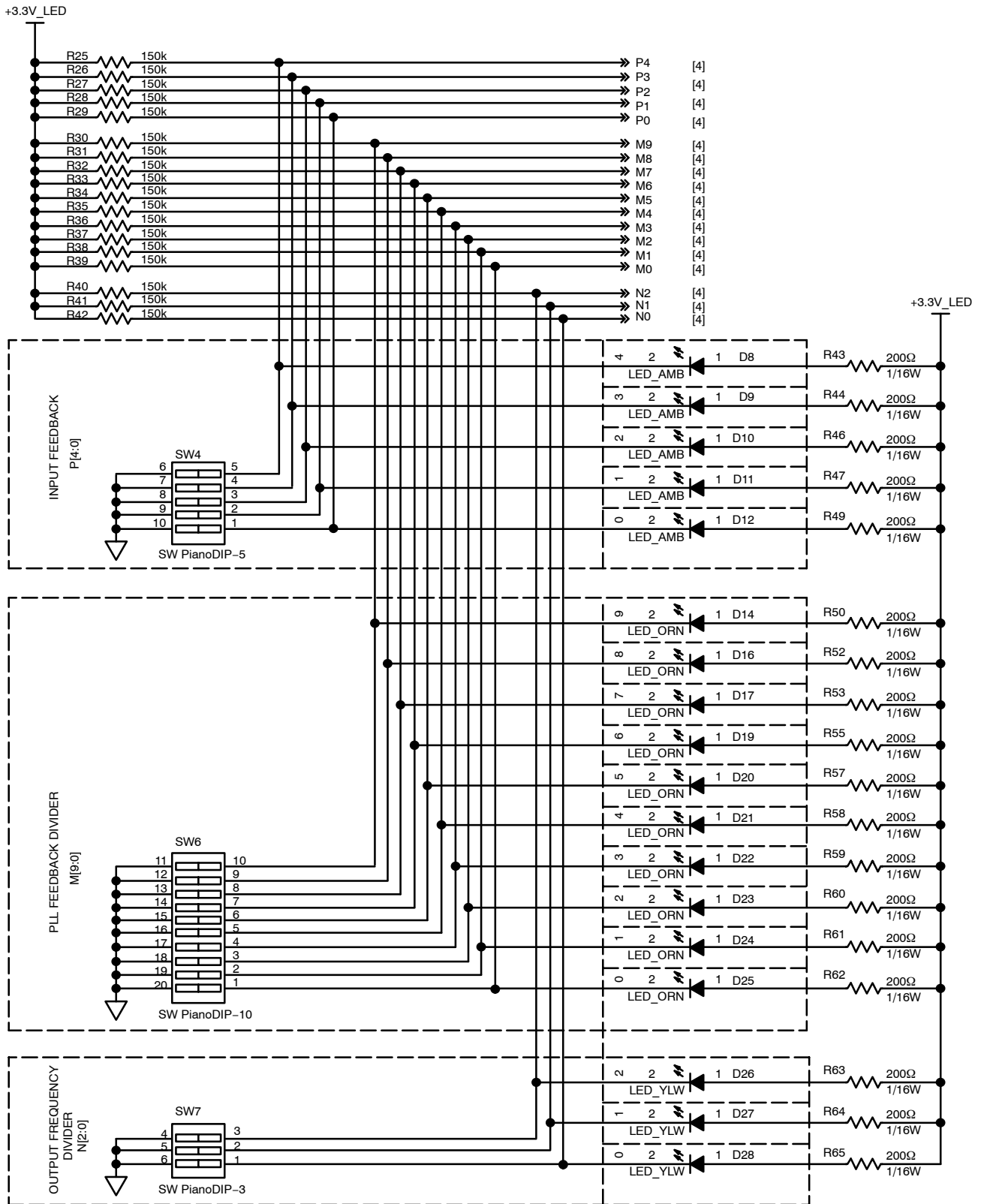


Figure 9. Switches and LED

NB4N441MNGEVB

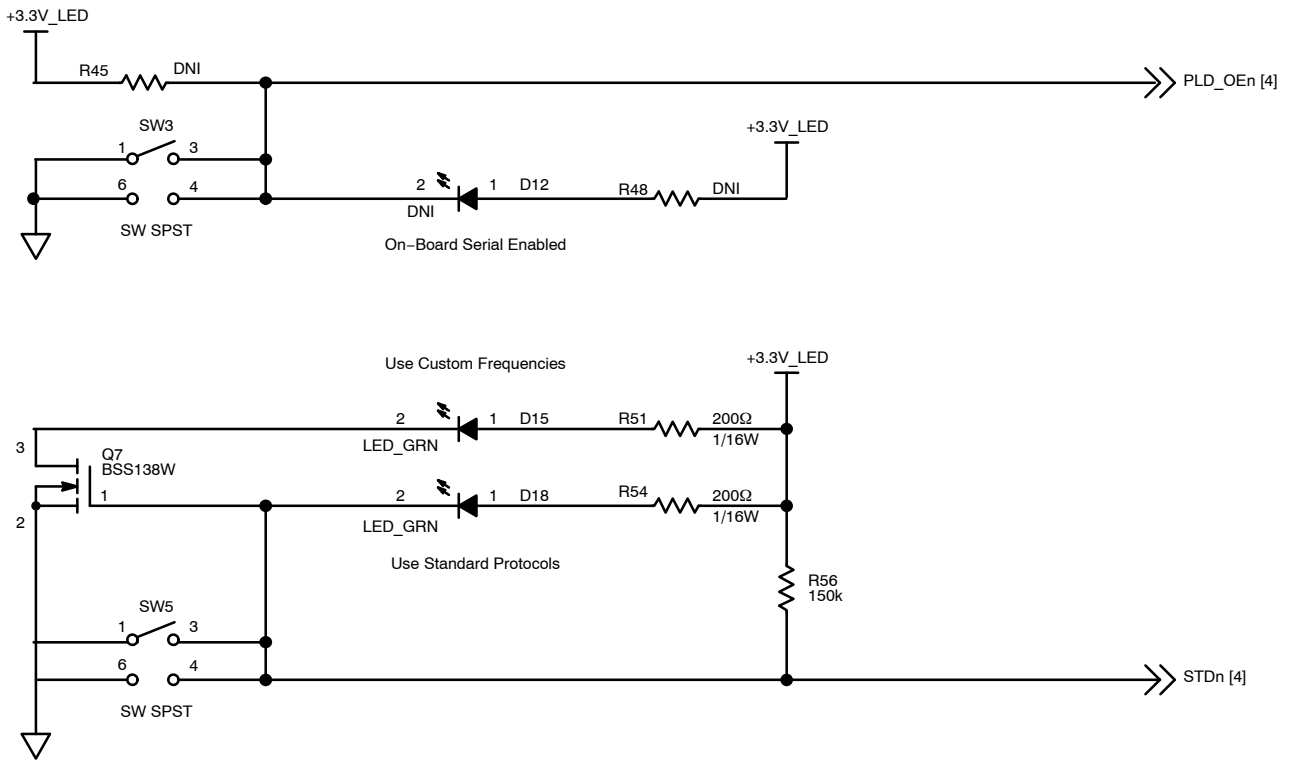


Figure 10. Output Enable

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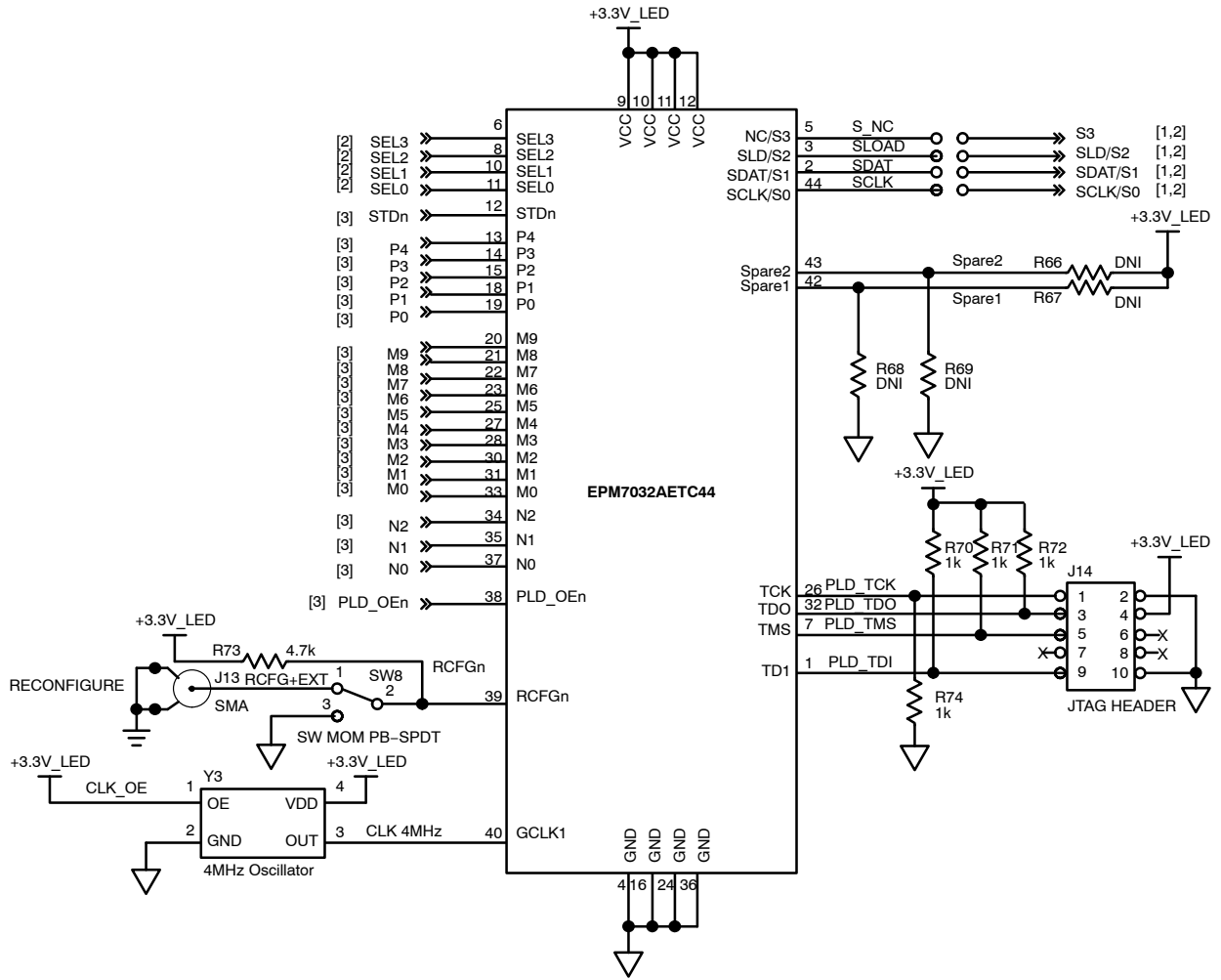


Figure 11. PLD

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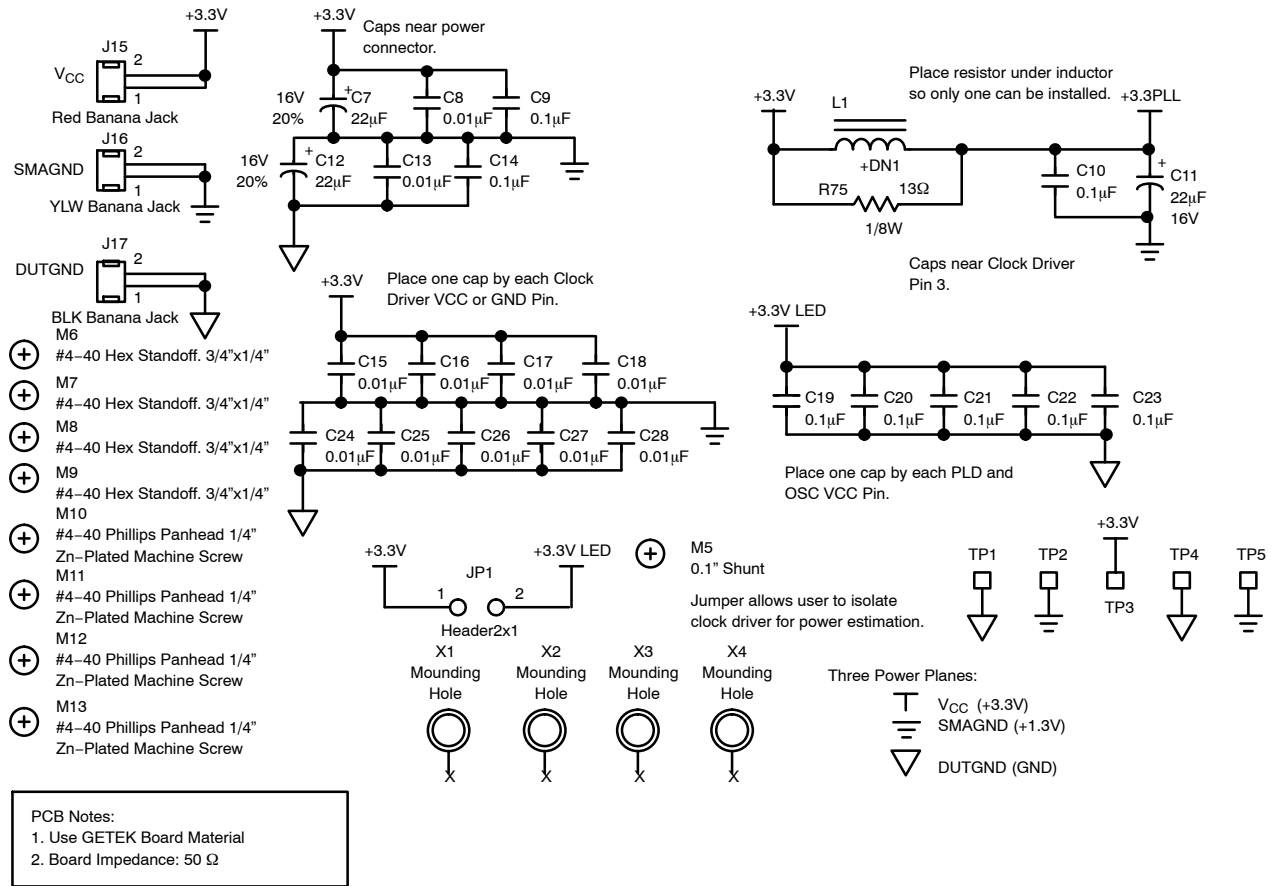


Figure 12. Power and Hardware

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APPENDIX 3: BILL OF MATERIALS, LAMINATION STACKUP, AND ASSEMBLY NOTES

| Item | Mfg Part # | Description | Manufacturer | Reference | Vendor Part # | Vendor | Qty |
|------|-------------------------|---|--------------------|--|----------------|------------------|-----|
| 1 | | DNI | | C1,C2,R3,C3,R4,C4,R5,C5,C6,R45,R48,R66,R67,R68,R69,R76,R77,R78,R79 | | | 19 |
| 2 | T494D226K016AS | 22 μ F | Kemet | C7,C11,C12 | 399-1782-1-ND | Digikey | 3 |
| 3 | C0603C103K5RACTU | 0.01 μ F | Kemet | C8,C10,C13,C15,C16,C17,C18,C24,C25,C26,C27,C28 | 399-1091-1-ND | Digikey | 12 |
| 4 | ECJ-1VB1C104K | 0.1 μ F | Panasonic | C9,C14 | PCC1762CT-ND | Digikey | 2 |
| 5 | ECJ-1VB1C104K | 0.1 μ F | Panasonic | C19,C20,C21,C22,C23 | PCC1762CT-ND | Digikey | 5 |
| 6 | LTST_C190GKT | LED_GRN | Lite-On | D3,D1 | 160-1183-1-ND | Digikey | 2 |
| 7 | LTST_C190CKT | LED_RED | Lite-On | D2 | 160-1181-1-ND | Digikey | 1 |
| 8 | LTST_C190EKT | LED_ORN | Lite-On | D4,D5,D6,D7 | 160-1182-1-ND | Digikey | 4 |
| 9 | LTST_C190AKT | LED_AMB | Lite-On | D8,D9,D10,D11,D13 | 160-1180-1-ND | Digikey | 5 |
| 10 | | DNI | | D12 | | | 1 |
| 11 | LTST_C190EKT | LED_ORN | Lite-On | D14,D16,D17,D19,D20,D21, D22,D23,D24,D25 | 160-1182-1-ND | Digikey | 10 |
| 12 | LTST_C190GKT | LED_GRN | Lite-On | D15,D18 | 160-1183-1-ND | Digikey | 2 |
| 13 | LTST_C190YKT | LED_YLW | Lite-On | D26,D27,D28 | 160-1184-1-ND | Digikey | 3 |
| 14 | 22-03-2021 | Header2x1 | Molex | JP1 | WM4000-ND | Digikey | 1 |
| 15 | 142-0701-801 | SMA | Johnson Components | J1,J2,J4,J7,J8,J9,J10,J11 | J502-ND | Digikey | 8 |
| 16 | 0673-0-15-01-30-02-10-0 | 0673 | Mill-Max | J3,J5 | | | 2 |
| 17 | 142-0701-801 | SMA | Johnson Components | J6 | J502-ND | Digikey | 1 |
| 18 | 10-89-1081 | 8-pin Header | Molex | J12 | WM6808-ND | Digikey | 1 |
| 19 | 142-0701-801 | SMA | Johnson Components | J13 | J502-ND | Digikey | 1 |
| 20 | 10-89-1101 | JTAG HEADER | Molex | J14 | WM6810-ND | Digikey | 1 |
| 21 | 571-0500 | RED BANANA JACK | Deltron | J15 | 150-039 | Farnell / Newark | 1 |
| 22 | 571-0700 | YLW BANANA JACK | Deltron | J16 | 150-043 | Farnell / Newark | 1 |
| 23 | 571-0100 | BLK BANANA JACK | Deltron | J17 | 150-040 | Farnell / Newark | 1 |
| 24 | 10-89-1081 | DNI | Molex | J18 | WM6808-ND | Digikey | 1 |
| 25 | CDRH74-102MC | DNI | Sumida | L1 | 308-1197-1-ND | Digikey | 1 |
| 26 | 382811-5 | 0.1" Shunt | AMP/Tyco | M1,M2,M3,M4 | A26229-ND | Digikey | 4 |
| 27 | 382811-5 | 0.1" Shunt | AMP/Tyco | M5 | A26229-ND | Digikey | 1 |
| 28 | 1895 | #4-40 Hex Standoff, 3/4"x1/4" | Keystone | M6,M7,M8,M9 | 1895K-ND | Digikey | 4 |
| 29 | PMS 440 0025 PH | #4-40 Phillips Panhead 1/4" Zn-plated Machine Screw | Building Fasteners | M10,M11,M12,M13 | H342-ND | Digikey | 4 |
| 30 | 50-000-00306 | 24 LD QFN GCI Flex Socket | M&M Specialties | M14 | 50-000-00306 | M&M Specialties | 1 |
| 31 | BSS138W-7 | BSS138W | Diodes Inc. | Q1,Q2,Q3,Q4,Q5,Q6 | BSS138WDICT-ND | Digikey | 6 |
| 32 | BSS138W-7 | BSS138W | Diodes Inc. | Q7 | BSS138WDICT-ND | Digikey | 1 |
| 33 | BSS84W-7 | BSS84W | Diodes Inc. | Q8 | 621-BSS84W | Mouser | 1 |
| 34 | ERJ-3GEYJ221V | 200 Ω | Panasonic | R1,R2,R6,R12,R13,R14,R15 | P220GCT-ND | Digikey | 7 |

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| Item | Mfg Part # | Description | Manufacturer | Reference | Vendor Part # | Vendor | Qty |
|------|----------------------|-----------------|------------------|---|------------------|---------|-----|
| 35 | ERJ-3GEYJ753V | 75k | Panasonic | R7,R8,R9,R10 | P75KGCT-ND | Digikey | 4 |
| 36 | ERJ-3GEY0R00V | 0.0 | Panasonic | R11 | P0.0GCT-ND | Digikey | 1 |
| 37 | ERJ-3GEYJ472V | 4.7k | Panasonic | R16,R17,R18,R19 | P4.7KGCT-ND | Digikey | 4 |
| 38 | ERJ-3GEY0R00V | 0.0 | Panasonic | R20,R21,R22,R23 | P0.0GCT-ND | Digikey | 4 |
| 39 | ERJ-3GEY0R00V | 0.0 | Panasonic | R24 | P0.0GCT-ND | Digikey | 1 |
| 40 | ERJ-3GEYJ154V | 150k | Panasonic | R25,R26,R27,R28,R29,R30,R31,R32,R33,R34,R35,R36,R37,R38,R39,R40,R41,R42,R56 | P150KGCT-ND | Digikey | 19 |
| 41 | ERJ-3GEYJ221V | 200Ω | Panasonic | R43,R44,R46,R47,R49,R50,R51,R52,R53,R54,R55,R57,R58,R59,R60,R61,R62,R63,R64,R65 | P220GCT-ND | Digikey | 20 |
| 42 | ERJ-3GEYJ102V | 1K | Panasonic | R70,R71,R72,R74 | P1.0KGCT-ND | Digikey | 4 |
| 43 | ERJ-3GEYJ472V | 4.7k | Panasonic | R73 | P4.7KGCT-ND | Digikey | 1 |
| 44 | ERJ-6GEYJ130V | 13Ω | Panasonic | R75 | P13ACT-ND | Digikey | 1 |
| 45 | GT11MSCKETR | SW SPDT | C&K | SW1 | CKN1099CT-ND | Digikey | 1 |
| 46 | 76PSB04 | SW DIP-4 | Grayhill | SW2 | GH1215-ND | Digikey | 1 |
| 47 | | DNI | | SW3 | | | 1 |
| 48 | 76PSB05 | SW PianoDIP-5 | Grayhill | SW4 | GH1216-ND | Digikey | 1 |
| 49 | GT12MSCKETR | SW SPST | C&K | SW5 | CKN1100CT-ND | Digikey | 1 |
| 50 | 76PSB10 | SW PianoDIP-10 | Grayhill | SW6 | GH1221-ND | Digikey | 1 |
| 51 | 76PSB03 | SW PianoDIP-3 | Grayhill | SW7 | GH1214-ND | Digikey | 1 |
| 52 | EP12SD1SAKE | SW MOM PB-SPDT | C&K | SW8 | CKN4056CT-ND | Digikey | 1 |
| 53 | 5015 | TP_SMT_KEYSTONE | Keystone | TP1,TP2,TP3,TP4,TP5 | 5015KCT-ND | Digikey | 5 |
| 54 | NB4N441 | NB4N441 | ON Semiconductor | U1 | | | 1 |
| 55 | EPM7032AETC44-10 | EPM7032AETC44 | Altera | U2 | EPM7032AETC44-10 | Arrow | 1 |
| 56 | | Mounting Hole | | X1,X2,X3,X4 | | | 4 |
| 57 | HCM49-21.47727MABJT | DNI | Citizen | Y1 | 300-6143-1-ND | Digikey | 1 |
| 58 | HC49US27.000MABJ | 27MHz XTAL | Citizen | Y2 | 300-6050-ND | Digikey | 1 |
| 59 | CSX750FBC4.000000MTR | 4MHz Oscillator | Citizen | Y3 | 300-7232-1-ND | Digikey | 1 |

NB4N441MNGEVB

LAMINATION STACK

- L1 Signal
- L2 SMAGND
- L3 V_{CC} and DUTGND
- L4 DUTGND and Signal

| LAMINATION DIAGRAM | | | | | |
|-------------------------------|------------|------------------|----------------------|----------------|-------------|
| Layer Number | Layer Name | Copper Thickness | Dielectric Thickness | Layer Material | Trace Width |
| 1 | TOP | 1/2 OZ. | | | 0.012 |
| | | | 0.006 | GETEK | |
| 2 | SMAGND | 1 OZ. | | | --- |
| | | | Adjust | GETEK | |
| 3 | PWR | 1 OZ. | | | --- |
| | | | 0.006 | GETEK | |
| 4 | DUTGND | 1/2 OZ. | | | 0.011 |
| FINISHED PCB THICKNESS TO BE: | | | 0.64 ±0.003 | | |

ASSEMBLY NOTES:

Notes (Unless Otherwise Specified)

Material:

- GETEK Laminate Epoxy/Polyphenylene Oxide Resin Type NEMA FR-4 (IPC-L-1088/04). See Layer Table. Inner Layers: 1 oz. Copper clad
Outer Layers: 1/2 oz. Copper Foil Plated to 1 1/2 oz finished.
- Refer to Stacking Diagram for Finished Board Thickness.

Tooling:

- Photo etch circuitry per artwork drill locations controlled by drill file.drl fabrication print.
- The dielectric thickness of the controlled impedance layers is for reference only. Final acceptance shall be determined by these layer pairs having a characteristic impedance of $52.5 \Omega \pm 10\%$. The vendor can make width adjustments on only the critical conductor widths of ± 0.0005 . All other adjustments must have prior approval from Baldwin Tech Layer Grouping (1.2).
- Finished conductor width to be 0.012".

Finish:

- Plating Specification: Electrodeposited hard gold plate, Type 1 (99.7% min gold) Grade C (Knoop Hardness 130-200), Class 1 (50-100 micro-inches thick) in accordance with MIL-G-4520C and ANSI/IPC-A-6000. Section 4.0 (surface plating acceptability requirements), Class 3 (50-100

micro-inches thick) over electrodeposited nickel plate in accordance with ANSI/IPC-A-6000, Section 4.0, Class 3 (200-600 micro-inches thick).

- Drill sizes are finished. Plated through holes to have a minimum barrel plating of 0.0008 in.
- Board twist and warp not to exceed 0.005 in (5%) per linear inch. Front to back registration to be within 0.003 in.
- True position tolerance shall be determined by a minimum annular ring of 0.005 in.
- Plated holes shall not be rough or irregular so as to hinder proper solder wicking.
- Soldermask: Green LPI: B0
- Apply Legend (SILKSCREEN) to both sides using a nonconductive, white, Epoxy based ink per artwork.
- No board shop logo on board.
- Each PCB shall be serialized, in legend, in the area shown, as follow: 0005-1-1 (Sequential Number (assigned per panel)-Panel Number (assigned per log)-Year and Week).

Testing:

- Final Electrical Test shall be performed per provided IPC-356 netlist. The PCB shall have a verification stamp. Connectivity to be verified against IPC format net list.
- A TDR report for each layer shall be provided by vendor at time of shipment.

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