TEXAS INSTRUMENTS

CD40192B, CD40193B Types

CMOS Presettable Up/Down Counters (Dual Clock With Reset)

High-Voltage Types (20-Volt Rating)
CD40192 – BCD Type
CD40193 – Binary Type

■ CD40192B Presettable BCD Up/Down Counter and the CD40193B Presettable Binary Up/Down Counter each consist of 4 synchronously clocked, gated "D" type flip-flops connected as a counter. The inputs consist of 4 individual jam lines, a $\overline{\text{PRESET ENABLE}}$ control, individual CLOCK UP and CLOCK DOWN signals and a master RESET. Four buffered Q signal outputs as well as $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ outputs for multiple-stage counting schemes are provided.

The counter is cleared so that all outputs are in a low state by a high on the RESET line. A RESET is accomplished asynchronously with the clock. Each output is individually programmable asynchronously with the clock to the level on the corresponding jam input when the $\overline{\text{PRESET ENABLE}}$ control is low.

The counter counts up one count on the positive clock edge of the CLOCK UP signal provided the CLOCK DOWN line is high. The counter counts down one count on the positive clock edge of the CLOCK DOWN signal provided the CLOCK UP line is high.

The $\overline{\text{CARRY}}$ and $\overline{\text{BORROW}}$ signals are high when the counter is counting up or down. The $\overline{\text{CARRY}}$ signal goes low one-half clock cycle after the counter reaches its maximum count in the count-up mode. The $\overline{\text{BORROW}}$ signal goes low one-half clock cycle after the counter reaches its minimum count in the count-down mode. Cascading of multiple packages is easily accomplished without the need for additional external circuitry by tying the $\overline{\text{BORROW}}$ and $\overline{\text{CARRY}}$ outputs to the CLOCK DOWN and CLOCK UP inputs, respectively, of the succeeding counter package.

The CD40192B and CD40193B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Individual clock lines for counting up or counting down
■ Synchronous high-speed carry and borrow propagation delays for cascading
■ Asynchronous reset and preset capability
■ Medium-speed operation—f_{CL} = 8 MHz (typ.) @ 10 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
■ Noise margin over full package temperature range:
  1 V at V_{DD} = 5 V   2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

■ Up/down difference counting
■ Multistage ripple counting
■ Synchronous frequency dividers
■ A/D and D/A conversion
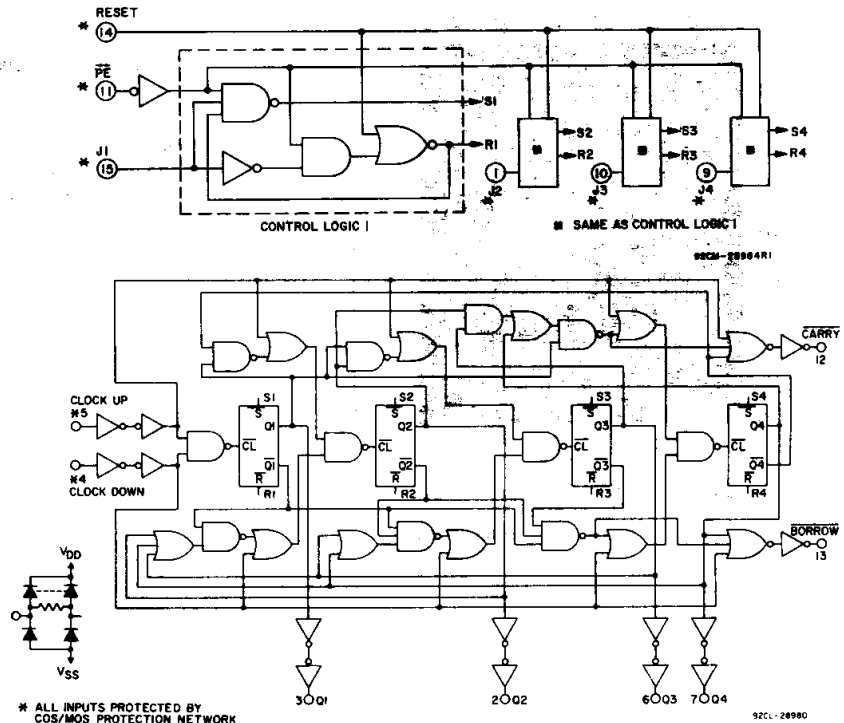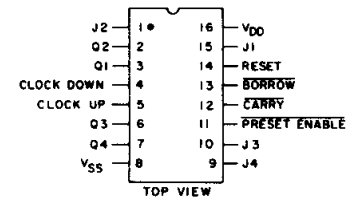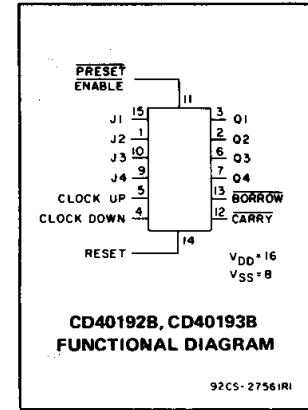■ Programmable binary or BCD counting

CD40192B, CD40193B FUNCTIONAL DIAGRAM

92CS-2756IRI

CD40192B, CD40193B TERMINAL ASSIGNMENT

92CS-27564R2

Fig. 1 — CD40192B logic diagram (BCD).
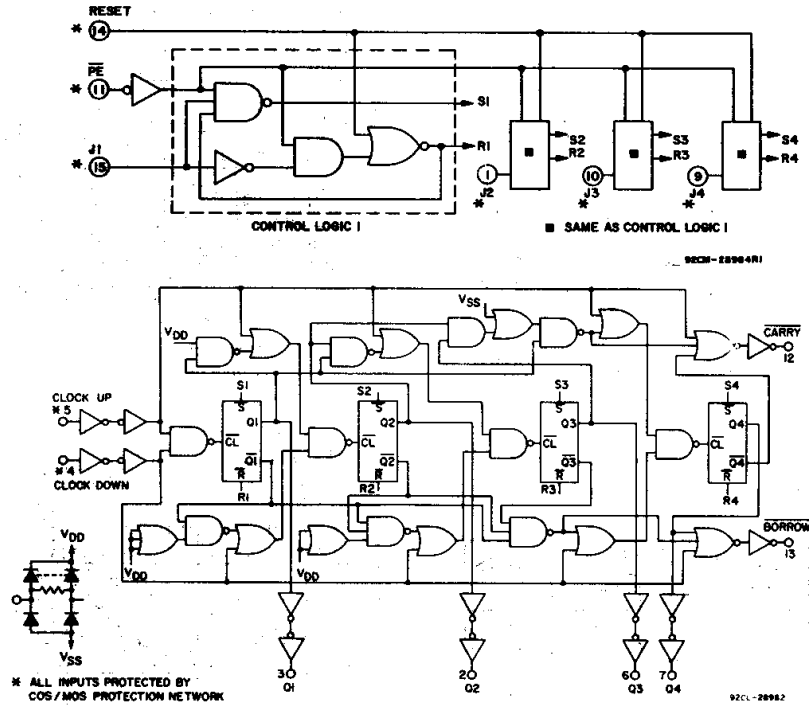
Fig. 2 — CD40193B logic diagram (binary).

Fig. 3 — CD40192B timing diagram.

Fig. 4 — Internal logic of Flip-flop.
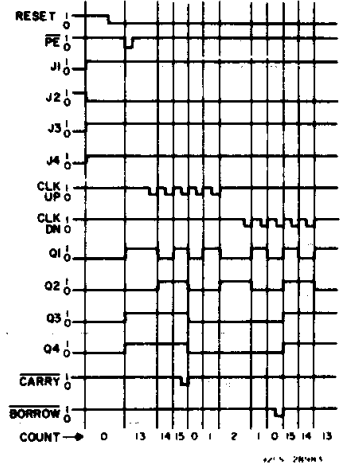
Fig. 5 — CD40193B timing diagram.

TRUTH TABLE

CLOCK UP	CLOCK DOWN	PRESET ENABLE	RESET	ACTION
⤒	1	1	0	COUNT UP
⤓	1	1	0	NO COUNT
1	⤒	1	0	COUNT DOWN
1	⤓	1	0	NO COUNT
X	X	0	0	PRESET
X	X	X	1	RESET

1 = HIGH LEVEL   0 = LOW LEVEL   X = DON'T CARE

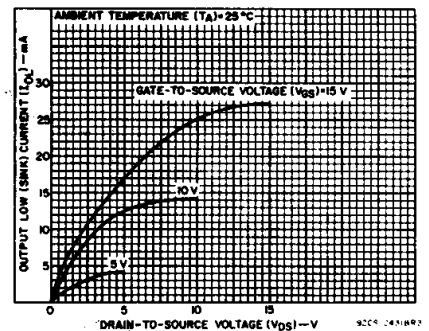
Fig. 6 — Typical output low (sink) current characteristics.

COMMERCIAL CMOS HIGH VOLTAGE ICs

3

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) .... $-0.5V$ to $+20V$

INPUT VOLTAGE RANGE, ALL INPUTS .... $-0.5V$ to $V_{DD} +0.5V$

DC INPUT CURRENT, ANY ONE INPUT .... $\pm10mA$

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^oC$ to $+100^oC$ 500mW

For $T_A = +100^oC$ to $+125^oC$ .... Derate Linearity at 12mW/^oC to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types).......... 100mW

OPERATING-TEMPERATURE RANGE (T_A) .... -55^oC to $+125^oC$

STORAGE TEMPERATURE RANGE (T_{stg}) .... -65^oC to $+150^oC$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... $+265^oC$

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^oC$ **(unless otherwise specified)**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

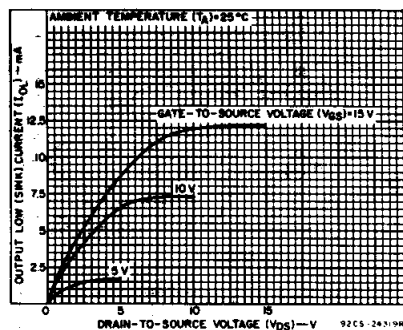| CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply Voltage Range (For T_A = Full Temp. Range)	–	3	18	V
Removal Time: RESET or $\overline{PE}$	5	80	–	ns
	10	40	–	
	15	30	–	
Pulse Width: RESET	5	480	–	ns
	10	300	–	
	15	260	–	
$\overline{PE}$	5	240	–	ns
	10	170	–	
	15	140	–	
CLOCK	5	180	–	ns
	10	90	–	
	15	60	–	
Clock Input Frequency	5	DC	2	MHz
	10		4	
	15		5.5	
Clock Rise & Fall Time	5	–	15	μs
	10	–	15	
	15	–	5	

Fig. 7 — Minimum output low (sink) current characteristics.
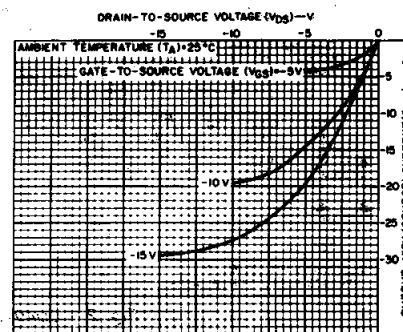

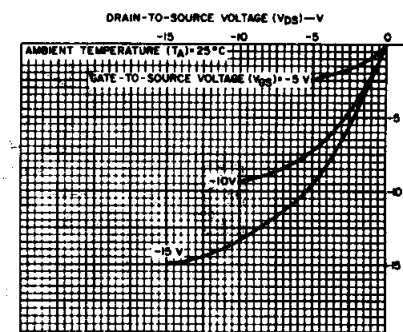Fig. 8 — Typical output high (source) current characteristics.

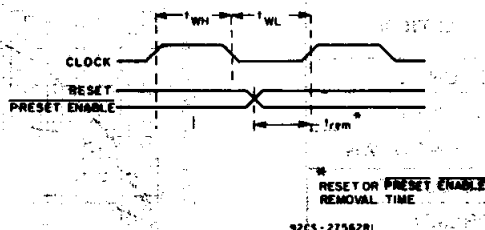Fig. 9 — Minimum output high (source) current characteristics.
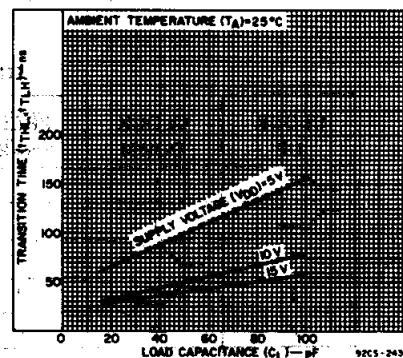

Fig. 10 — Timing diagram defining t_{rem}

Fig. 11 — Typical transition time as a function of load capacitance.

CD40192B, CD40193B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	−	0,5	5	5	5	150	150	−	0.04	5	μA
	−	0,10	10	10	10	300	300	−	0.04	10	
	−	0,15	15	20	20	600	600	−	0.04	20	
	−	0,20	20	100	100	3000	3000	−	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	−	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	−	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	−	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	−	mA
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	−	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	−	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	−	
Output Voltage: Low-Level, V_{OL} Max.	−	0,5	5	0.05				−	0	0.05	V
	−	0,10	10	0.05				−	0	0.05	
	−	0,15	15	0.05				−	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	−	0,5	5	4.95				4.95	5	−	
	−	0,10	10	9.95				9.95	10	−	
	−	0,15	15	14.95				14.95	15	−	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	−	5	1.5				−	−	1.5	V
	1, 9	−	10	3				−	−	3	
	1.5, 13.5	−	15	4				−	−	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	−	5	3.5				3.5	−	−	
	1, 9	−	10	7				7	−	−	
	1.5, 13.5	−	15	11				11	−	−	
Input Current I_{IN} Max.	−	0,18	18	±0.1	±0.1	±1	±1	−	$\pm 10^{-5}$	±0.1	μA
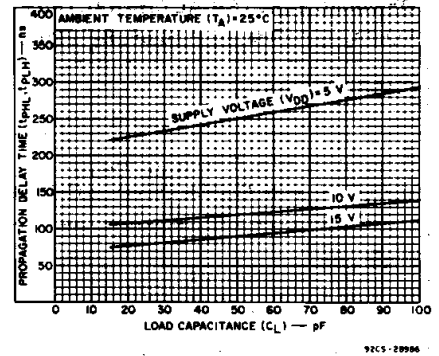
Fig. 12 — Typical propagation delay time as a function of load capacitance.
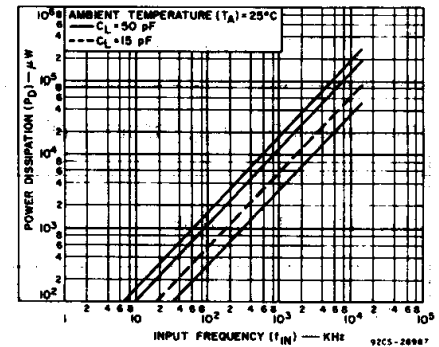
Fig. 13 — Dynamic power dissipation.

88−96
(2.235−2.438)

4−10
(0.102−0.254)

111−119
(2.819−3.022)

92CS−28930RI

Dimensions and pad layout for the CD40192BH (dimensions and pad layout for the CD40193BH are identical).

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

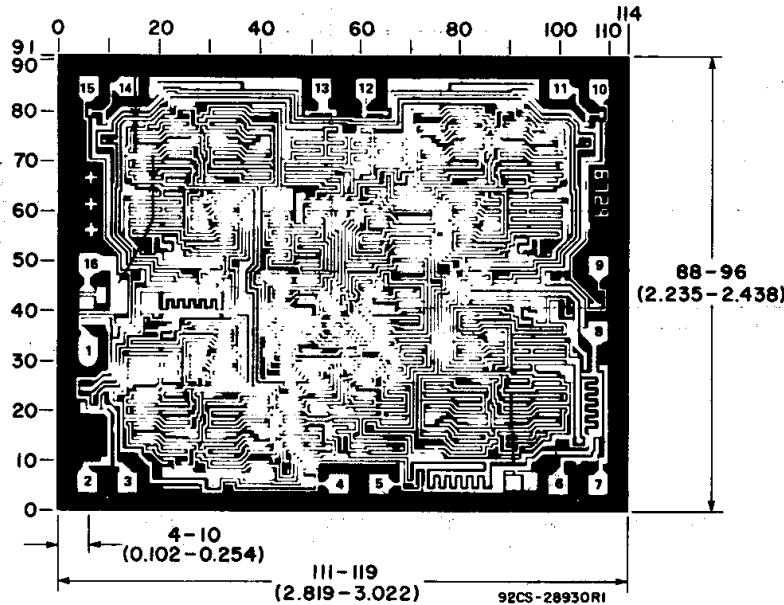| CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time t_{PHL}, t_{PLH}: CLOCK UP or CLOCK DOWN to Q, RESET to Q	5	–	250	500	ns
	10	–	120	240	
	15	–	90	180	
$\overline{PE}$ to Q	5	–	200	400	ns
	10	–	100	200	
	15	–	70	140	
CLOCK UP to $\overline{CARRY}$, CLOCK DOWN to $\overline{BORROW}$	5	–	160	320	ns
	10	–	80	160	
	15	–	60	120	
$\overline{RESET}$ or $\overline{PE}$ to $\overline{BORROW}$ or $\overline{CARRY}$	5	–	300	600	ns
	10	–	150	300	
	15	–	110	220	
Transition Time, t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Min. Removal Time, t_{rem}* RESET or $\overline{PE}$	5	–	40	80	ns
	10	–	20	40	
	15	–	15	30	
Min. Pulse Width, t_w RESET	5	–	240	480	ns
	10	–	150	300	
	15	–	130	260	
$\overline{PE}$	5	–	120	240	ns
	10	–	85	170	
	15	–	70	140	
CLOCK	5	–	90	180	ns
	10	–	45	90	
	15	–	30	60	
Max. Clock Input Frequency, f_{CL}	5	2	4	–	MHz
	10	4	8	–	
	15	5.5	11	–	
Clock Rise & Fall Time, t_r, t_f	5	–	–	15	μs
	10	–	–	15	
	15	–	–	5	
Input Capacitance, C_{IN}: RESET	–	–	10	15	pF
All Other Inputs	–	–	5	7.5	pF

* The time required for RESET or PRESET ENABLE control to be removed before clocking (see timing diagram, Fig. 10.
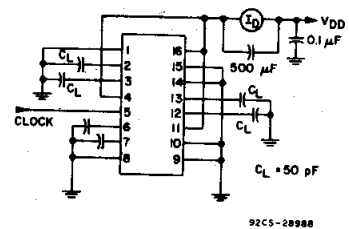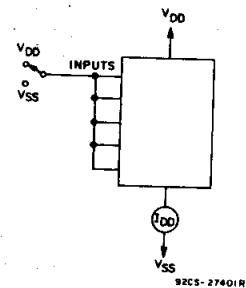

Fig. 14 – Dynamic power dissipation test circuit.
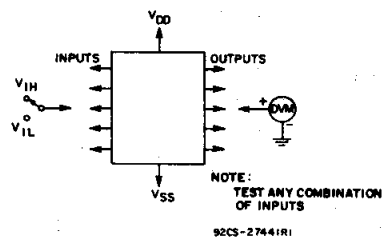

Fig. 15 – Quiescent-device-current test circuit.

Fig. 16 – Input-voltage test circuit.
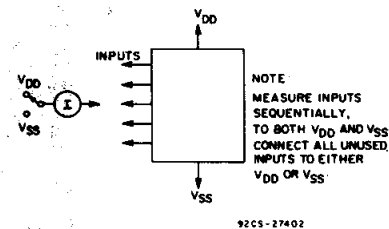

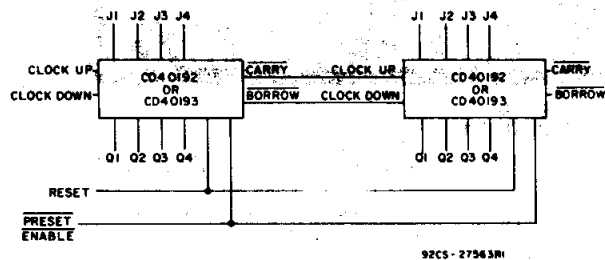Fig. 17 – Input current test circuit.

Fig. 18 – Cascaded counter packages.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD40192BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD40192BE	Samples
CD40192BF	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD40192BF	Samples
CD40192BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD40192BF3A	Samples
CD40192BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40192B	Samples
CD40193BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD40193BE	Samples
CD40193BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD40193BF3A	Samples
CD40193BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40193B	Samples
CD40193BNSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD40193B	Samples
CD40193BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0193B	Samples
CD40193BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM0193B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD40192B, CD40192B-MIL, CD40193B, CD40193B-MIL :

● Catalog : CD40192B, CD40193B

● Military : CD40192B-MIL, CD40193B-MIL

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

    ● Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD40192BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40193BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD40193BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD40192BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD40193BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD40193BPWR	TSSOP	PW	16	2000	853.0	449.0	35.0

PACKAGE MATERIALS INFORMATION

TUBE
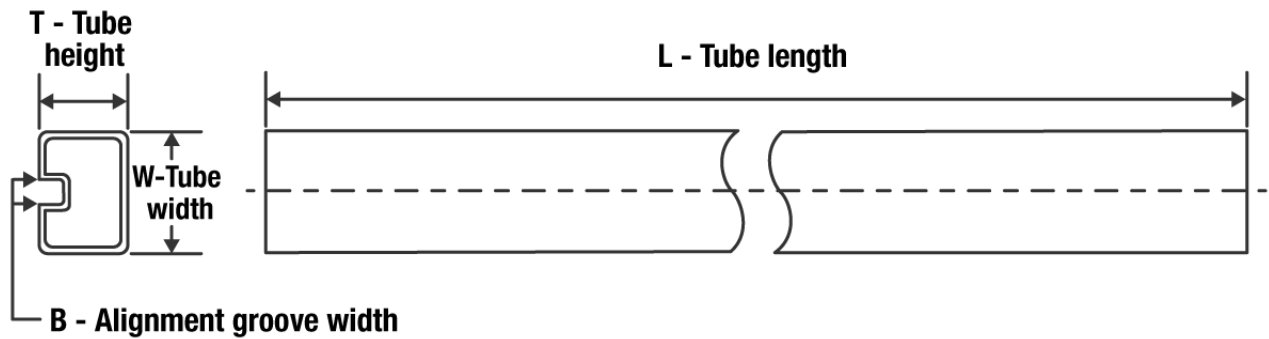
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD40192BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40192BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40193BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40193BE	N	PDIP	16	25	506	13.97	11230	4.32
CD40193BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

C

SEATING PLANE

0.1 C

8.2
7.4 TYP

A

PIN 1 ID
AREA

14X 1.27

1

16

10.4
10.0
NOTE 3

2X
8.89

8

9

B

5.4
5.2
NOTE 4

16X 0.51
0.35

⊕ 0.25Ⓜ C A B

2.00 MAX

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0.3
0.1

0° - 10°

1.05
0.55

(1.25)

DETAIL A
TYPICAL

4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE
DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS
INSTRUMENTS
www.ti.com

16X (1.85)

SYMM
℄

1

16X (0.6)

14X (1.27)

SYMM
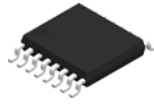℄

16

9

8

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

SEATING PLANE

PIN 1 INDEX AREA

6.6
6.2 TYP

14X 0.65

16

2X
4.55

5.1
4.9
NOTE 3

1

8

9

16X 0.30
0.19

⊕ 0.1 Ⓜ C A B

4.5
4.3
NOTE 4

C

△ 0.1 C

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0.75
0.50

0° -8°

DETAIL A
TYPICAL

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

1

16X (0.45)

SYMM

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A   02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DIM / PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package is hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.   Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option /D\

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
        /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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