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U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_PWR1  
PWR1.SchDoc

U\_Clock  
Clock.SchDoc

U\_B2B-Connectors  
B2B-Connectors.SchDoc

U\_FPGA-MISC  
FPGA-MISC.SchDoc

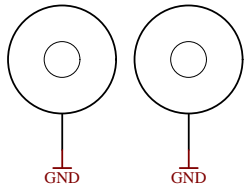
U\_PWR2  
PWR2.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

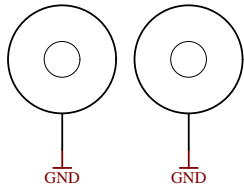
A

A

Mount.Hole 3.2mm    Mount.Hole 3.2mm



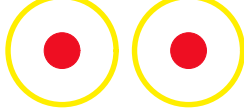
Mount.Hole 3.2mm    Mount.Hole 3.2mm



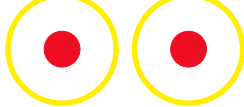
FIDU-DOT - small FIDU-DOT - small



PM1                  PM2  
FIDU-DOT - small FIDU-DOT - small



PM3                  PM4  
FIDU-DOT - small FIDU-DOT - small



PM5                  PM6

B

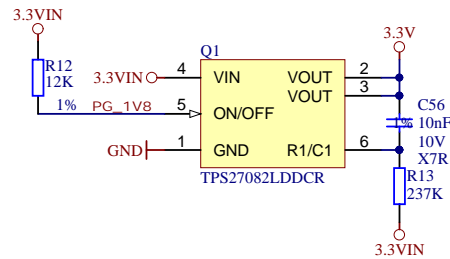
B

C

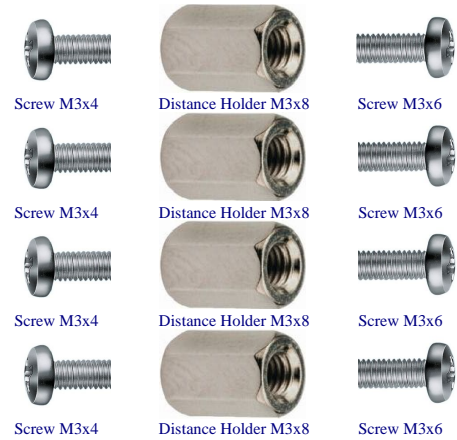
C

D

D



Top of Board



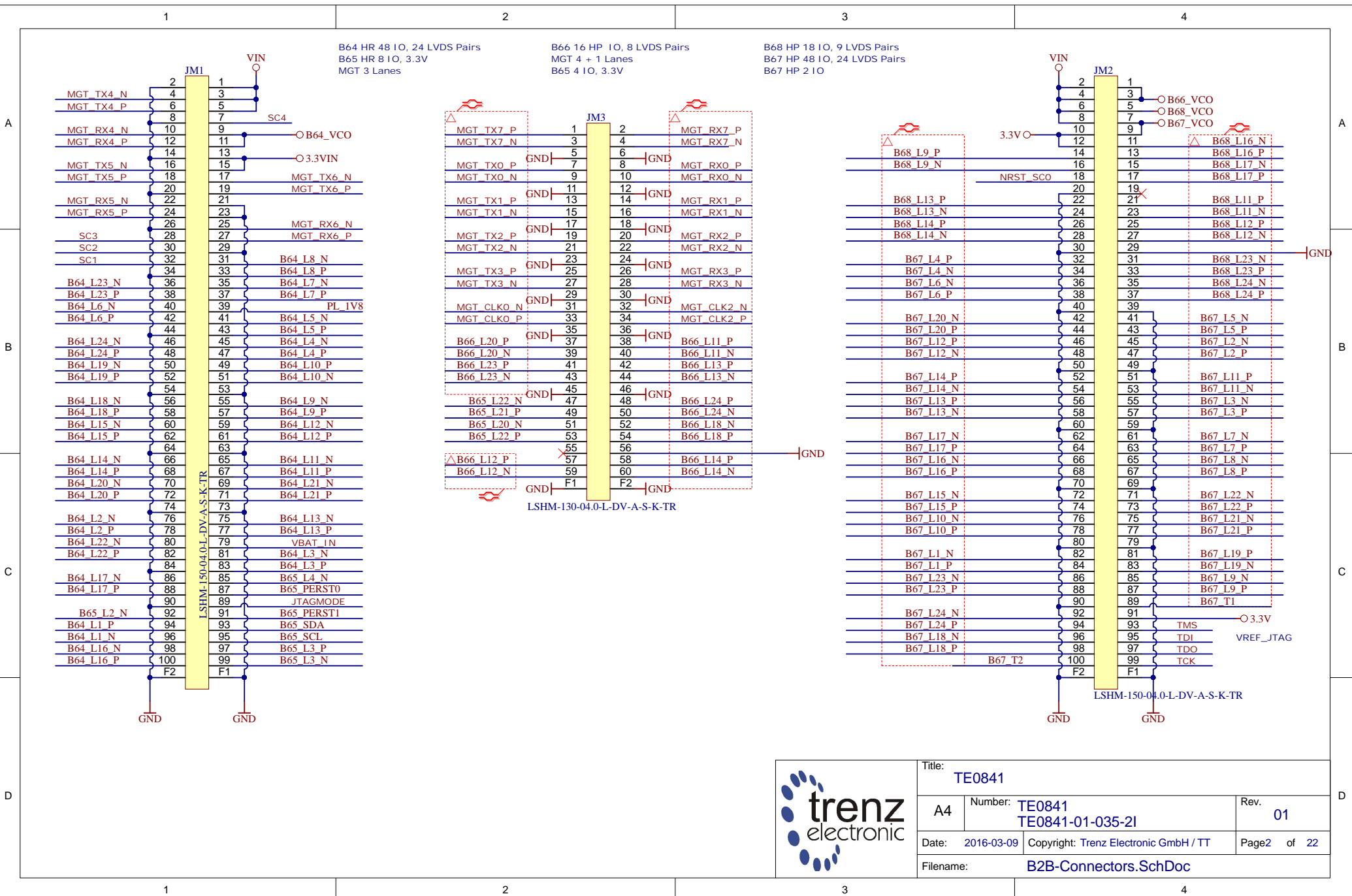
Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page1 of 22
Filename: TE0841.SchDoc		

1

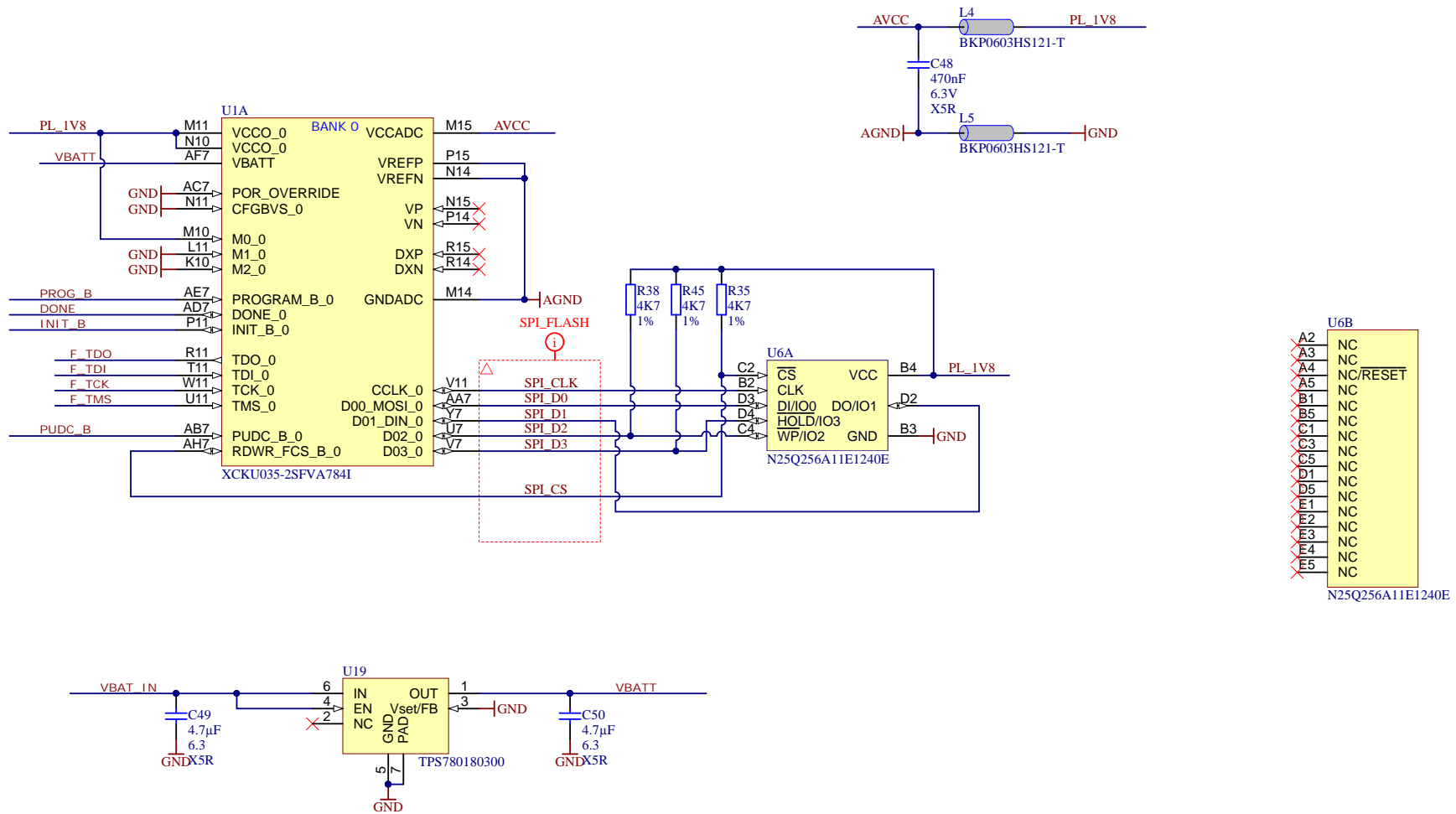

2

3

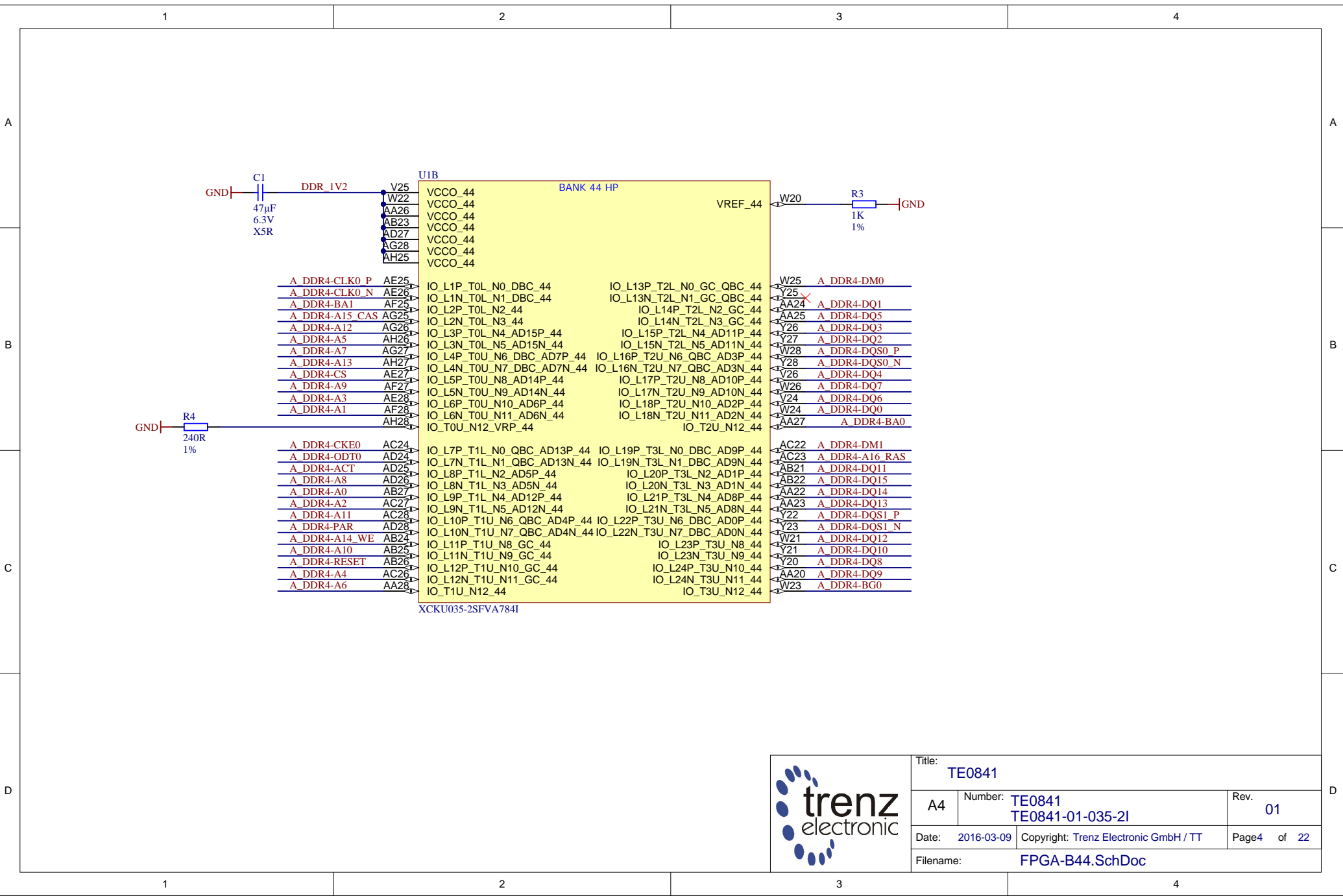
4



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page2 of 22
Filename: B2B-Connectors.SchDoc		

Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page3 of 22
Filename: FPGA-MISC.SchDoc		



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-2I	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page4 of 22
Filename: FPGA-B44.SchDoc		

1

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A

A

B

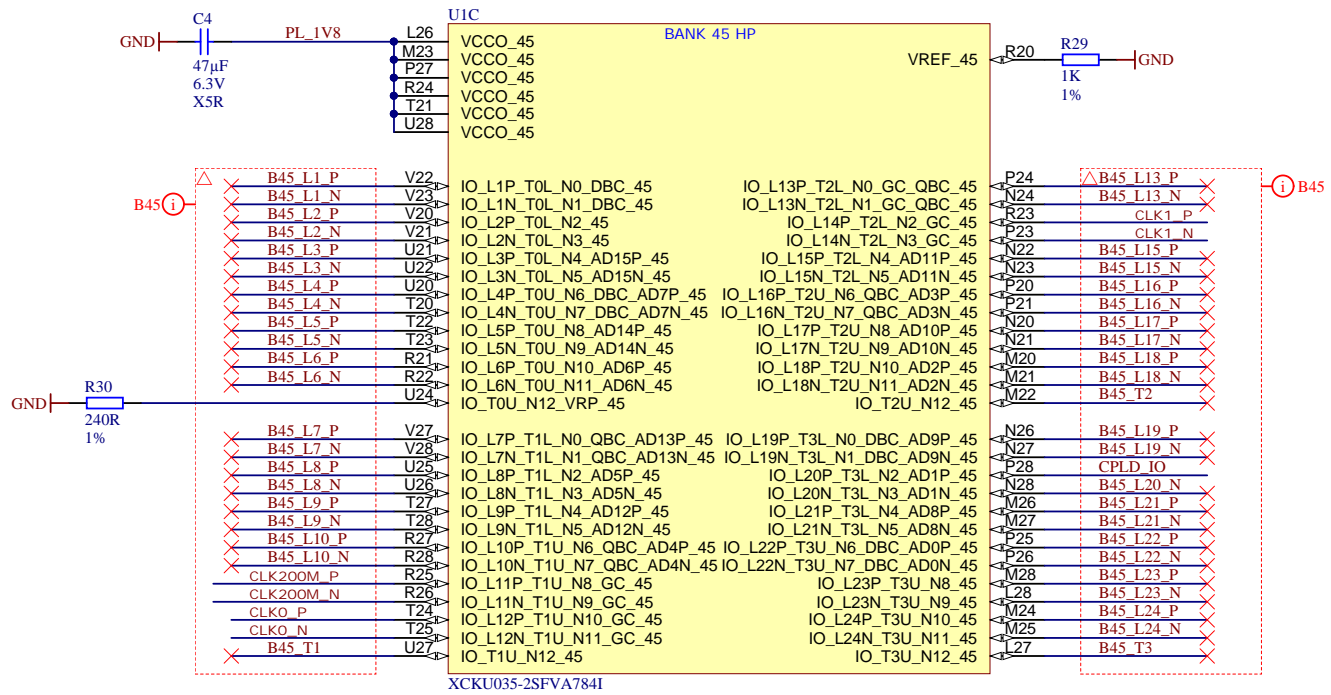
B

C

C

D

D



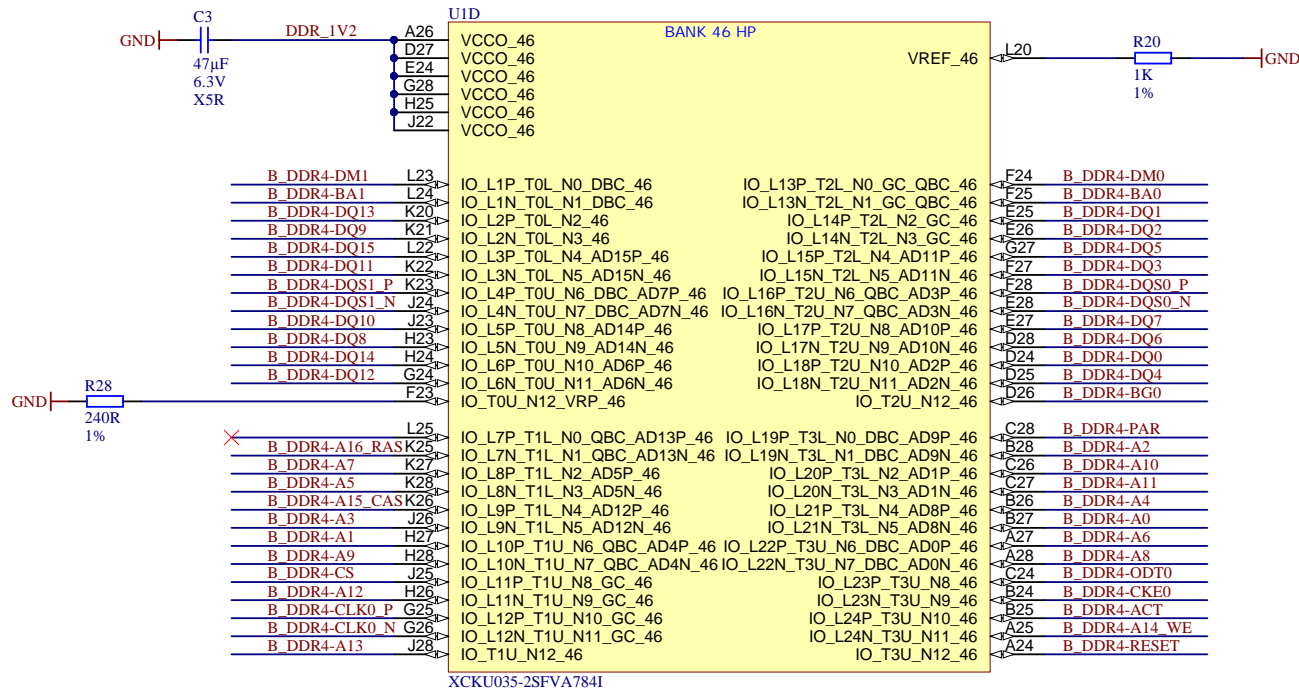
Title: TE0841		
A4	Number: TE0841 TE0841-01-035-2I	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page5 of 22
Filename: FPGA-B45.SchDoc		

1

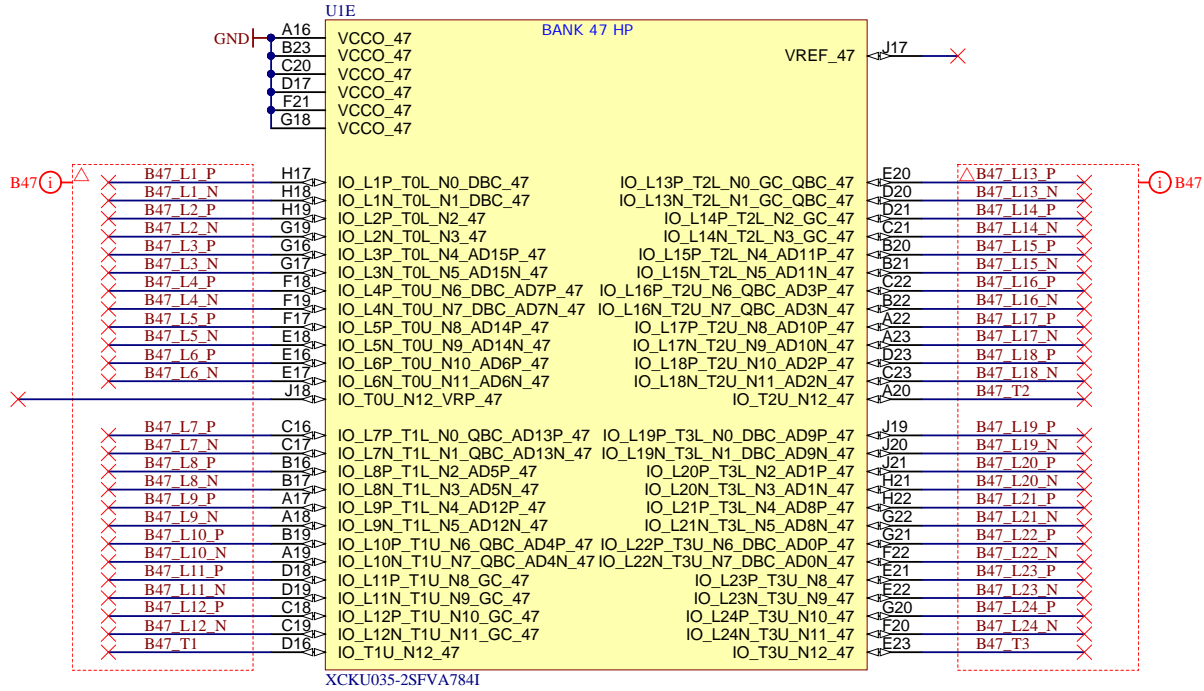
2

3

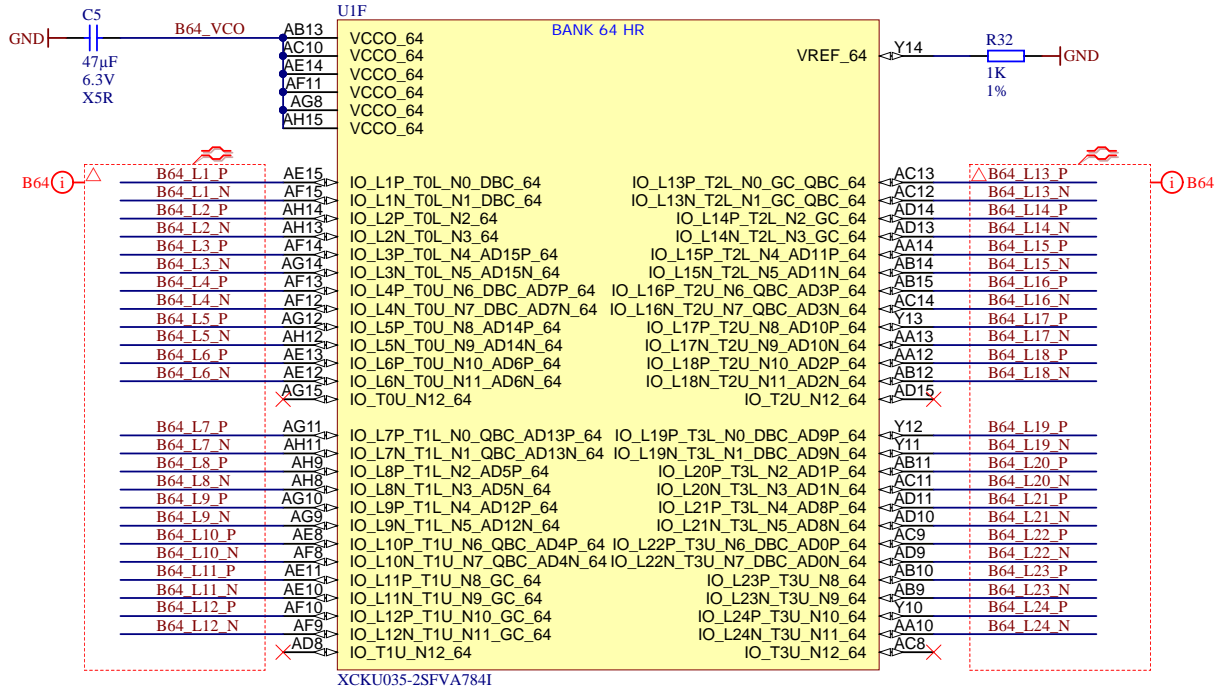

4



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page6 of 22
Filename: FPGA-B46.SchDoc		

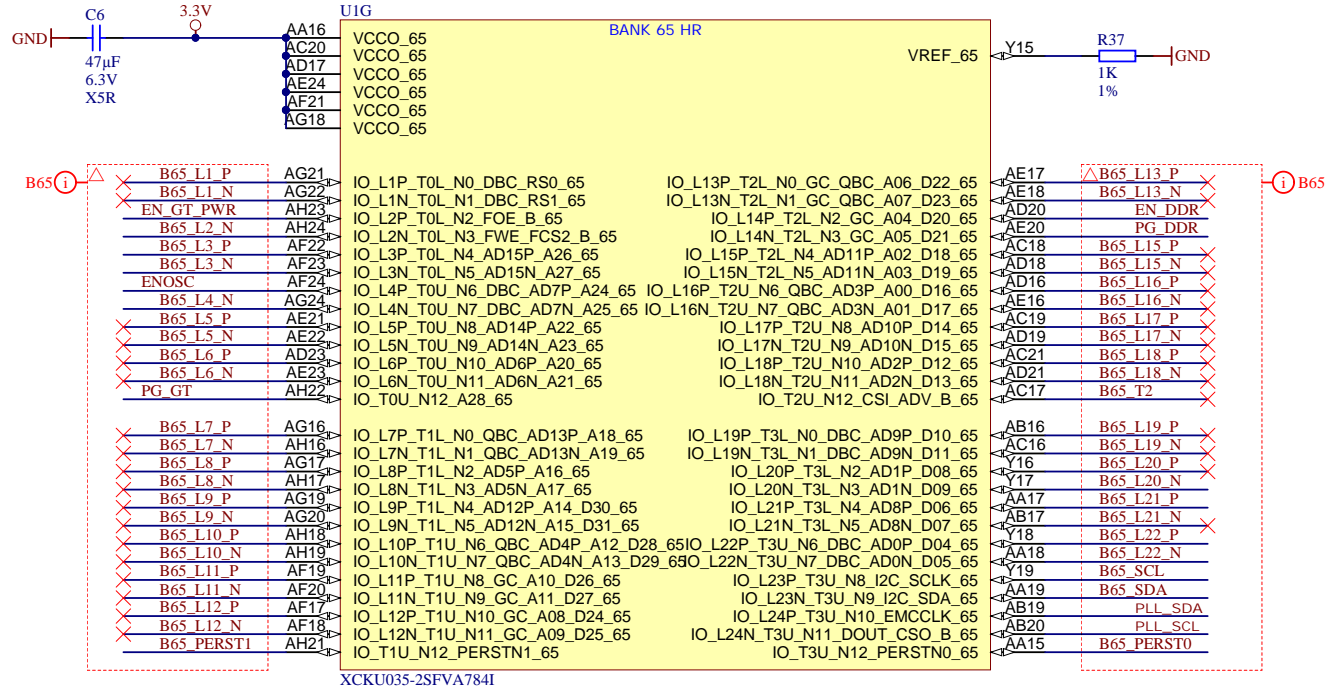


Title: TE0841		
A4	Number: TE0841 TE0841-01-035-2I	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 7 of 22
Filename: FPGA-B47.SchDoc		

Title: <b>TE0841</b>		
A4	Number: <b>TE0841</b> <b>TE0841-01-035-2I</b>	Rev. <b>01</b>
Date: <b>2016-03-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>22</b>
Filename: <b>FPGA-B64.SchDoc</b>		





XCKU035-2SFVA7841



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page9 of 22
Filename: FPGA-B65.SchDoc		

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A

A

B

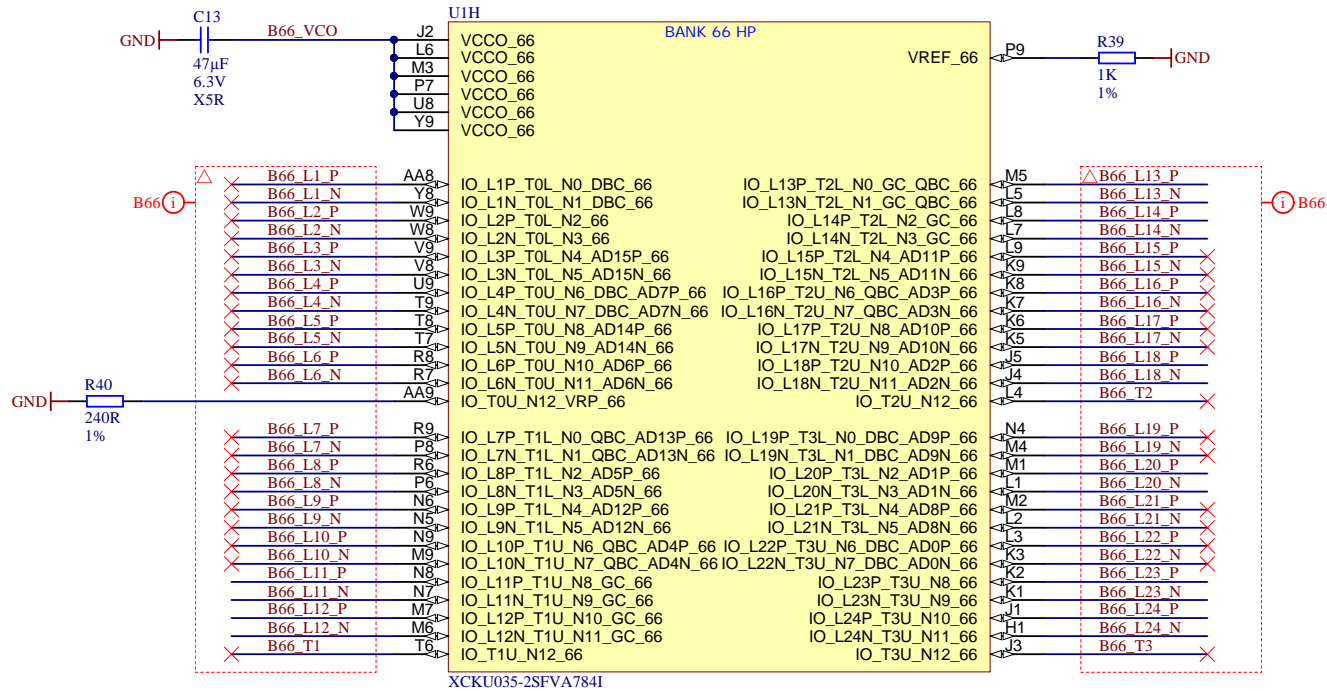
B

C

C

D

D



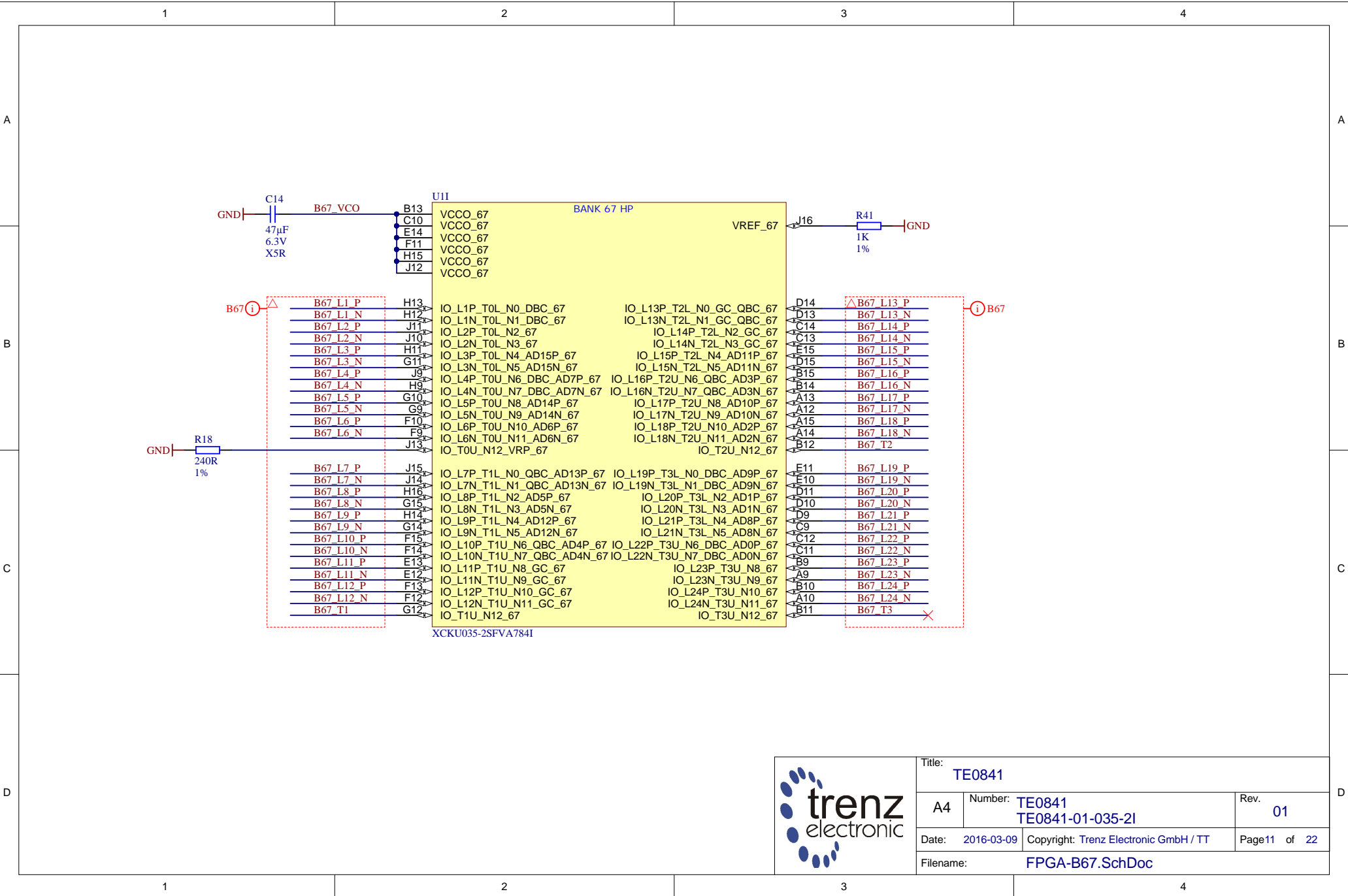
Title: <b>TE0841</b>		
A4	Number: <b>TE0841</b> <b>TE0841-01-035-2I</b>	Rev. <b>01</b>
Date: <b>2016-03-09</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>22</b>
Filename: <b>FPGA-B66.SchDoc</b>		

1

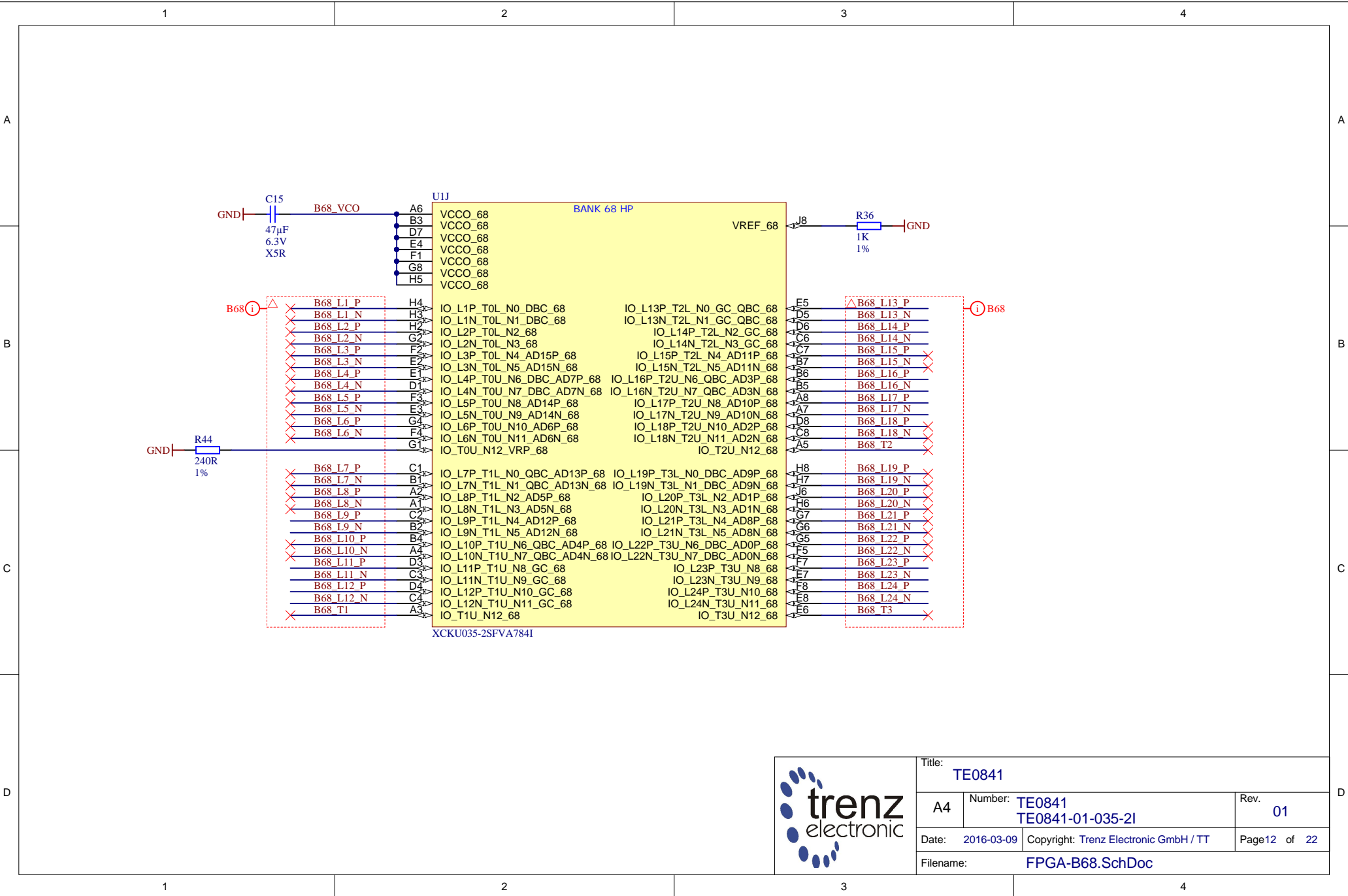
2

3

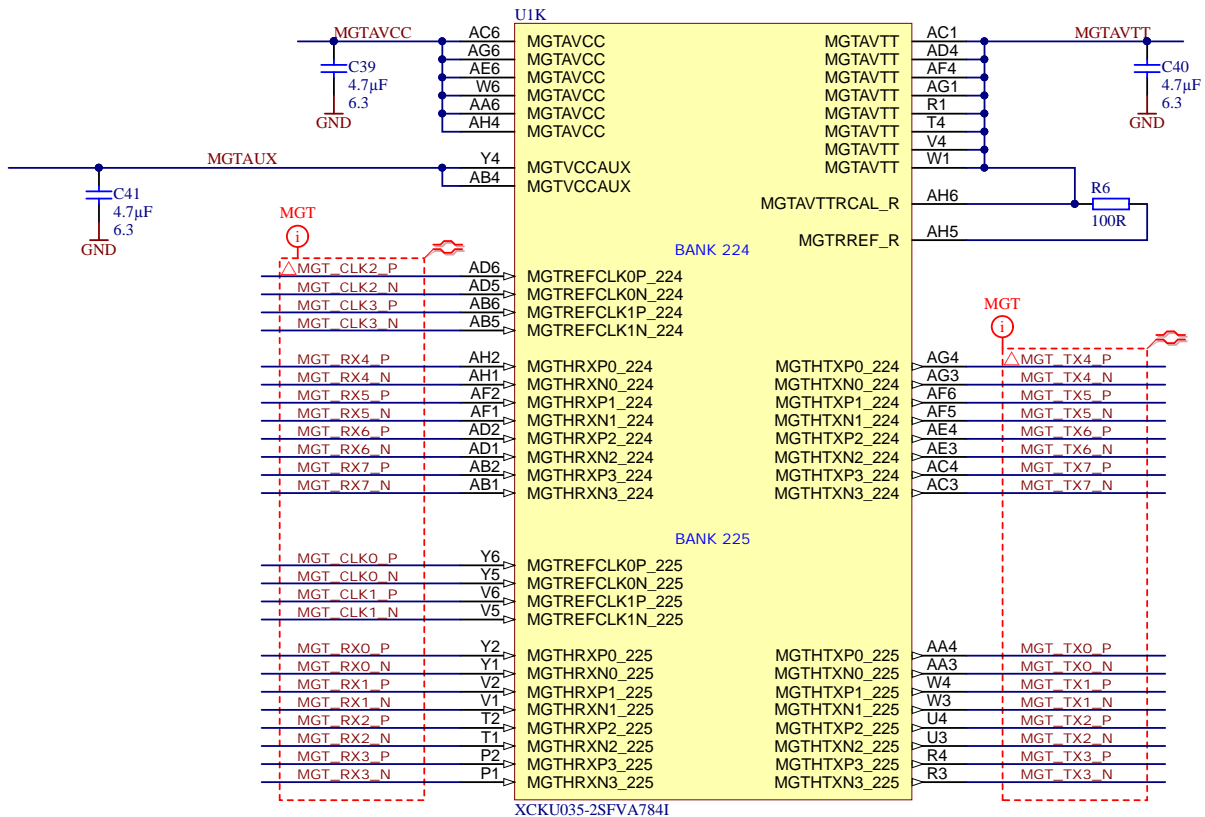
4



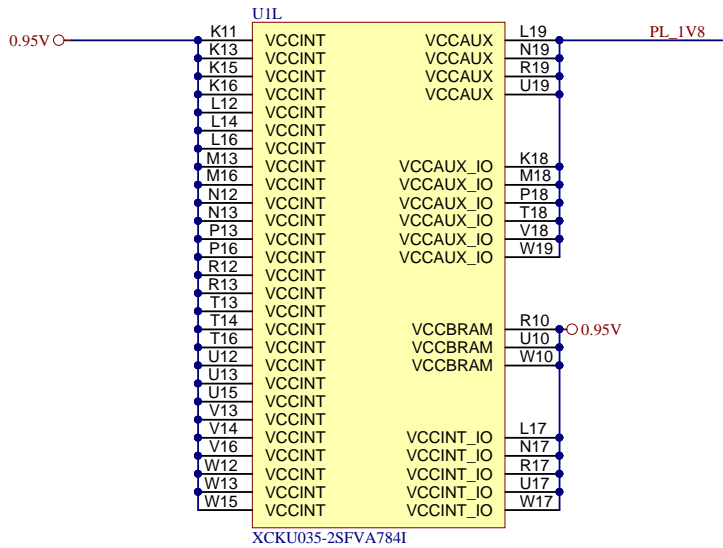
Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 11 of 22
Filename: FPGA-B67.SchDoc		



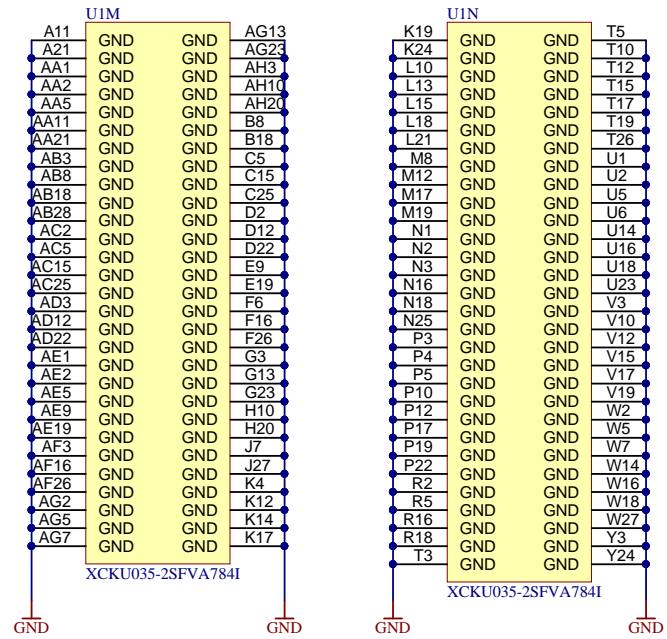
Title: TE0841		
A4	Number: TE0841 TE0841-01-035-2I	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 12 of 22
Filename: FPGA-B68.SchDoc		



	Title: TE0841	
	A4	Number: TE0841 TE0841-01-035-2I
	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT
	Filename: FPGA-MGT.SchDoc	Rev. 01

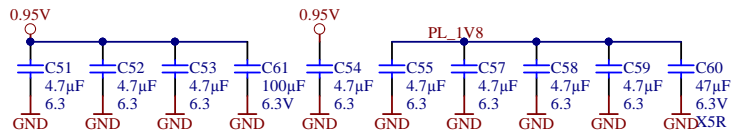


XCKU035-2SFVA784I

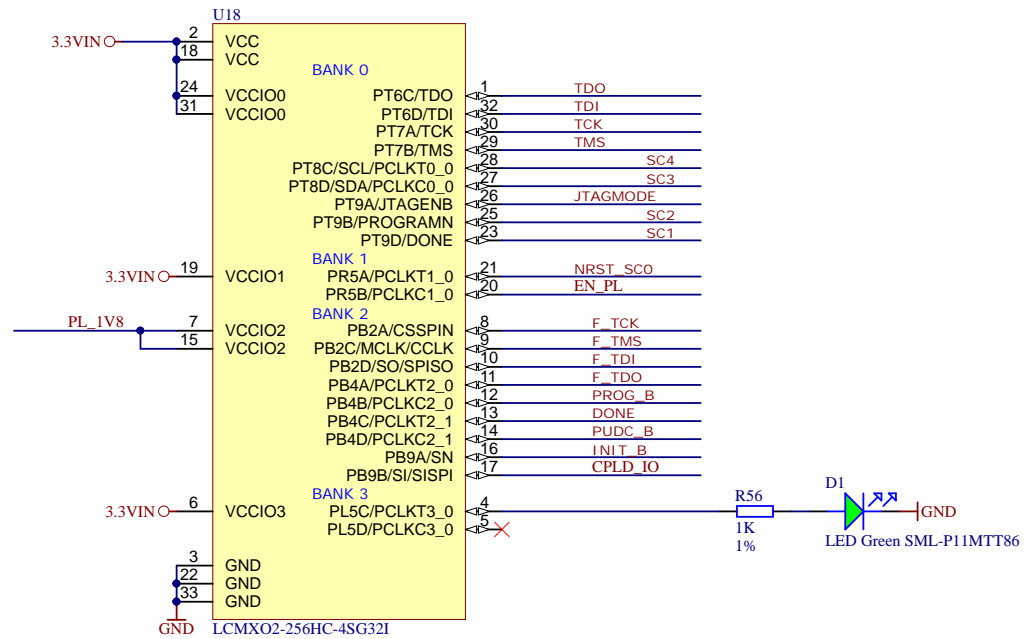


XCKU035-2SFVA784I

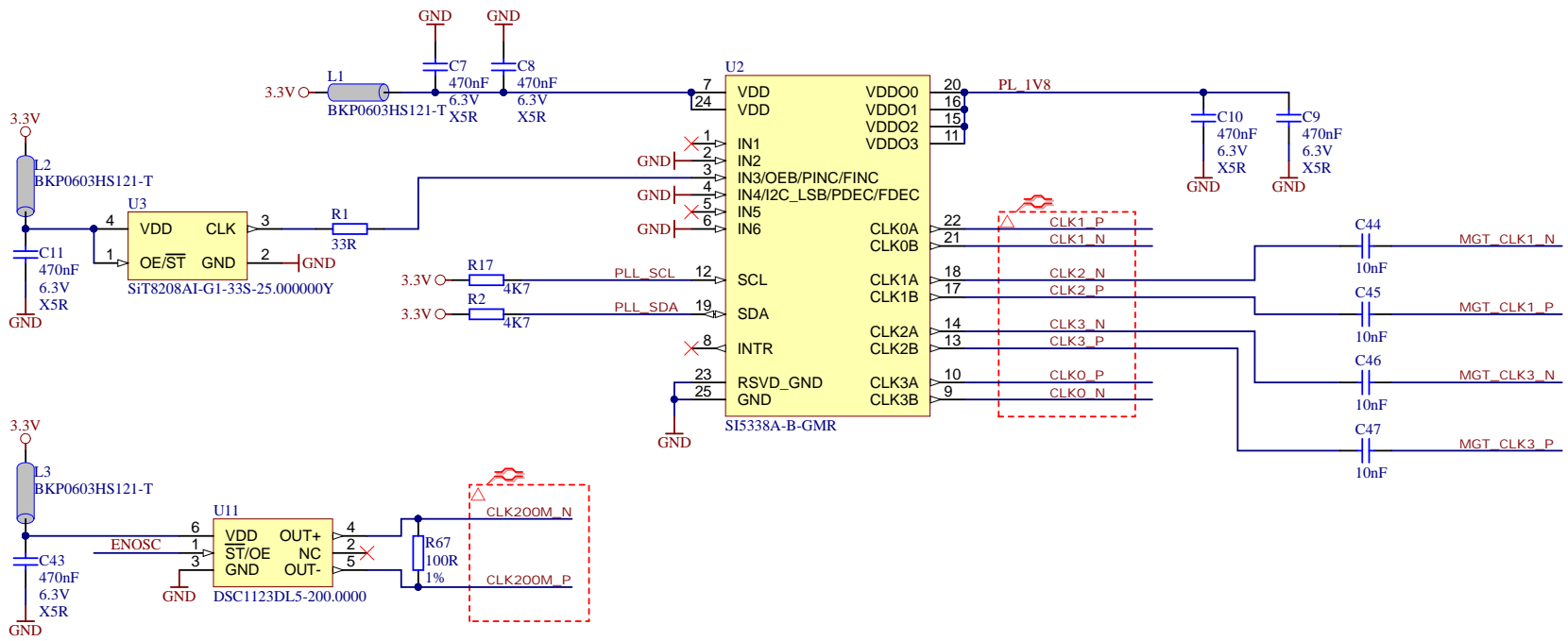
XCKU035-2SFVA784I




Title: TE0841		
A4	Number: TE0841 TE0841-01-035-2I	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 14 of 22
Filename: FPGA-PWR.SchDoc		



Title: TE0808		
A4	Number: TE0841 TE0841-01-035-2I	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 15 of 22
Filename: CPLD.SchDoc		



	Title: TE0841		
	A4	Number: TE0841 TE0841-01-035-21	Rev. 01
	Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 16 of 22
	Filename: Clock.SchDoc		

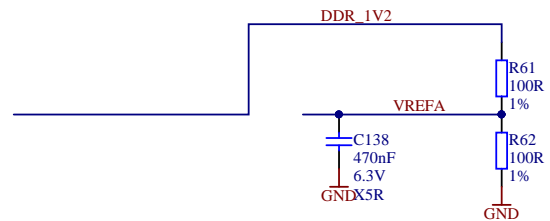
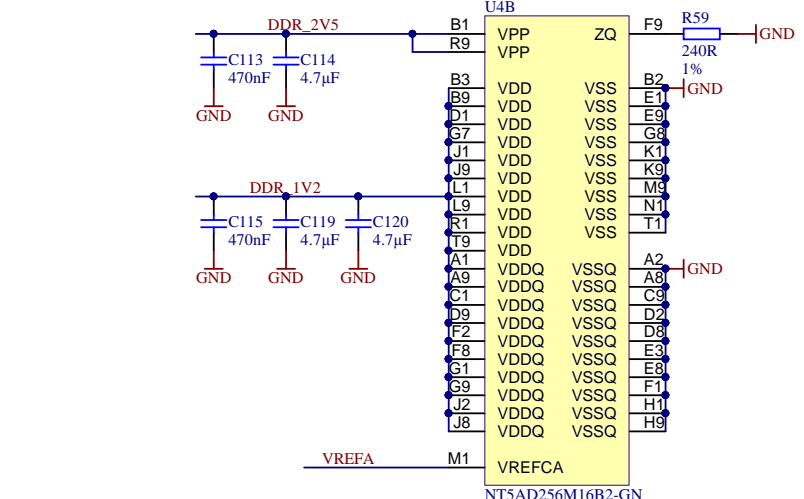
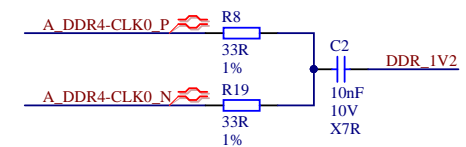
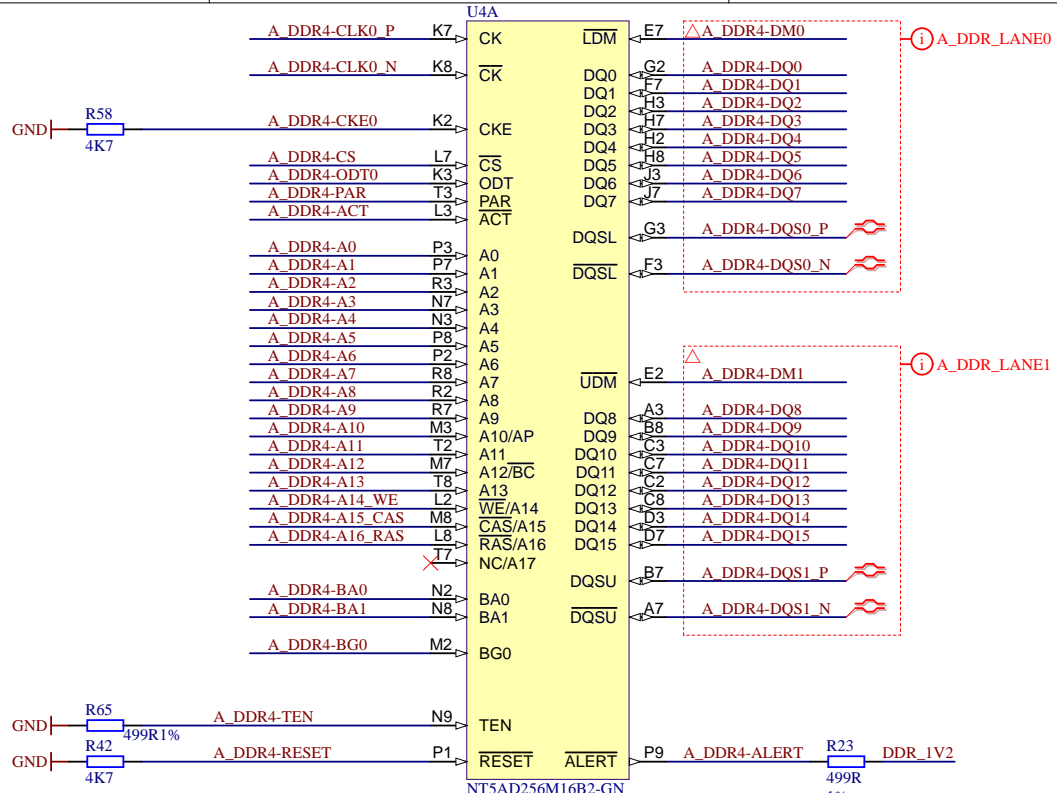


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Title: TE0808		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 17 of 22
Filename: DDR4-RAM.SchDoc		

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1

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4

A

A

B

B

C

C

D

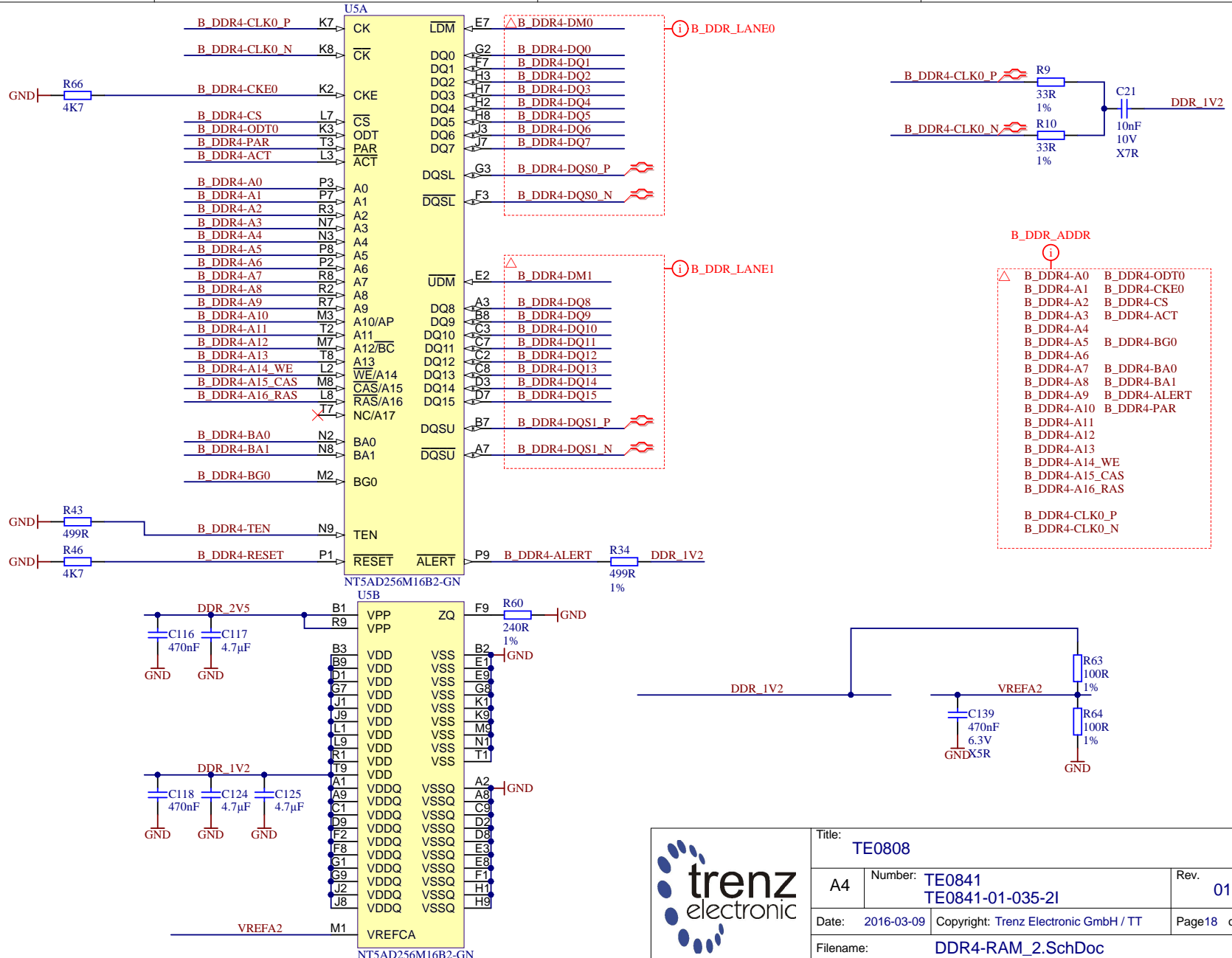
D

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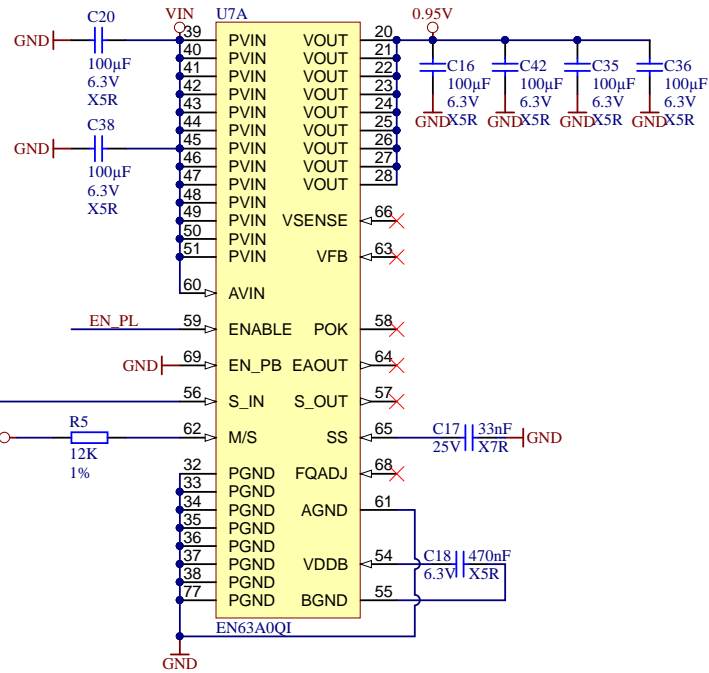
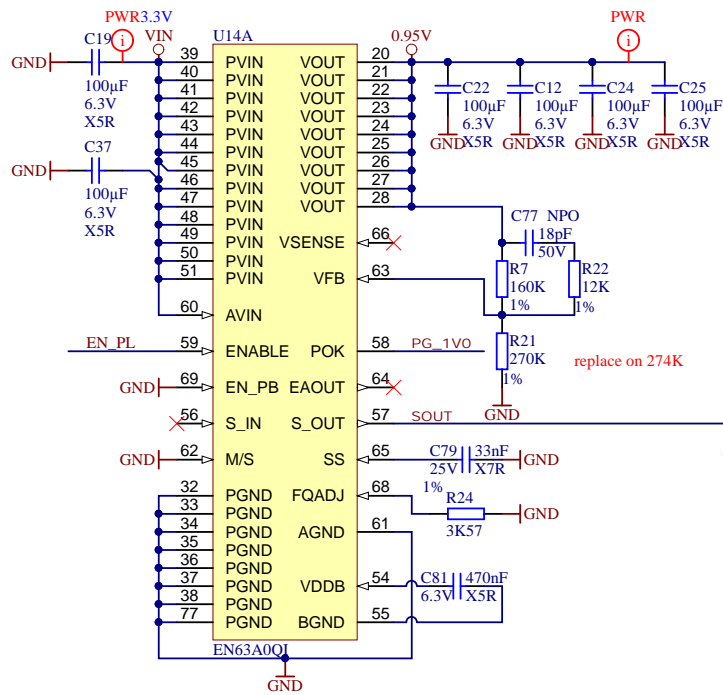
Title: TE0808		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page18 of 22
Filename: DDR4-RAM_2.SchDoc		

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**U14B EN63A0QI Pin Connections:**

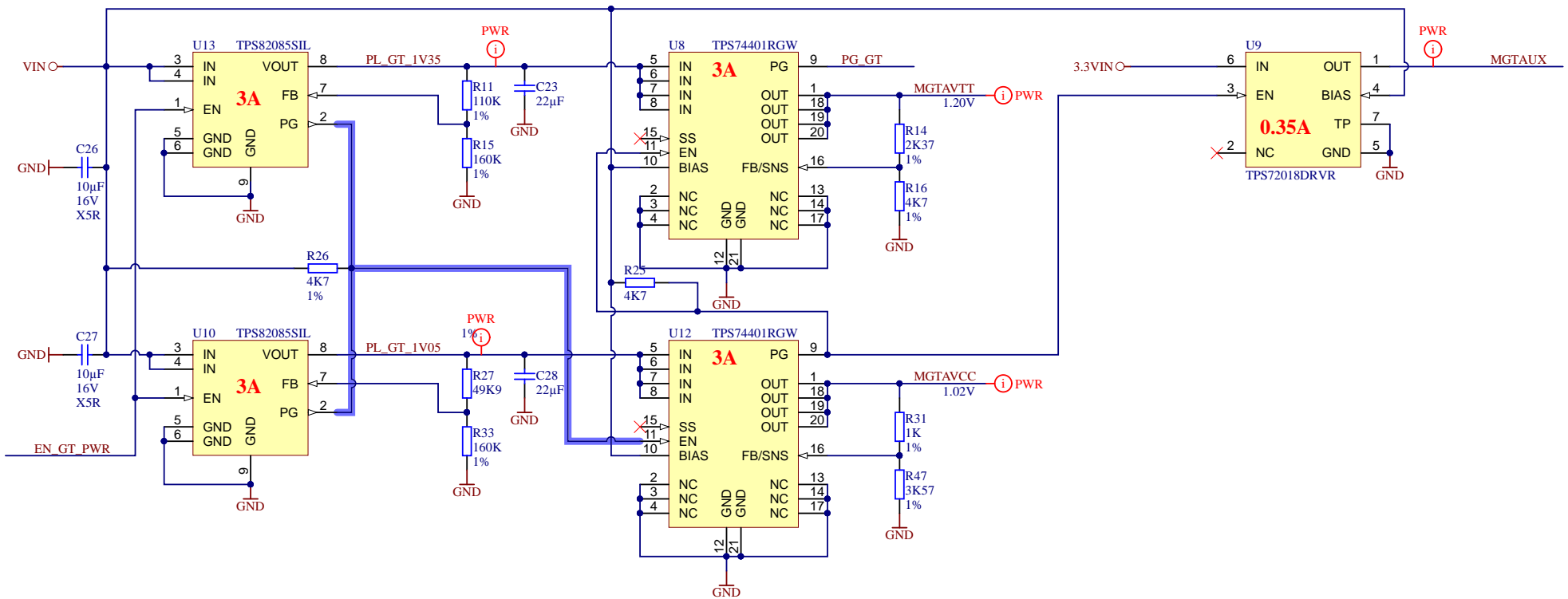
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76


**U7B EN63A0QI Pin Connections:**

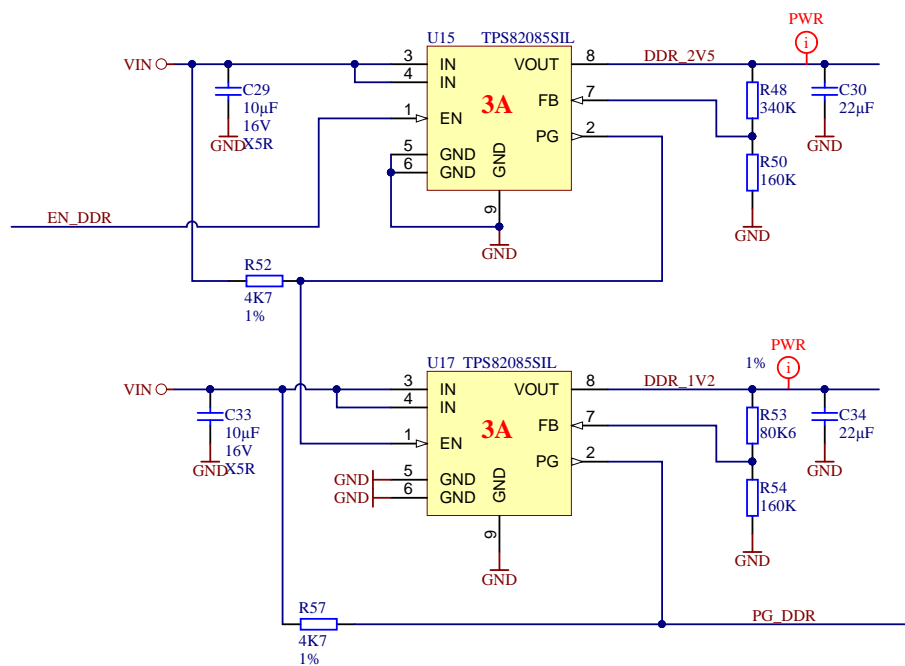
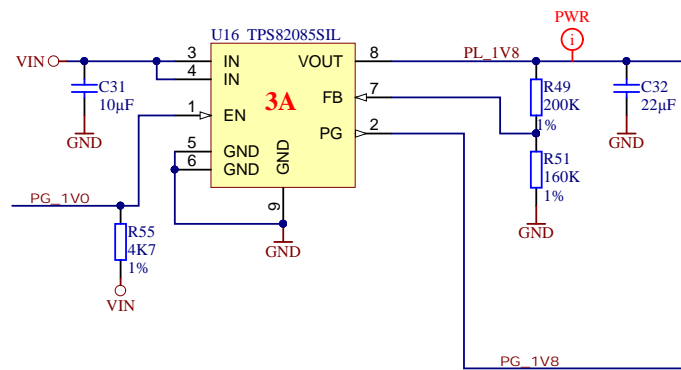
1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76



Title: TE0841		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page 19 of 22
Filename: PWR1.SchDoc		



			Title: TE0841	
			A4	Number: TE0841 TE0841-01-035-21
Date: 2016-03-09		Copyright: Trenz Electronic GmbH / TT		Page20 of 22
Filename: PWR2.SchDoc				



Title: TE0808		
A4	Number: TE0841 TE0841-01-035-21	Rev. 01
Date: 2016-03-09	Copyright: Trenz Electronic GmbH / TT	Page21 of 22
Filename: POWER_2.SchDoc		

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CHANGES REV01 TO REV01A (08.16.2017):

1) U1: changed schematic symbol. Next pins swapped to mach same polarity order:  
 -- AE13 (IO\_L6P\_T0U\_N10\_AD6P\_64)/AE12 (IO\_L6N\_T0U\_N11\_AD6N\_64)  
 -- J5 (IO\_L18P\_T2U\_N10\_AD2P\_66)/J4 (IO\_L18N\_T2U\_N11\_AD2N\_66)

2) Net names changed (no electrical changes):

JM1: swapped signals B64\_L6:  
 -- B64\_L6\_N - pin 40 (was pin 42)  
 -- B64\_L6\_P - pin 42 (was pin 40)  
 JM3: swapped signals B64\_L6:  
 -- B66\_L18\_N - pin 52 (was pin 54)  
 -- B66\_L18\_P - pin 54 (was pin 52)

A

A

B

B

C

C

D

D

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Title: <b>TE0808 - Changes list</b>		
A4	Number: <b>TE0841</b> <b>TE0841-01-035-2I</b>	Rev. <b>01</b>
Date: <b>2017-08-16</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>22</b> of <b>22</b>
Filename: <b>Revision_Changes.SchDoc</b>		