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SN74LVCH16540A
16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS
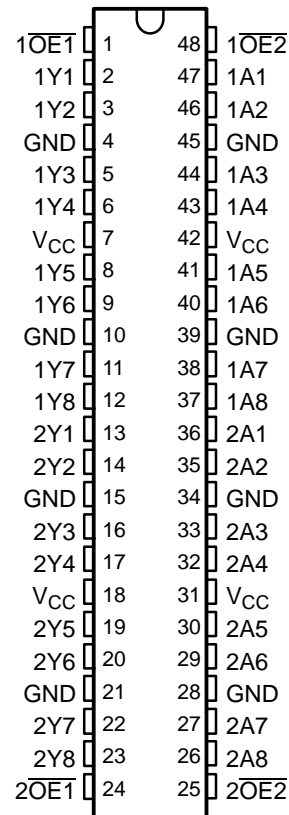SCAS569H−MARCH 1996−REVISED MARCH 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 3.7 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 1000-V Charged-Device Model (C101)**

DGG, DGV, OR DL PACKAGE
(TOP VIEW)

1$\overline{OE1}$	1	48	1$\overline{OE2}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
1Y5	8	41	1A5
1Y6	9	40	1A6
GND	10	39	GND
1Y7	11	38	1A7
1Y8	12	37	1A8
2Y1	13	36	2A1
2Y2	14	35	2A2
GND	15	34	GND
2Y3	16	33	2A3
2Y4	17	32	2A4
V_{CC}	18	31	V_{CC}
2Y5	19	30	2A5
2Y6	20	29	2A6
GND	21	28	GND
2Y7	22	27	2A7
2Y8	23	26	2A8
2$\overline{OE1}$	24	25	2$\overline{OE2}$

DESCRIPTION/ORDERING INFORMATION

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation and provides a high-performance bus interface for wide data paths.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube	SN74LVCH16540ADL	LVCH16540A
		Tape and reel	SN74LVCH16540ADLR	
	TSSOP – DGG	Tape and reel	SN74LVCH16540ADGGR	LVCH16540A
	TVSOP – DGV	Tape and reel	SN74LVCH16540ADGVR	LDH540A

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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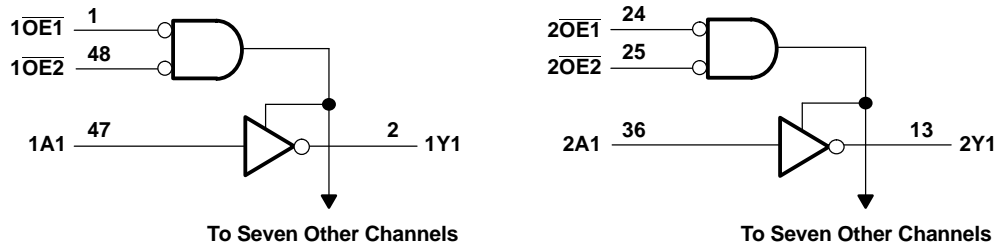**www.ti.com**

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE
(EACH 8-BIT SECTION)

INPUTS			OUTPUT
$\overline{\text{OE1}}$	$\overline{\text{OE2}}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)

To Seven Other Channels   To Seven Other Channels

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WITH 3-STATE OUTPUTS

SCAS569H – MARCH 1996 – REVISED MARCH 2005

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DGV package		58	
		DL package		63	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the recommended operating conditions table.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 2.7 V		−12	
		V_{CC} = 3 V		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}	$I_{OH} = -100$ μA		1.65 V to 3.6 V	$V_{CC} - 0.2$			V
	$I_{OH} = -4$ mA		1.65 V	1.2			
	$I_{OH} = -8$ mA		2.3 V	1.7			
	$I_{OH} = -12$ mA		2.7 V	2.2			
			3 V	2.4			
	$I_{OH} = -24$ mA		3 V	2.2			
V_{OL}	$I_{OL} = 100$ μA		1.65 V to 3.6 V			0.2	V
	$I_{OL} = 4$ mA		1.65 V			0.45	
	$I_{OL} = 8$ mA		2.3 V			0.7	
	$I_{OL} = 12$ mA		2.7 V			0.4	
	$I_{OL} = 24$ mA		3 V			0.55	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5	μA
$I_{I(hold)}$	$V_I = 0.58$ V		1.65 V		[2]		μA
	$V_I = 1.07$ V				[2]		
	$V_I = 0.7$ V		2.3 V		45		
	$V_I = 1.7$ V				−45		
	$V_I = 0.8$ V		3 V		75		
	$V_I = 2$ V				−75		
	$V_I = 0$ to 3.6 V[3]		3.6 V			±500	
I_{off}	V_I or $V_O = 5.5$ V		0			±10	μA
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			20	μA
	3.6 V ≤ V_I ≤ 5.5 V[4]					20	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		5		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		6.5		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.
(2) This information was not available at the time of publication.
(3) This is the bus-hold maximum dynamic current required to switch the input from one state to another.
(4) This applies in the disabled state only.

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	[1]	[1]	[1]	[1]		4.5	1	3.7	ns
t_{en}	$\overline{OE}$	Y	[1]	[1]	[1]	[1]		5.9	1.5	4.8	ns
t_{dis}	$\overline{OE}$	Y	[1]	[1]	[1]	[1]		6.3	1.6	5.9	ns

(1) This information was not available at the time of publication.

Operating Characteristics

$T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V TYP	V_{CC} = 2.5 V TYP	V_{CC} = 3.3 V TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	(1)	(1)	34	pF
	Outputs disabled		(1)	(1)	2	

(1) This information was not available at the time of publication.

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SCAS569H−MARCH 1996−REVISED MARCH 2005

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PARAMETER MEASUREMENT INFORMATION
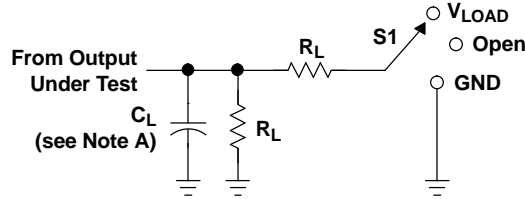
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

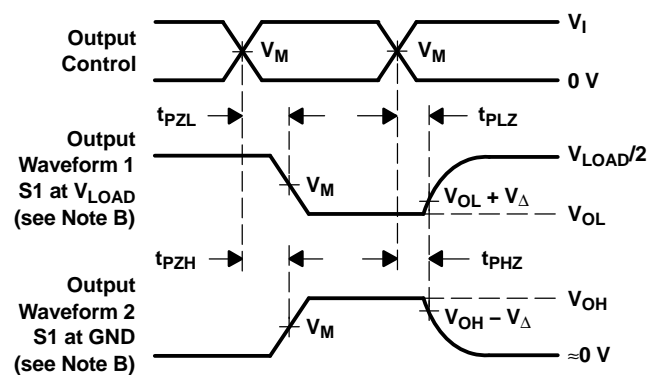| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
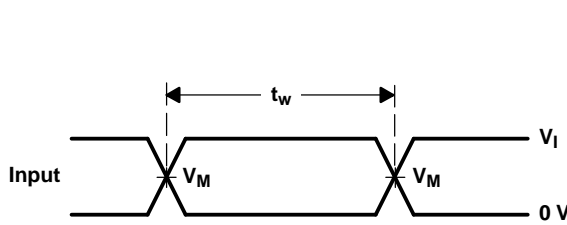
VOLTAGE WAVEFORMS
PULSE DURATION
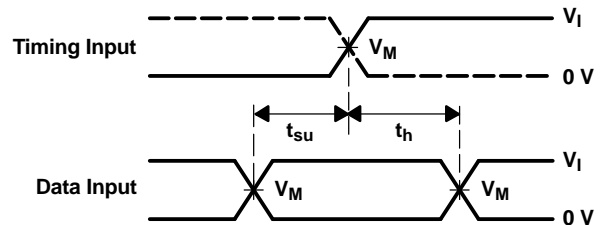
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
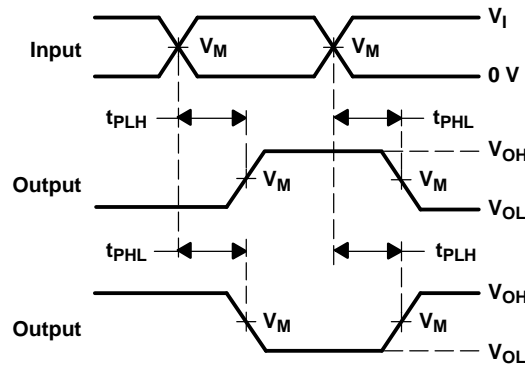
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCH16540ADGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH16540A	Samples
SN74LVCH16540ADL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH16540A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH16540ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH16540ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

$\dfrac{0.0135\ (0,343)}{0.008\ (0,203)}$ ⊕ | 0.005 (0,13) Ⓜ

48   25

$\dfrac{0.420\ (10,67)}{0.395\ (10,03)}$

$\dfrac{0.299\ (7,59)}{0.291\ (7,39)}$

$\dfrac{0.010\ (0,25)}{0.005\ (0,13)}$

Gage Plane

1   24

0°−8°

0.010 (0,25)

$\dfrac{0.630\ (16,00)}{0.620\ (15,75)}$

$\dfrac{0.040\ (1,02)}{0.020\ (0,51)}$

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ | 0.004 (0,10)

0.004 (0,10)

4040048−3/F   05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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8.3 / 7.9 TYP

A

PIN 1 ID AREA

46X 0.5

48

1

12.6 / 12.4 NOTE 3

2X 11.5

24

25

B

6.2 / 6.0

48X 0.27 / 0.17

⌖ | 0.08Ⓜ | C | A | B

C

SEATING PLANE

⌒ | 0.1 | C

1.2 / 1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75 / 0.50

0.15 / 0.05

DETAIL A
TYPICAL
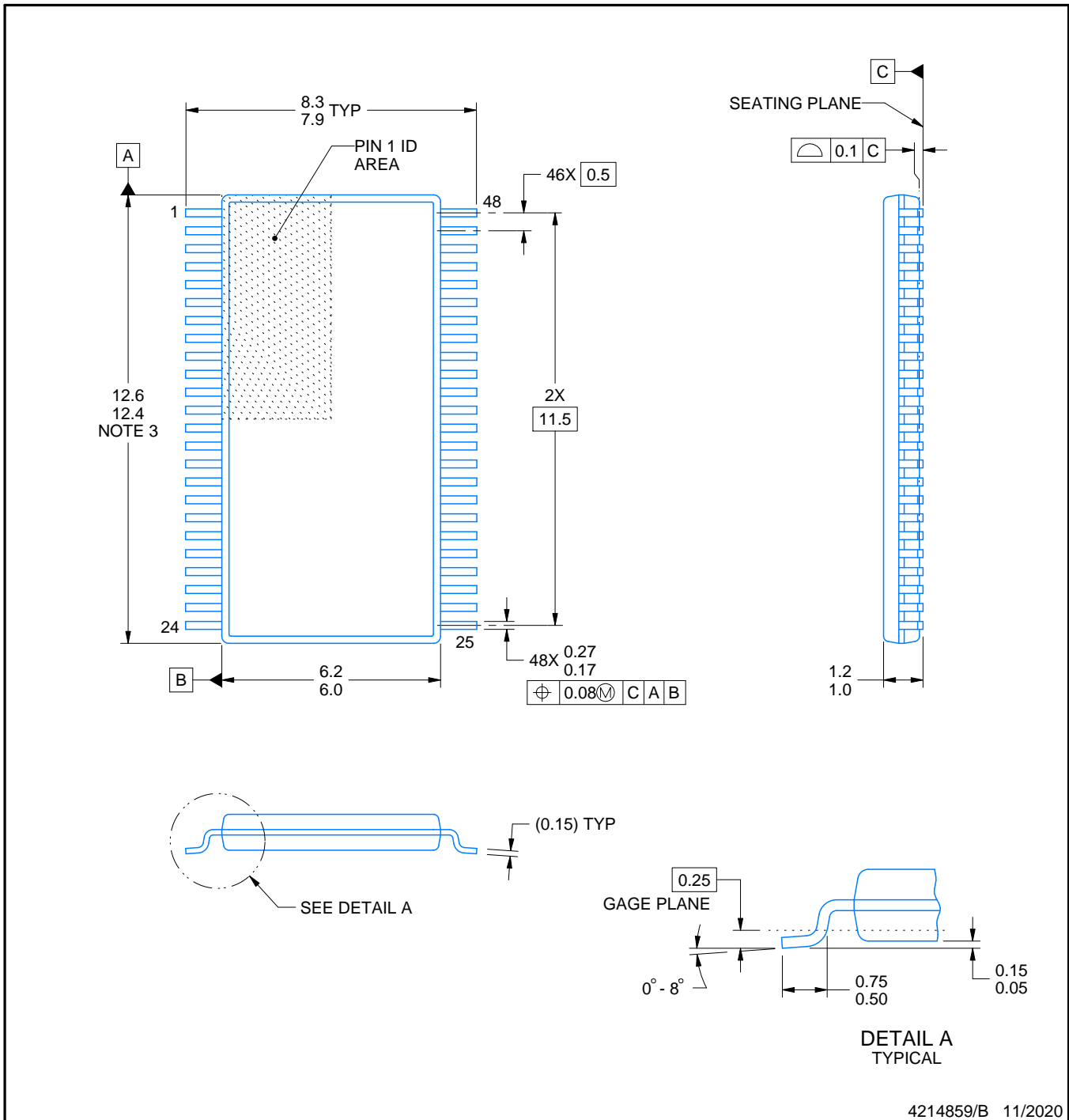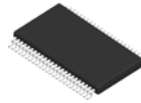
4214859/B 11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

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48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM

48

SYMM

24

25

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214859/B   11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DGG0048A

48X (1.5)

SYMM

1

48

48X (0.3)

46X (0.5)

(R0.05) TYP

SYMM

24

25

(7.5)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
    B. This drawing is subject to change without notice.
    C. Body dimensions do not include mold protrusion not to exceed 0,15.
    D. Falls within JEDEC MO-153

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