PCN Number:	20171128000	**PCN Date:**	Dec 5, 2017
Title:	AFE5816ZAV/AFE58JD16ZAV Design Change and Datasheet Updates		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	Mar 5, 2018	**Estimated Sample Availability:**	Date provided at sample request.

Change Type:					
☐	Assembly Site	☐	Assembly Process	☐	Assembly Materials
☒	Design	☒	Electrical Specification	☐	Mechanical Specification
☐	Test Site	☐	Packing/Shipping/Labeling	☐	Test Process
☐	Wafer Bump Site	☐	Wafer Bump Material	☐	Wafer Bump Process
☐	Wafer Fab Site	☐	Wafer Fab Materials	☐	Wafer Fab Process
		☐	Part number change		

PCN Details

Description of Change:

This notification is to inform of a design change to the AFE5816ZAV and AFE58JD16ZAV devices. Affected devices are listed in the Product Affected section of this document.

The design change is to suppress VCA and memory write glitches for improving overall performance.

The datasheet numbers will be changing:

	Current	New
Device	**Datasheet Number**	**Datasheet Number**
AFE5816ZAV	SBAS688D	SBAS688E
AFE58JD16ZAV	SBAS719	SBAS719A

The product datasheet(s) is also updated as seen in the change revision history below:

AFE5816 16-Channel Ultrasound AFE With 90-mW/Channel Power, 1-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC and Passive CW Mixer

Changes from Revision D (November 2015) to Revision E — **Page**

- Deleted *Output and Gain Code Step Response vs Time* figure ... 24
- Deleted condition statement from *Output and Gain Code Step Response vs Time* figure ... 24
- Changed *Device Power vs Gain Code* figure ... 25
- Deleted *Device Power vs Gain Code (TGC_CONS register bit = 1)* figure ... 25
- Changed *VCA Power vs Gain Code* figure ... 25
- Changed *AVDD_1P9 Supply Current vs Gain Code* figure ... 26
- Deleted contour curves from *Typical Characteristics: TGC Mode* section ... 26
- Changed *Input Signal Support in TGC Mode* section ... 32
- Added footnote 2 to *Profile Description for Up, Down Ramp Mode* table ... 39
- Changed TGC_SLOPE and TGC_UP_DN clock traces in *External Non-Uniform Mode* figure ... 40
- Added footnote 2 to *Profile Description for External Non-Uniform Mode* table ... 41
- Changed Figure 72 ... 45
- Added footnote 2 to *Internal Non-Uniform Mode Profile Definition* table ... 47
- Added *Latency Between a Transition in TGC_SLOPE and the Resulting Change in Gain* table and associated paragraph to *Timing Specifications* section ... 47
- Changed second sentence in sixth paragraph of *Continuous-Wave (CW) Beamformer* section ... 51
- Changed Figure 77 ... 52
- Changed last paragraph of *16 × f_{cw} Mode* section ... 53
- Changed *Clock Configurations* figure ... 56
- Changed Number of samples from "2045" to "2047" in Table 15 ... 67
- Changed *HPF_ROUND_ENABLE register bit (register 21, bit 5)* to *HPF_ROUND_EN_CH1-8 and HPF_ROUND_EN_CH9-16 bits* in last paragraph of *Digital HPF* section ... 69
- Added last paragraph to *Partial Power-Up and Power-Down Mode* section ... 76
- Added PLL initialization method (step 4) to *Initialization Set Up* section ... 84
- Added *PLL Initialization* section ... 86
- Changed *PIN_PAT_LVDS* to *PAT_LVDS15[2:0]* in register 59 of *ADC Register Map* table ... 97
- Added registers 65 and 66 to *ADC Register Map* table ... 97
- Changed 001 row description from *half frame 0, half frame 1* to *half frame 1, half frame 0* in *Pattern Mode Bit Description* table ... 99
- Changed *HPF_ROUND_EN* to *HPF_ROUND_EN_CH1-8* in register 21 ... 108
- Changed bit 5 from 0 to *HPF_ROUND_EN_CH9-16* in register 45 ... 122
- Changed bits 7-5 from *PIN_PAT_LVDS* to *PAT_LVDS15[2:0]* in register 59 ... 130
- Added register descriptions for registers 65 and 66 ... 132
- Deleted register 202 from *VCA Register Map* table ... 134
- Deleted WEBENCH from *Related Documentation* section ... 158

Revision History (continued)

AFE58JD16 16-Channel Ultrasound AFE with 90-mW/Channel Power, 1-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC and Passive CW Mixer

Changes from Original (August 2015) to Revision A **Page**

- Deleted *Output and Gain Code Step Response vs Time* figure 26
- Deleted condition from *Output and Gain Code Step Response vs Time* figure 26
- Changed *Device Power vs Gain Code* figure 27
- Deleted *Device Power vs Gain Code (TGC_CONS Register Bit = 1)* figure 27
- Changed *VCA Power vs Gain Code* figure 27
- Changed *AVDD_1P9 Supply Current vs Gain Code* figure 28
- Changed *Total Power Dissipation vs ADC Sample Rate* figure 28
- Deleted contour figures from *Typical Characteristics: TGC Mode* section 28
- Changed *Input to the device* conditions of *Typical Characteristics: Demodulator* section 30
- Changed *Input Signal Support in TGC Mode* section 37
- Added note 2 to *Profile Description for Up, Down Ramp Mode* table 44
- Changed TGC_SLOPE and TGC_UP_DN clock traces in *External Non-Uniform Mode* figure 45
- Added note 2 to *Profile Description for External Non-Uniform Mode* table 46
- Changed *Internal Non-Uniform Mode Operation* figure 50
- Added note 2 to *Internal Non-Uniform Mode Profile Definition* table 52
- Added *Latency Between a Transition in TGC_SLOPE and the Resulting Change in Gain* table and associated paragraph to *Timing Specifications* section 52
- Changed *However* to *Though not shown in Equation 5,* in *Continuous-Wave (CW) Beamformer* section 56
- Changed Figure 87 57
- Changed last paragraph of *16 × f_{cw} Mode* section 58
- Changed *Clock Configurations* figure 61

Revision History (continued)

- Changed number of samples from *2045* to *2047* in *Auto Offset Removal Accumulator Cycles* table 67
- Changed *HPF_ROUND_ENABLE register bit (register 21, bit 5)* to *HPF_ROUND_EN_CH1-8 and HPF_ROUND_EN_CH9-16 bits* in *Digital HPF* section 69
- Changed *Demodulator* section 69
- Changed *Masking of the Various Reset Operations Resulting from SYNC~ or SYSREF* table 97
- Added *Interfacing SYNC~ and SYSREF Between the FPGA and AFEs* section 103
- Changed *Circuit to Level-Shift the Common-Mode Voltage From 1.2 V at the Driver Output to 0.7 V at the AFE Input* figure 103
- Changed *AC-Coupling Scheme for SYSREF* figure 104
- Added *AFE58JD16 Family Comparison* section, moved location of table to *Feature Description* section 110
- Added last paragraph to *Partial Power-Up and Power-Down Mode* section 113
- Changed last paragraph of *Register Readout* section 116
- Added PLL initialization method to *Initialization Set Up* section 121
- Added *PLL Initialization* section 123
- Changed bits 6 and 7 from 0 to COMPR_FACTOR_JESD in register 3 of *ADC Register Map* table 135
- Added *_CH1-8* to bit 5 in register 21 of *ADC Register Map* table 135
- Changed bit 5 from 0 to HPF_ROUND_EN_CH9-16 in register 45 of *ADC Register Map* table 136
- Changed PIN_PAT_LVDS15[2:0] to PAT_LVDS in register 59 in *ADC Register Map* table 136
- Added register 65 and register 66 to *ADC Register Map* table 136

Reason for Change:

Suppress VCA and memory write glitches

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

Die Rev designator will change as shown in the table and sample label below:

Current	**New**
Die Rev [2P]	**Die Rev [2P]**
A	**B**

Sample product shipping label (not actual product label)

Product Affected: Design Change and datasheet updates

AFE5816ZAV	AFE58JD16ZAV

Qualification Report

Die-Rev for VCA glitch enhancement - MCM, AFE5816ZAV (RFAB+DMOS6+TITL)

Approve Date 16-Nov-2017

Product Attributes

Attributes	Qual Device: AFE5816ZAV	QBS Product Reference: AFE5816ZAV (PG1.1)	QBS Product Reference: AFE5818ZBV (PG1.0)	QBS Process Reference: SN75DP130DSRGZR	QBS Process Reference: VSP6825BZRC	QBS Package Reference: AFE5808ZCF	QBS Package Reference: HPAWAVE3ZCF	QBS Package Reference: SN0711033ZCL
Assembly Site	AP3	AP3	AMK-K4	CLARK	PHI	AP3	AP3	AP3
Package Family	NFBGA	NFBGA	NFBGA	QFN	JRBGA	NFBGA	NFBGA	NFBGA
Flammability Rating	UL 94 V-0	UL 94 V-0	UL 94 V-0	UL 94 V-0	UL 94 V-0	UL 94 V-0	UL 94 V-0	UL 94 V-0
Wafer Fab Supplier	DMOS6, RFAB	DMOS6, RFAB	DMOS6, FFAB	DMOS6	HIJI, RFAB	DMOS5, FFAB	DM6	DM5
Wafer Process	C05.2, C027.A	C027.A, C05.2	C027.A, BICOM3X	C027.A	C05, LBC4	C05, BICOM3X	C027.0	A035.1

- QBS: Qual By Similarity
- Qual Device AFE5816ZAV is qualified at LEVEL3-260C
- Device AFE5816ZAV contains multiple dies.

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: AFE5816ZAV	QBS Product Reference: AFE5816ZAV (PG1.1)	QBS Product Reference: AFE5818ZBV (PG1.0)	QBS Process Reference: SN75DP130DSRGZR	QBS Process Reference: VSP6825BZRC	QBS Package Reference: AFE5808ZCF	QBS Package Reference: HPAWAVE3ZCF	QBS Package Reference: SN0711033ZCL
AC	Autoclave 121C	96 Hours	-	-	-	3/231/0	-	-	1/77/0	-
ED	Electrical Characterization	Per Datasheet Parameters	Pass	-	-	Pass	-	Pass	Pass	Pass
ELFR	Early Life Failure Rate, 125C	48 Hours	-	-	3/3000/0	3/1852/0	-	-	-	-
HAST	Biased HAST, 130C/85%RH	96 Hours	-	-	3/162/0	3/225/0	3/230/0	-	-	3/231/0
HBM	ESD - HBM	4000 V	1/3/0	-	2/6/0	-	-	-	-	-
CDM	ESD - CDM	1500 V	1/3/0	-	-	-	-	1/3/0	1/3/0	-
HTOL	Life Test, 125C	1000 Hours	-	-	3/231/0	3/231/0	-	-	1/77/0	3/231/0
HTOL	Life Test, 140C	480 Hours	-	-	-	-	3/231/0	-	-	-
HTSL	High Temp. Storage Bake, 150C	1000 Hours	-	-	-	-	-	-	-	3/231/0
HTSL	High Temp. Storage Bake, 170C	420 Hours	-	-	3/231/0	3/231/0	3/231/0	-	1/77/0	-
LU	Latch-up	(per JESD78)	-	1/6/0	2/12/0	3/18/0	2/12/0	1/6/0	1/6/0	3/18/0
PD	Physical Dimensions	--	-	-	-	-	-	-	-	3/15/0
SBS	Solder Ball Shear	--	-	1/77/0	3/231/0	-	-	-	-	2/154/0
TC	Temperature Cycle, -55/125C	700 Cycles	-	1/77/0	3/231/0	-	-	1/77/0	-	3/231/0

TC	Temperature Cycle, -65/150C	500 Cycles	-	-	-	3/231/0	3/231/0	-	1/77/0	-
UHAST	Unbiased HAST 110C/85%RH	264 Hours	-	1/77/0	3/231/0	-	-	-	-	-
UHAST	Unbiased HAST 130C/85%RH	96 Hours	-	-	-	3/231/0	-	-	-	3/231/0

- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

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