Product Change Notification

(Notification - P1703015-DIGI)

(CST-R2-AD121)

February 13, 2017

To: *Our Valued Digi-Key, Inc. Customer*

Overview: The purpose of this notification is to communicate a product change of select Renesas Electronics America, Inc. (REA) devices. These devices have suggested replacements.

Select SRAM products in TSOP packages are undergoing the following changes (see the Appendix for specific details)...

1. Unification of Speed and Temperature Grades. Grades "-5SR", "-7SI", & "-7SR" are being unified to single grade, "-5SI".
2. Assembly and Final Test Site change from Renesas Semiconductor Beijing to Amkor Technology Malaysia (Assembly) & Powertech Technology Inc. (Final Test).
3. Lead Frame Material change from 42-Alloy to Cu.
4. Moisture Sensitivity Level change from MSL2 to MSL3.
5. Lead Plating Material change from Sn-Cu to Sn.
6. Standardization of JEDEC trays and Tape & Reel specifications.

There are no changes to reliability and quality levels. The replacement device has superior electrical specifications.

Affected Products: A review of our records indicate the attached list of products may affected your company.

Booking Part Number	Suggested Replacement Part Number
R1LV3216RSA-7SI#B0	R1LV3216RSA-5SI#B1

Part numbers given in this list are for active part numbers in REA database at the time of this notification.

Key Dates:

Final last time buy **(LTB)** orders of original part number placed to REA or to a franchised REA distributor.	**Dec. 15th, 2017**
Planned date for last time shipment **(LTS)** of original part number from REA.	**Dec. 15th, 2018**

Response: Please place last time buy (LTB) orders in a timely manner prior to the key dates listed to avoid product availability issues. If you anticipate volumes beyond your regular rate, please contact your REA sales representative with a forecast of your requirements. Shipments between the LTB and LTS dates are Non-Cancelable and Non-Returnable (NCNR).

Please contact your REA sales representative for any questions or comments.

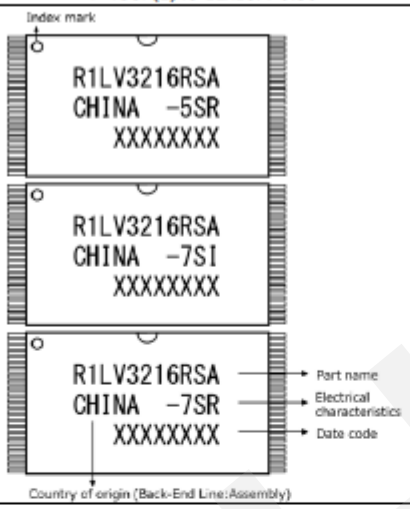
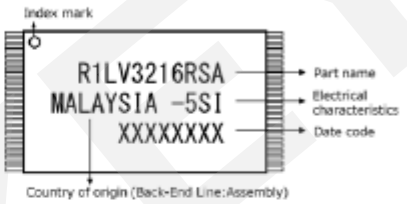
Thank you for your attention.

Sincerely,

Renesas Electronics America, Inc.

Appendix A: Comparison Table

48pin-TSOP(I) 32Mb(3V) Part name : R1LV3216RSA

Item		Pre Change	Post Change
Orderable part name		R1LV3216RSA-5SR/-7SI/-7SR#B0 (Tray packing)	R1LV3216RSA-5SI#B1 (Tray packing)
		R1LV3216RSA-5SR/-7SI/-7SR#S0 (Tape & Reel packing)	R1LV3216RSA-5SI#S1 (Tape & Reel packing)
Assembly line		Renesas Semiconductor Beijing (China)	Amkor Technology Malaysia (Malaysia)
Country of origin display		CHINA	MALAYSIA
JEITA Package Code		P-TSOP(1)48-12x18.4-0.50	P-TSOP(1)48-12x18.4-0.50
Package marking specification			
Assembly Material	Lead frame material	42Alloy	Cu
	Lead plating	Sn-Cu	Sn (pure tin)
	Die bonding	Epoxy film	Epoxy paste
	Wire bonding	Au	Au
	Mold	Epoxy resin (Halogen-included)	Epoxy resin (Halogen-free)
Final test line		Renesas Semiconductor Beijing (China)	Powertech Technology Inc. (Taiwan)
Tray packing	Packing specification	Current specification	New specification
	Tray	JEDEC Tray with Renesas Logo (TSOP I package size: 12mm x 18.4mm)	JEDEC Tray without Renesas Logo (TSOP I package size: 12mm x 18.4mm)
	Storage number	96pcs/tray	96pcs/tray
	Laying direction of ICs on a tray	Direction from the top left position to the down side (when the position of chamfer in tray's corner is bottom left.)	No change
	Number of trays (Max.)	8 trays + 1 tray (cover)	10 trays + 1 tray (cover)
	Inner box size (LxWxH)	330mm x 152mm x 75mm	351mm x 175mm x 104mm
Tape & Reel packing	Packing specification	Current specification	New specification
	Embossed tape	Current specification (type name : TE3216-16P)	New specification (type name : TSOP48-3)
	Storage number	1,000pcs/reel	1,000pcs/reel
	Inner box size (LxWxH)	347mm x 368mm x 54mm	362mm x 340mm x 60mm
Moisture-proof performance		MSL 2	MSL 3
Shipping label		Current specification	No change in format (Changes in orderable part name, country of origin and MSL display)

- Note: Accompanied with a change of JEDEC tray, the package seat position in tray pocket is to be changed.
- Note: Accompanied with a change of embossed tape, the package seat position in taping pocket is not to be changed. No change in width and pitch of embossed tape. No change in reel diameter.

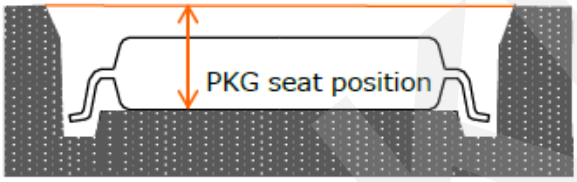
Appendix B: Packaging Specification (Tray Shipping)

Change the specification of the JEDEC tray (48pin-TSOP(I) products only)

- Regarding 48pin-TSOP(I) products (R1LV3216RSA), the package seat position in tray pocket is to be changed (see below).

  No change in outline dimensions and pocket pitch for JEDEC tray.

Package type	Pre Change		Post Change	
	Tray type name	PKG seat position (mm)	Tray type name	PKG seat position (mm)
48pin-TSOP(I)	L196-126	2.0	EA51220	1.5



Cross section of tray pocket

Appendix C: Product Integration

Regarding the EOL of "-5SR, -7SI, -7SR" products, these "Access and Temperature grades" are unified to "-5SI" (see below).

Package Type	Memory Cap., Supply Voltage	bit	Pre Change			Post Change		
			Orderable Part Name	Access time	Operation Temp.	Orderable Part Name	Access time	Operation Temp.
48pin-TSOP(I)	32Mb 3V	x16	R1LV3216RSA-5SR#B0 R1LV3216RSA-5SR#S0	55ns	0℃ ~70℃	R1LV3216RSA-5SI#B1 R1LV3216RSA-5SI#S1	55ns	-40℃ ~85℃
			R1LV3216RSA-7SI#B0 R1LV3216RSA-7SI#S0	70ns	-40℃ ~85℃			
			R1LV3216RSA-7SR#B0 R1LV3216RSA-7SR#S0		0℃ ~70℃			

Appendix D: Electrical Characteristics (DC/AC)

Regarding the EOL of "-5SR, -7SI, -7SR" products, electrical characteristics (DC/AC) of unified "-5SI" product is completely upper-compatible with "- "-5SR, -7SI, -7SR" products (see below).

Electrical characteristics (DC) : 32Mb(3V) R1LV3216RSA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV3216RSA-5SR, -7SI, -7SR#B0	R1LV3216RSA-5SI#B1
	R1LV3216RSA-5SR, -7SI, -7SR#S0	R1LV3216RSA-5SI#S1

DC conditions

Item	Symbol	Pre Change		Symbol	Post Change
Supply voltage	Vcc	2.7V~3.6V		Vcc	←
Operating temperature range	Ta	5SR, 7SR	0℃~70℃	Ta	-40℃~85℃
		7SI	-40℃~85℃		
Input high voltage	VIH	2.4V(min.) / Vcc+0.2V(max.)		VIH	←
Input low voltage	VIL	-0.2V(min.) / 0.4V(max.)		VIL	←

DC characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Operating Current	Icc1(TTL, Min.Cycle)	55mA(max.) / 40mA(typ.)		Icc1(TTL, Min.Cycle)	←	
	Icc2(MOS, Cycle=1us)	8mA(max.) / 3mA(typ.)		Icc2(MOS, Cycle=1us)	←	
Standby current	ISB(TTL)	0.3mA(max.) / 0.1mA(typ.)		ISB(TTL)	←	
	ISB1(MOS)	~25℃	12uA(max.) / 4uA(typ.)	ISB1(MOS)	~25℃	←
		~40℃	24uA(max.) / 7uA(typ.)		~40℃	←
		~70℃	50uA(max.)		~70℃	←
		~85℃ (for 7SI)	80uA(max.)		~85℃	←
Output high voltage	VOH	IOH=-0.5mA	2.4V(min.)	VOH	IOH=-0.5mA	←
Output low voltage	VOL	IOL=2mA	0.4V(max.)	VOL	IOL=2mA	←

Capacitance

Item	Symbol	Pre Change	Symbol	Post Change
Input capacitance	C in	10pF(max.)	C in	←
Input/Output capacitance	C I/O	10pF(max.)	C I/O	←

Data retention characteristics

Item	Symbol	Pre Change		Symbol	Post Change	
Vcc for data retention	VDR	2.0V(min.)		VDR	←	
Data retention current	IccDR	~25℃	12uA(max.) / 4uA(typ.)	IccDR	~25℃	←
		~40℃	24uA(max.) / 7uA(typ.)		~40℃	←
		~70℃	50uA(max.)		~70℃	←
		~85℃ (for 7SI)	80uA(max.)		~85℃	←
Chip deselect time to data retention	tCDR	0ns(min.)		tCDR	←	
Operation recovery time	tR	5ms(min.)		tR	←	

Appendix D (cont.): Electrical characteristics (DC/AC)

Electrical characteristics (AC) : 32Mb(3V) R1LV3216RSA

Products

Item	Pre Change	Post Change
Orderable part name	R1LV3216RSA-5SR, -7SI, -7SR#B0	R1LV3216RSA-5SI#B1
	R1LV3216RSA-5SR, -7SI, -7SR#S0	R1LV3216RSA-5SI#S1

AC characteristics
Read Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Read cycle time	tRC	5SR	55ns(min.)	tRC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address access time	tAA	5SR	55ns(max.)	tAA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select access time	tACS1 / tACS2	5SR	55ns(max.)	tACS1 / tACS2	55ns(max.)
		7SI, 7SR	70ns(max.)		
Output enable to output valid	tOE	5SR	25ns(max.)	tOE	25ns(max.)
		7SI, 7SR	35ns(max.)		
Output hold from address change	tOH	5SR	10ns(min.)	tOH	←
		7SI, 7SR	10ns(min.)		
LB#,UB# access time	tBA	5SR	55ns(max.)	tBA	55ns(max.)
		7SI, 7SR	70ns(max.)		
Chip select to output in low-Z	tCLZ1 / tCLZ2	5SR	10ns(min.)	tCLZ1 / tCLZ2	←
		7SI, 7SR	10ns(min.)		
LB#,UB# enable to low-Z	tBLZ	5SR	5ns(min.)	tBLZ	←
		7SI, 7SR	5ns(min.)		
Output enable to output in low-Z	tOLZ	5SR	5ns(min.)	tOLZ	←
		7SI, 7SR	5ns(min.)		
Chip deselect to output in high-Z	tCHZ1 / tCHZ2	5SR	0ns(min.) / 20ns(max.)	tCHZ1 / tCHZ2	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
LB#,UB# disable to high-Z	tBHZ	5SR	0ns(min.) / 20ns(max.)	tBHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Output disable to output in high-Z	tOHZ	5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		

Write Cycle

Item	Symbol	Pre Change		Symbol	Post Change
Write cycle time	tWC	5SR	55ns(min.)	tWC	55ns(min.)
		7SI, 7SR	70ns(min.)		
Address valid to end of write	tAW	5SR	50ns(min.)	tAW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Chip select to end of write	tCW	5SR	50ns(min.)	tCW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Write pulse width	tWP	5SR	40ns(min.)	tWP	40ns(min.)
		7SI, 7SR	55ns(min.)		
LB#,UB# valid to end of write	tBW	5SR	50ns(min.)	tBW	50ns(min.)
		7SI, 7SR	65ns(min.)		
Address setup time	tAS	5SR	0ns(min.)	tAS	←
		7SI, 7SR	0ns(min.)		
Write recovery time	tWR	5SR	0ns(min.)	tWR	←
		7SI, 7SR	0ns(min.)		
Data to write time overlap	tDW	5SR	25ns(min.)	tDW	25ns(min.)
		7SI, 7SR	35ns(min.)		
Data hold from write time	tDH	5SR	0ns(min.)	tDH	←
		7SI, 7SR	0ns(min.)		
Output enable from end of write	tOW	5SR	5ns(min.)	tOW	←
		7SI, 7SR	5ns(min.)		
Output disable to output in high-Z	tOHZ	5SR	0ns(min.) / 20ns(max.)	tOHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		
Write to output in high-Z	tWHZ	5SR	0ns(min.) / 20ns(max.)	tWHZ	0ns(min.) / 20ns(max.)
		7SI, 7SR	0ns(min.) / 25ns(max.)		