UM2076
User manual

Getting started with the STEVAL-ISF003V1

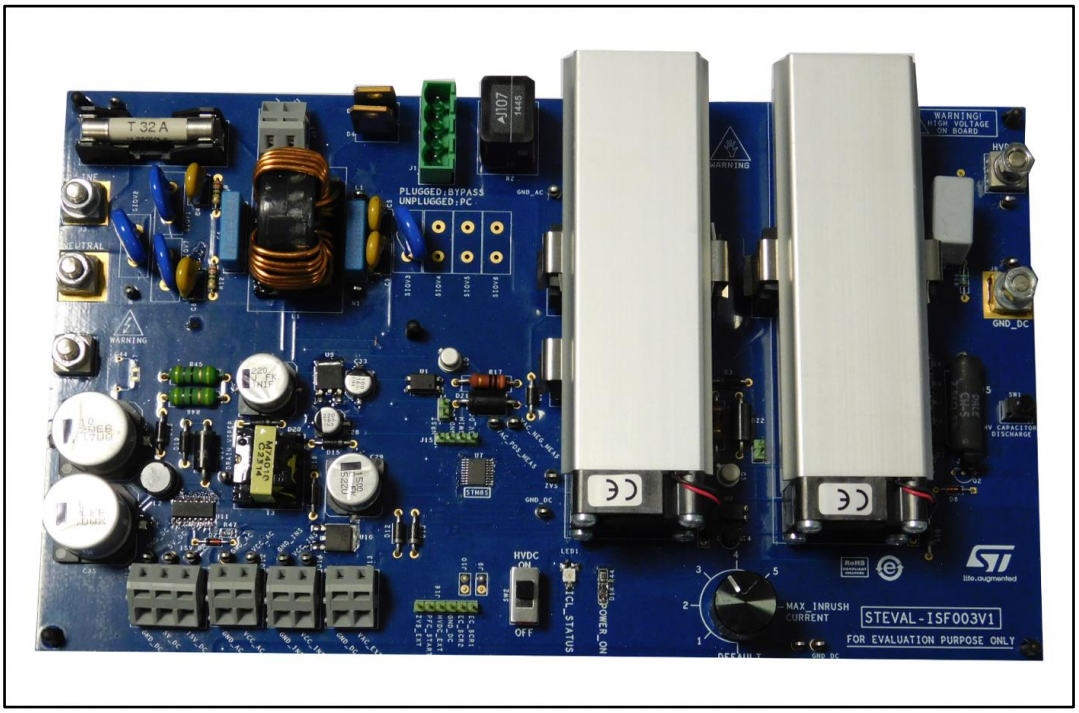
Introduction

The STEVAL-ISF003V1 evaluation board allows the inrush-current which charges a DC bus capacitor to be limited to comply with the IEC 61000-3-3 standard. This inrush-current limitation is based on a soft-start procedure of the mixed bridge diodes and SCRs rectifier using progressive phase control at board start-up.

This solution can also drastically reduce standby losses as the DC bus can be totally disconnected from the AC mains when it does not have to operate. DC bus deactivation is simply achieved by turning off SCRs, without requiring an additional relay to open the circuit in standby.

The steady-state losses are also reduced, thanks to the removal of the NTC / PTC resistor traditionally used to limit inrush-current. Therefore, no relay is required to bypass this resistor as it is no longer used.

Figure 1: STEVAL-ISF003V1 evaluation board (top view)



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1 Evaluation board overview

1.1 What does this evaluation board aim to demonstrate?

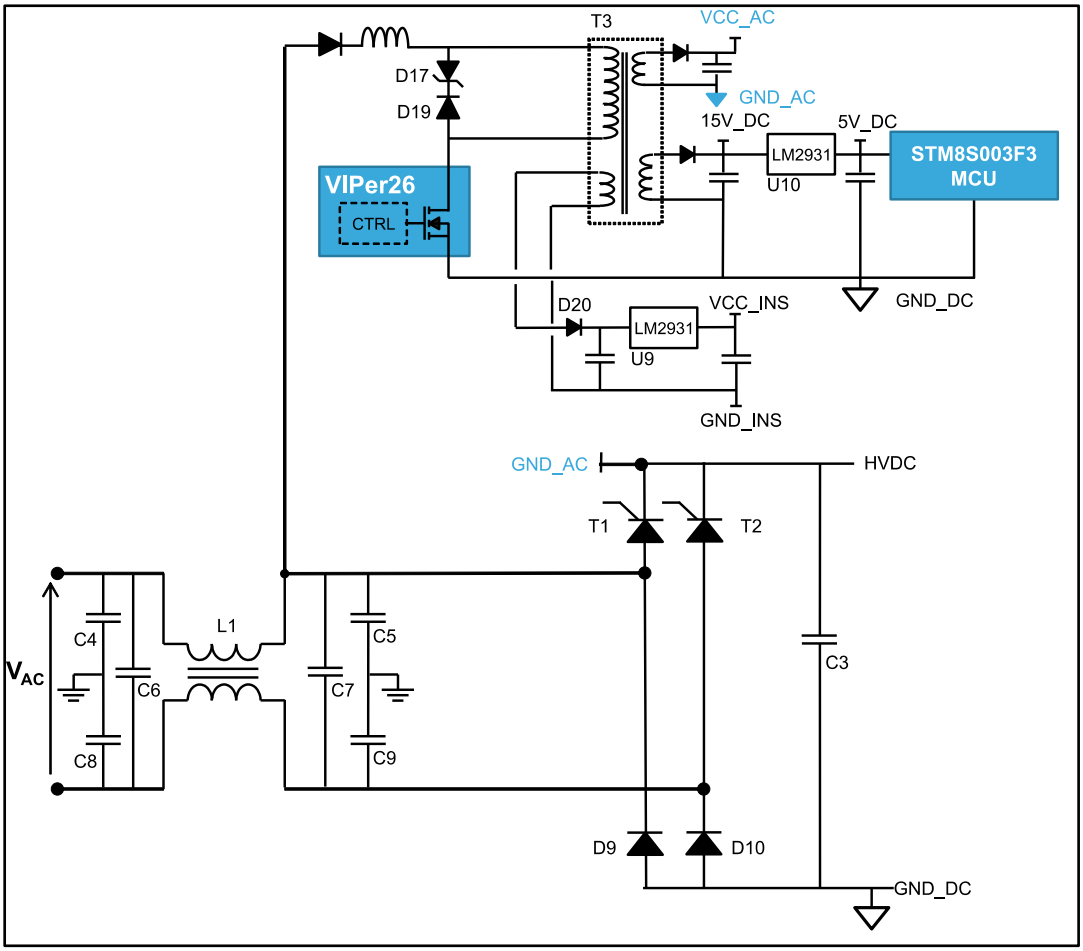
The STEVAL-ISF003V1 is a standalone board designed to demonstrate efficient trade-offs regarding:

- inrush-current limitation without inrush-current resistors
- standby losses in line with ECO European directive

The STEVAL-ISF003V1 board is also a development tool for designing broad inrush-current reduction systems (EV chargers, telecom power supply, etc.). For this purpose, connectors are available for an external power factor corrector, an intelligent power module (IPM), or for an external microcontroller (refer to *Section 2.5: "Possible board variations"*).

1.2 STEVAL-ISF003V1 functional blocks

Figure 2: STEVAL-ISF003V1 functional block diagram



See *Section 3: "Schematic diagrams"* for detailed schematics.

The main sections of the STEVAL-ISF003V1 board are:

1. T1 and T2 silicon-controlled rectifiers (SCRs) in the mixed rectifier bridge.
2. The MCU, which drives SCRs through opto-transistors (see APPENDIX 6) and can also activate any supply or motor inverter referenced to the DC bus ground (GND_DC) in a final application.
3. The flyback power converter providing the sources in the table below.

Table 1: Power sources from flyback converter

Source	Output	Ground	Destination	Maximum output current
VCC_AC	5 V	GND_AC is connected to the HVDC bus	control SCRs (T1 and T2)	200 mA
5V_DC	+5 V	referenced to the DC bus Ground (GND_DC)	MCU and control circuits	90 mA
15V_DC	+15 V	referenced to the DC bus Ground (GND_DC)	can supply an IPM to control a three-phase motor in a final application	500 mA (together with 5V_DC consumption)
VCC_INS	+5 V	insulated output	for components which must be insulated from the mains voltage, (e.g., sensors). Not used on the evaluation board	90 mA

For further information regarding the SMPS outputs, please refer to *Section 4: "STEVAL-ISF003V1 power supplies and typical consumption"*.

1.3 Target applications

Target applications include all those using a diode-bridge to rectify the AC line voltage, where NTC or PTC resistor removal and loss reduction in standby are desirable, such as:

- EV chargers.
- Telecom power supplies.

1.4 Main part numbers

The references of the main part numbers used in this evaluation board are:

- Inrush-current-limiter SCRs: TN5050H-12WY
- Rectifier diodes: STBR6012WY
- Microcontroller unit (MCU): STM8S003F3
- Flyback IC: VIPER26LD

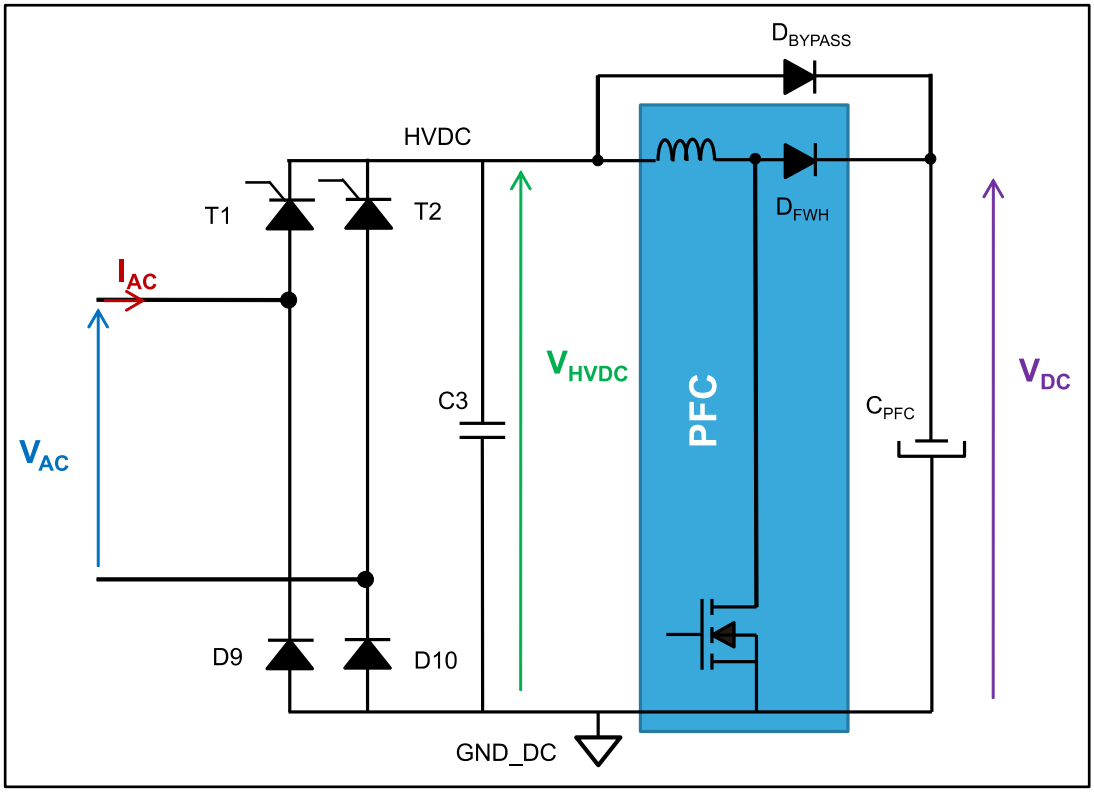
1.5 Operating range

The STEVAL-ISF003V1 board is designed to work in the following operating ranges:

- RMS line voltage range:85 to 264 V_{RMS}
- Line voltage frequency range: 45 to 65 Hz
- Ambient temperature range is: 0 to 60 °C (heatsink fans keep junction temperature of bridge components below T_j max)
- Maximum input current: 32 A_{RMS} (7.4 kW input power for operation on 230 V_{RMS} and 3.6 kW input power on 120 V_{RMS}).

- Allowed DC output capacitor (or DC bus capacitor): up to 2 mF. This value is the equivalent of all capacitors in parallel at the bridge output, like C3 and C_{PFC} at the PFC in the figure below. If an interleaved PFC is used, all the output capacitors of each PFC must be added.

Figure 3: Connection of a PFC at the HVDC output



1.6 Performance characteristics

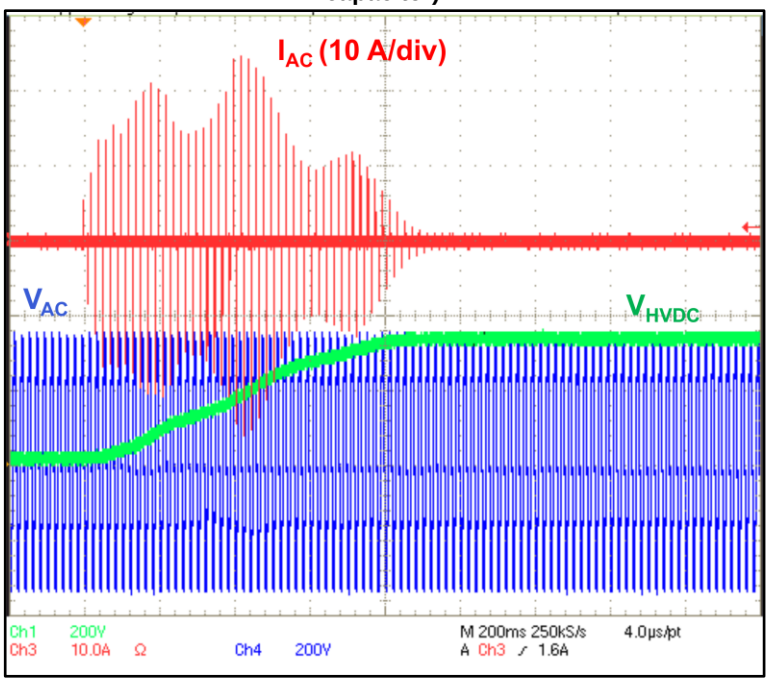
- Efficiency at 230 V 50 Hz 3.3 kW (with output DC resistive load @ COUT = 1mF) > 98%
- Efficiency at 120 V 60 Hz 3.3 kW (with output DC resistive load @ COUT = 1mF) > 98 %
- Standby losses < 300 mW (refer to *Section 1.7: "Standby consumption"*)
- Compliance with IEC 61000-3-3 (with MAX_INRUSH CURRENT potentiometer set to default position, refer to *Section 5: "Inrush-current limitation"*)
- Compliance with EN55014 (CIPSPR 22 method B, refer to *Section 9: "EN55014 test results"*)
- IEC 61000-4-4: 2 kV criteria A, SCR1 and SCR2 withstands a level of 5 kV without triggering. This avoids undesired triggering and uncontrolled inrush-current in case of EMI noise.
- IEC 61000-4-5: 4 kV
- IEC61000-4-11: criteria A for dips down to 100% of the line voltage during 1 cycle; criteria B for interrupts up to 300 cycles or more (refer to *Section 6: "Mains voltage dips and interruptions"*).

The figure below shows an example of the progressive DC capacitor charge which is ensured by SCR1 and SCR2. The test is performed at start-up when the STEVAL-ISF003V1 board is connected to a 230 V, 50 Hz grid (V_{AC}), while the output DC capacitor is

completely uncharged (its initial voltage is null). The output DC capacitor connected to the demonstration board is 1 mF.

The output capacitor is charged over 900 ms while the input RMS current (2.8 A) remains far below the 16.1 A (I_{AC}). The input RMS current easily complies with the IEC 61000-3-3 standard.

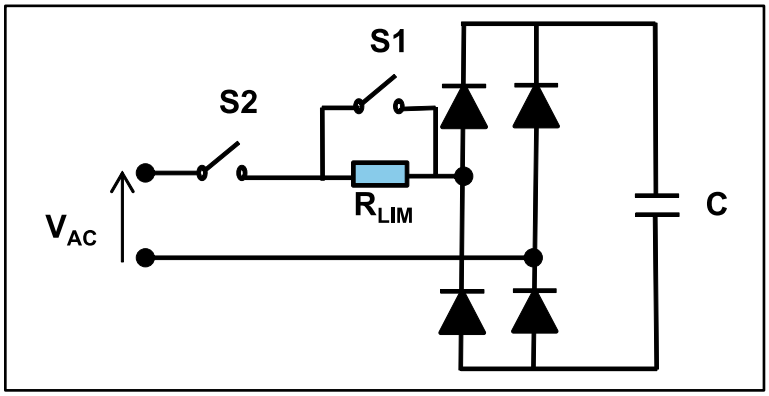
Figure 4: Inrush-current at STEVAL-ISF003V1 start-up on 230 V line (1 mF output DC capacitor)



1.7 Standby consumption

Mixed SCR/Diode rectifier bridges prevent undesirable standby losses through full bridge disconnection by simply turning off the SCRs; this would otherwise require a front-end relay, like S2 in the figure below, to achieve.

Figure 5: Solution using relays to limit the inrush-current and standby losses



To appreciate the benefits of bridge disconnection, we measured the typical losses of the STEVAL-ISF003V1 board in standby mode for the following cases:

1. STEVAL-ISF003V1 board (without modifications) with SCRs in the OFF state (SW2 HVDC switch in OFF position) and the J1 bypass mode jumper is unplugged (PTC not connected).
2. Same as 1, but the following circuits used for demonstration purposes and which consume undesired power in standby are disconnected:
   - HV Capacitor Discharge circuit: R5 and R6 are disconnected from the DC bus
   - D6 HVDC LED: D1 is disconnected from the DC bus
   - D14 POWER_ON LED: R44 is disconnected
3. Same as 2, but the J1 bypass jumper is plugged (PTC connected) to simulate the losses for a conventional solution using only one PTC (EPCOS B59107J0130A020).

Table 2: "Comparison of standby losses" gives the experimental results for the above cases with 230 and 120 V line voltages and a 2-mF HV output capacitor connected to the demonstration board. The test results clearly show that the mixed SCR/Diode bridge rectifier is the only solution with power consumption lower than 0.5 W, as currently required by European directive 2005/32/EC.

The losses on this demonstration board are mainly due to:

- resistors R54, R55 and R56 to discharge the HV output capacitor
- resistors R7 and R9 and the current source to control HVDC LED indicating HVDC voltage
- resistors R6 and R9 to accelerate the HV output capacitor discharge time connected to the demonstration board output
- the other R24, R25 and R28 resistor divider circuit to sense the HVDC voltage

The HVDC voltage is monitored to ensure proper soft-start operation and avoid the DC capacitor charging too long (e.g., a load is kept connected to the DC bus before start-up). In standard circuits, such a voltage sensor is often required (e.g., to start the PFC or the DC/DC supplies).

The losses for a 230 V rectified voltage are:

- 140 mW for the discharge circuit
- 500 mW for the HVDC LED circuit
- 180 mW for the acceleration circuit to discharge the HV output capacitor connected to the demonstration board output
- 52 mW for the HVDC sense.

Table 2: Comparison of standby losses

case	SCR status	PTC status	circuits			power consumption (mW)	
			Power LED	HVDC LED	HV capacitor discharge circuit	V_{AC}=230 V_{RMS}, C_{HVout}=2 mF	V_{AC}=120 V_{RMS}, C_{HVout}=2 mF
1	OFF	OFF	connected			270	200
2	OFF	OFF	disconnected			200	140
3	OFF	ON	disconnected			500	200

2 Getting started

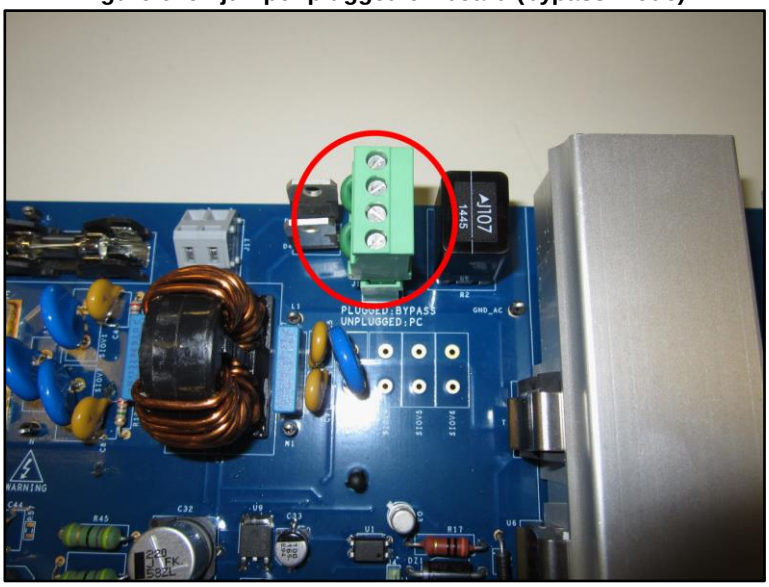
2.1 Safety instructions

The high voltage levels used to operate the STEVAL-IHT008V1 evaluation board may present a serious electrical shock hazard. This evaluation board must be used in a suitable laboratory and only by qualified personnel who are familiar with the installation, use, and maintenance of power electrical systems. The STEVAL-ISF003V1 evaluation board is designed for demonstration purposes only and must not be used for either domestic installation or industrial installation.

2.2 Board connection and start-up

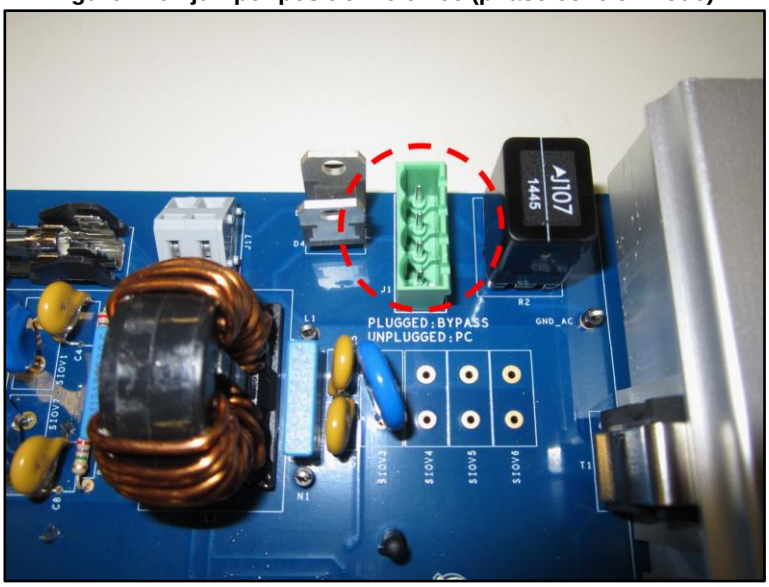
To reduce inrush-current by operating the board with the PTC, plug jumper J1 as indicated by the silk-screen and in the following figure.

Figure 6: J1 jumper plugged on board (bypass mode)



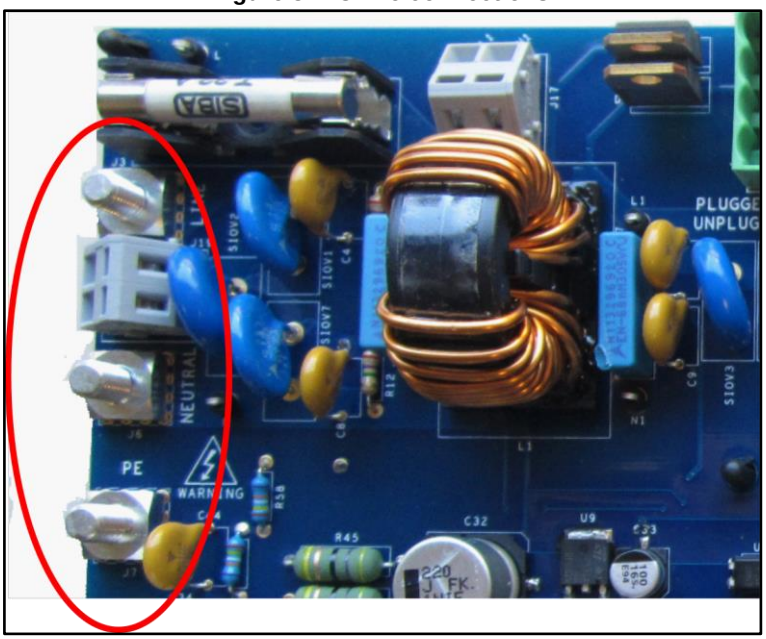
To control the inrush-current with SCRs, do not plug the J1 jumper.

Figure 7: J1 jumper position left free (phase control mode)



Connect L, N and PE (if required) on the respective J3, J6 and J7 headers to an un-powered mains plug.

Figure 8: AC line connections

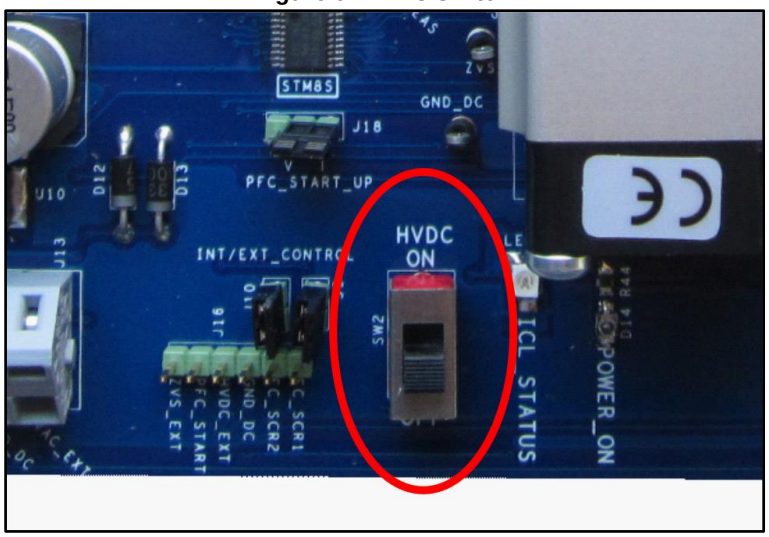


Switch on the mains voltage; from this moment, do not make any contact with live parts under line voltage.

The Power_ON LED lights red to indicate the evaluation board is powered. The ICL-STATUS LED first lights red, then orange, then green and finally turns off to indicate the board is operational. This occurs each time the board is connected to the AC line and the C39 capacitor (5V_DC) is discharged.

Toggle the HVDC switch ON to start charging the DC capacitors.

Figure 9: HVDC switch



When J1 jumper is unplugged, DC capacitor charging can be accelerated if the allowed peak current is increased by rotating the MAX-INRUSH CURRENT potentiometer knob clockwise.

2.3 DC bus capacitor discharge for demonstration purposes

With default STEVAL-ISF003V1 output 47 nF capacitor (C3) and associated 470 kΩ resistors (R54, 55, and R56) used in parallel to discharge the C3 capacitor, the DC bus discharging time is a few milliseconds, if no load is connected.

For larger C3 capacitors, a circuit with MOSFET Q2 and resistor R5 is implemented to accelerate this discharging time, especially when several start-ups are required over a short interval for test or demonstration purposes. Q2 remains on while the SW1 SPDT toggle switch (marked HV CAPACITOR DISCHARGE on the PCB) is set to the momentary ON position.

For a 2-mF C3 capacitor, the full discharge time is around 15 seconds. In this case, the SW1 switch must be kept at the momentary ON position for these 15 seconds, at least.

The D6 LED (marked HVDC on the PCB) remains lit while the HVDC voltage remains above 50 V; as soon as this LED turns off, switch SW1 can be released and a new start-up can begin.

2.4 LED indications

Several status LEDs on the board provide useful information.

- ICL-STATUS (LED D1):
  - On board plug-in, the LED lights red, then orange, then green and finally then off to indicate that the microcontroller has finished the start-up procedure (correct mains connection, line frequency measurement, power supply available, etc.) and the board is ready. The DC output capacitor can now be charged when the HVDC switch (SW6) is toggled ON.
  - Green flashing: the DC bus capacitors are charging (flashing starts when the HVDC switch is toggled ON and ends when the DC bus capacitors are fully charged). This flashing mode can last less than one second and may therefore not be perceived.

  - Green: DC bus is charged to the right voltage.
  - Orange flashing: the DC bus capacitors are charging, but the rate of increase of the output DC voltage is too low. This may occur when a load connected to the HVDC bus sinks too much current for the DC capacitor to charge efficiently.
  - Orange: the LED stops flashing and remains lit orange if the output DC capacitor is not charged to the peak line voltage. This may occur if the bridge is started but a power load is already connected to the HVDC bus and sinks too much current for the DC capacitor to fully charge.
  - Red flashing: the MCU detected an error (e.g., line voltage outside 85 to 264 V operating range or line frequency outside 45 to 65 Hz operating range).
- HVDC (LED6): lights red when the voltage between HVDC and GND_DC terminals is higher than 50 V (refer to *Section 2.3: "DC bus capacitor discharge for demonstration purposes"*).
- POWER_ON (LED14): lights when the AC line is plugged to the AC line.

2.5 Possible board variations

The STEVAL-ISF003V1 board allows some external components to be added to the front-end circuit so designers can evaluate entire systems.

2.5.1 EMI filter and DC bus capacitor alteration

The EMI filter and DC capacitors are simple through-hole devices so they are easy to change. This allows a designer to adapt the EMI filter and HVDC voltage ripple to specific application requirements (e.g., the power rating).

However, if these components are modified, the SCR control law must be updated to maintain IEC 61000-3-3 compliance. This can be done by adjusting the maximum peak current during start-up with the MAX-INRUSH CURRENT potentiometer. When this potentiometer is turned clockwise, the SCRs are turned on sooner (according to the AC line polarity) at each half-cycle, leading to a higher peak current.

Maximum RMS current or voltage fluctuation (if a normalized line impedance is used) must then be measured according to the potentiometer position to check IEC 61000-3-3 compliance.

If the EMI filter capacitor (C4 to C9) values are increased, R10 and R12 values may be decreased to ensure that the capacitors still discharge down to a safe voltage (120 V for DC voltage) in less than one or two seconds. Indeed, the EMI filter capacitor voltage is applied to the power plug when the board is unplugged and, if the power terminals have accessible live parts, you may be vulnerable to electric shock.

2.5.2 Power factor circuit connection

A PFC can be connected on the HVDC bus via the HVDC (J2) and GND_DC connections (J8). Capacitor C3 must be unsoldered by using a 630 V DC film capacitor if needed.

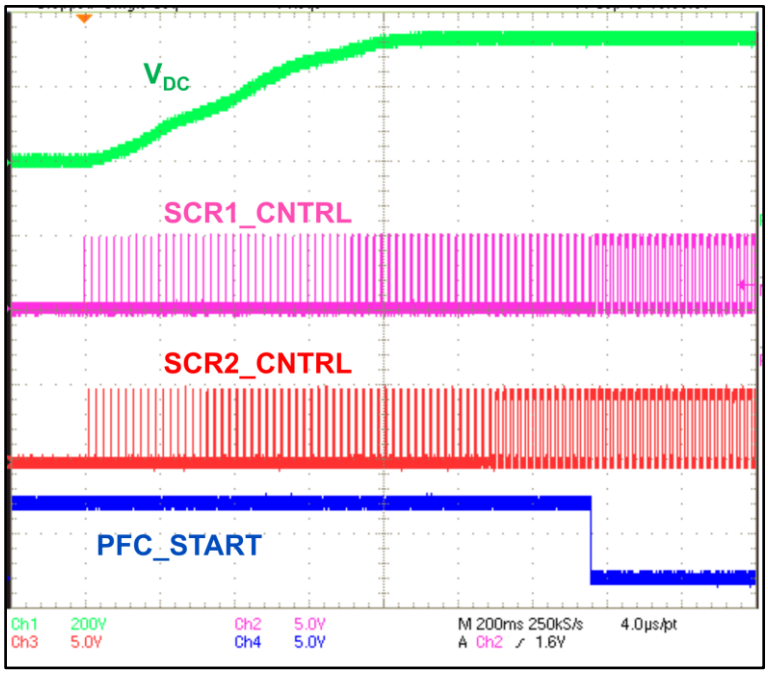
As SCRs are alternately controlled by a DC gate current (according to AC line polarity), when the HVDC voltage reaches its steady-state value, either a discontinuous mode or a continuous mode PFC can be used.

For proper STEVAL-ISF003V1 front-end circuit operation, the PFC must be activated after the PFC_START signal is set to a low level (refer to *Figure 10: "PFC activation permission (PFC_Start signal) when the HV output capacitor is charged"*, indicating that the PFC HV output capacitor is charged. This signal is referenced to GND_DC terminal and is available from the J16 header.

The PFC_START signal is an open drain output that must be compatible with the digital rail used by an external system. The PFC DC storage capacitor (C_{PFC} in *Figure 3: "Connection of a PFC at the HVDC output"*) must be inside the range specified in *Section 1.5: "Operating range "*.

Connector J13 gives the rectifier AC line voltage and can be used to by an external PFC to shape the input current waveform.

Figure 10: PFC activation permission (PFC_Start signal) when the HV output capacitor is charged



2.5.3 Motor inverter connection

An inverter or any other DC/DC power converter can be added after the PFC or directly behind the HVDC bus output.

A 15 V positive output referenced to the DC Bus Ground (GND_DC) is available on header J11 to supply an IPM module if needed. The maximum current sunk from this supply must be well below the limit.

2.5.4 Control with an external microcontroller

You can control the STEVAL-ISF003V1 front-end circuit with an external MCU instead of the embedded STM8S003F3 MCU to directly check the compliance of your own firmware with this kind of circuit.

All the control signals required to drive the SCRs are available on the J16 header. EC_SCR1 and EC_SCR2 are the connections to externally drive SCR1 and SCR2, respectively. GND_DC of the DC bus ground and the ZVS_ext signal (to synchronize the control signals of the external MCU) are also available on this header.

For correct operation with external signals, Jumpers J9 and J10 (marked as INT/EXT_CONTROL on the PCB) must be removed to disconnect the opto-transistor input

LEDs from the U7 microcontroller outputs (see SCRs gate ctrl section in *Section 3: "Schematic diagrams"*).

It is also possible to control the STEVAL-ISF003V1 front-end circuit with an external MCU by using the embedded STM8S003F3. In this case, the inrush-current limitation is managed by the embedded STM8S003F3 MCU. The control signal required to start the inrush-current limitation is available on J16 header (HVDC_EXT).

The input HVDC_EXT signal is 3.3 V/5 V compatible.

3 Schematic diagrams

Figure 11: STEVAL-IFS003V1 power and insulated control schematic

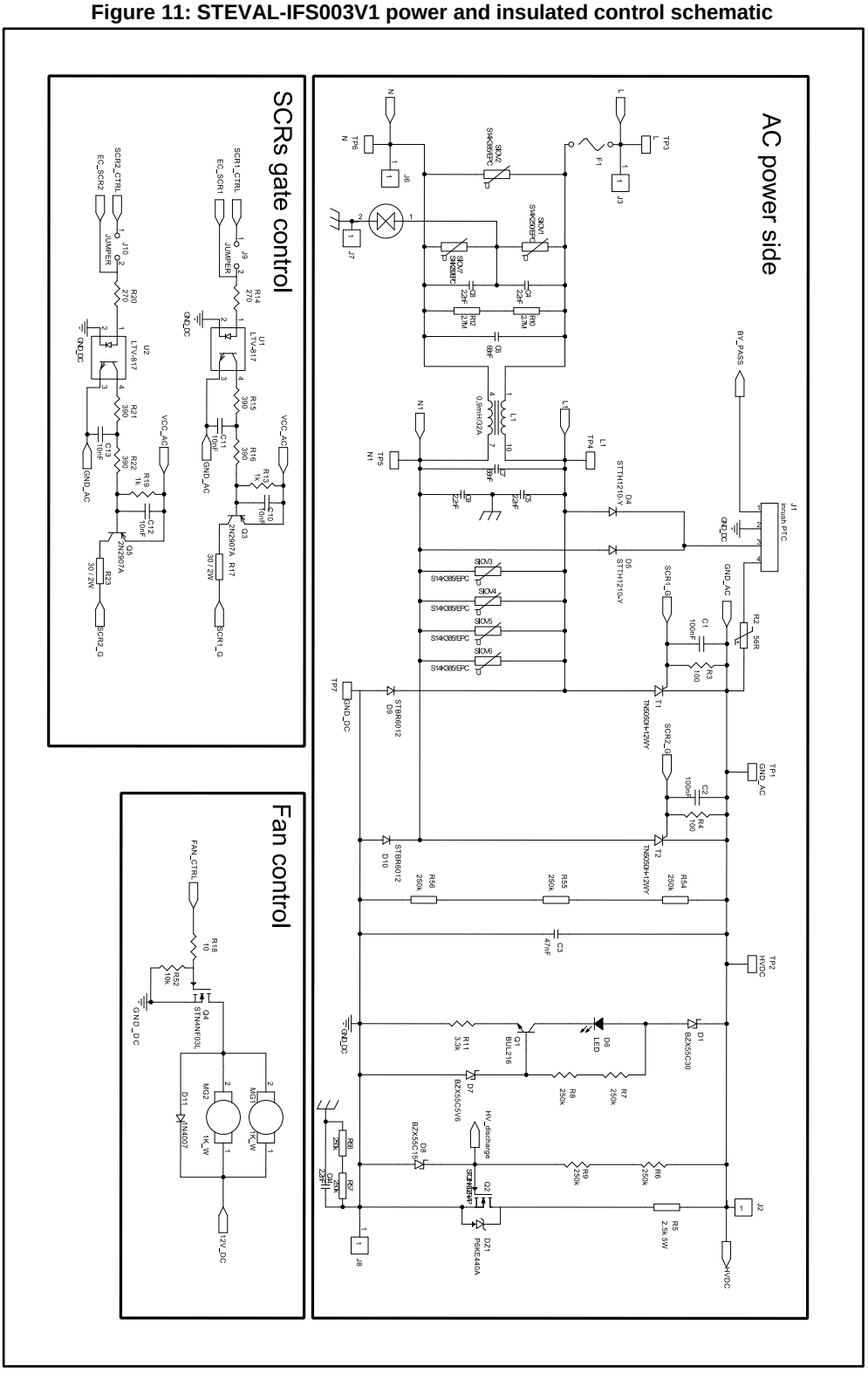


Figure 12: STEVAL-ISF003V1 control circuit schematic

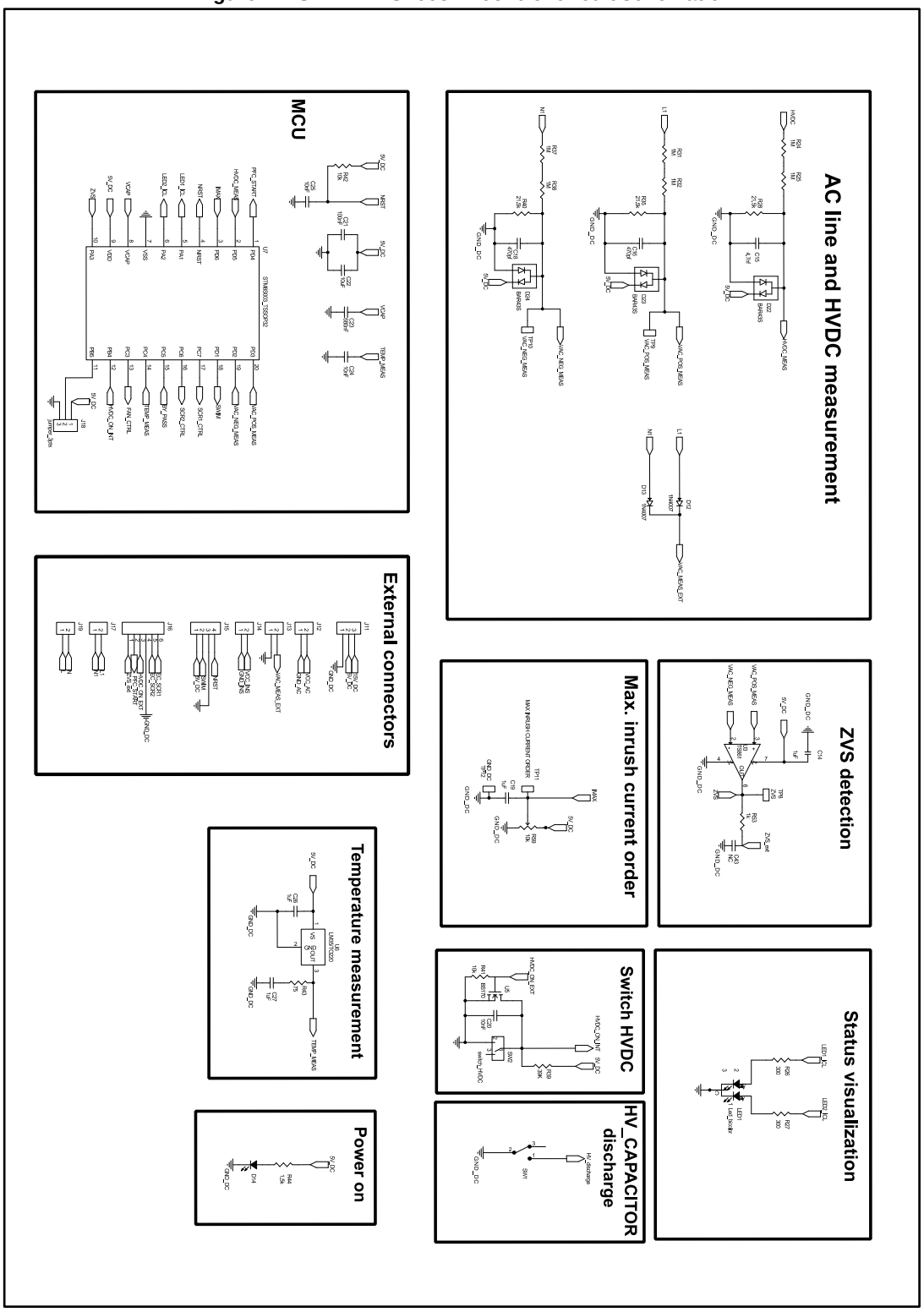
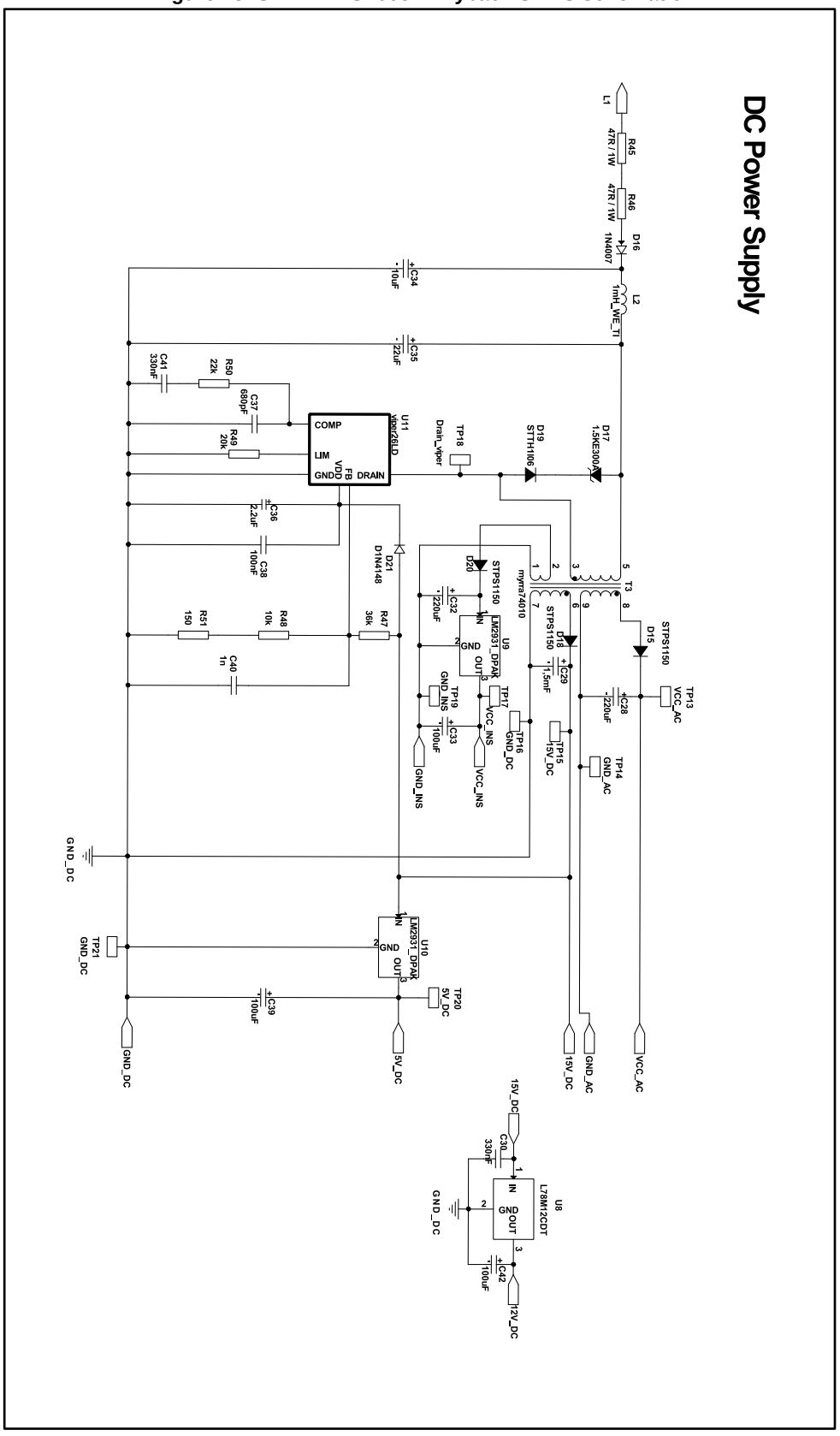


Figure 13: STEVAL-ISF003V1 flyback SMPS schematic



4 STEVAL-ISF003V1 power supplies and typical consumption

The table below gives the typical current consumed from the 5V_DC output for the different STEVAL-IFS003V1 operating modes.

Table 3: Typical STEVAL-ISF003V1 control-circuit consumption

Operating mode		Current sunk from 5V_DC (mA)
MCU in standby mode (SCRs off)	Power_ON LED connected	2.9
	Power_ON LED not connected	0.7
MCU in standby mode (SCRs on)	Power_ON LED connected	27.6
	Power_ON LED not connected	25.4

Table 1: "Power sources from flyback converter" lists the following flyback output supplies:

- a non-regulated 5 V VCC_AC supply for SCR control
- +15 V and +5 V supplies (15V_DC and 5V_DC outputs) supply circuits referenced to the DC bus Ground (MCU, IPM if added)
- a +5 V insulated supply (VCC_INS/GND_INS) for sensors if needed, this output is not implemented by default

Only the +15 V output is regulated by the VIPer26LD circuit, as this supply is always loaded when the other outputs are loaded. The two +5 V supplies (5V_DC, VCC_INS) are also regulated thanks to two LM2931 positive voltage regulators.

The VCC_AC level is not regulated: its voltage level will be higher if it is not loaded and if the +15 V supply is loaded with its maximum current.

The current capabilities of the different outputs are (for the whole operating range):

- For 5V_DC: 90 mA
- For VCC_AC (non-regulated 5 V negative output): 200 mA
- For 15V_DC: 500 mA (with 5V_DC consumption included)
- For VCC_INS (optional 5 V regulated output): 90 mA

A +12 V supply is implemented to supply the fan to control the SCR/diode rectifier bridge temperature; it is regulated through the L78M12 device from the 15V_DC positive supply.

The two figures below give the typical output voltage according to the current sunk from each output. The measurements were taken with the STEVAL-ISF003V1 connected to 230 V and 120 V lines for the whole temperature operating range (0 to 60 °C). The 15 V_DC, and the 5 V outputs (5V_DC and VCC_INS) are well regulated by the VIPer26LD and LM2931 devices, respectively.

For the VCC_AC, four curves provide the minimum and maximum values of this output when the MCU and fan are ON and OFF, respectively. For these two cases, the minimum voltage is reached when no current is sunk from the 15V_DC, and the maximum voltage is reached when a 500 mA maximum current is sunk from the 15V_DC.

Figure 14: Typical output characteristics of the 5 V and 15 V positive supplies (5V_DC/15V_DC)

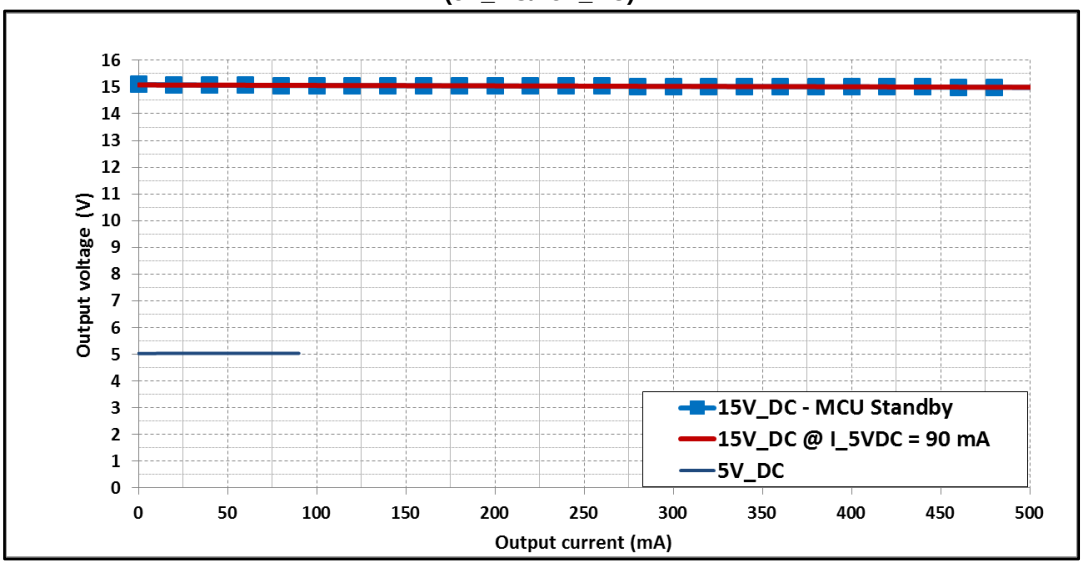
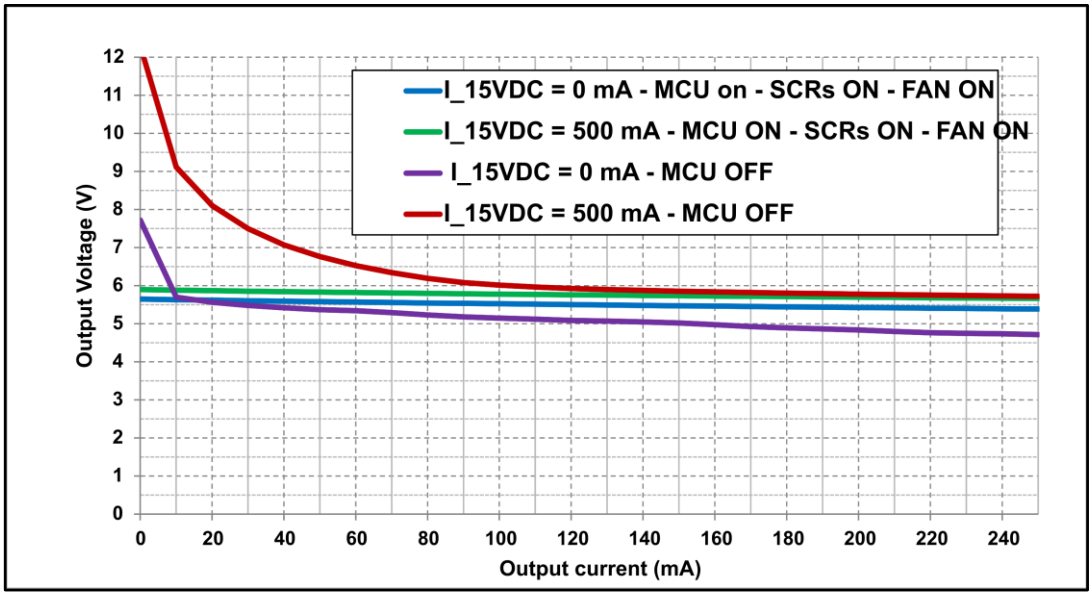


Figure 15: Typical output characteristics of the 5 V positive supply (VCC_AC)



5 Inrush-current limitation

5.1 IEC 61000-3-3 overview

The IEC 61000-3-3 standard gives the limitation of voltage changes and fluctuations for equipment with rated RMS current lower than 16 A connected to a public low-voltage grid. These voltages fluctuations are caused by the equipment when the current sunk from the grid is too high, resulting in a voltage drop due to the line impedance.

The mains voltage fluctuation causes undesired brightness variation in lamps and displays, known as “flicker”. This is why designers must keep the inrush-current sunk by their equipment down to specific limits.

The following equation explains the link between the line current variation δI_{input} (due to the equipment operation) and the relative mains voltage variation (δU) which must drop to a maximum allowed value (d_{max}, given in %).

Where Z_{ref} is the normalized line impedance (0.6 Ω with 796 µH in series for a single-phase grid) and U is the nominal RMS line voltage

The d_{max} level shall not exceed 4 %. A 6% or 7% limit is also allowed according to the way the equipment is switched (manually or automatically, delayed or not, etc.) or for specific appliances.

A δU variation exceeding 3.3 % during a single voltage change should not last more than 500 ms.

The table below gives the associated maximum input current variation related to these different d_{max} levels. To simplify the analysis, we can say that an appliance fulfils the IEC 61000-3-3 limit at start-up if its RMS current remains below 16.1 A. The relative variation is then lower than 3.3% and so the compliance is ensured even if the start-up lasts more than 500 ms. This is clearly a restricted case for simplification purposes; higher current variations may also allow compliance with this standard.

Table 4: Maximum input RMS current variation for 230 V single-phase grid according to IEC 61000-3-3

d_{max} (%)	δU (V)	δI_{input} (A)
3.3	7.6	16.1
4	9.2	19.5
6	13.8	29.3
7	16.1	341

5.2 STEVAL-ISF003V1 compliance with the IEC 61000-3-3 limit

One of the most common solutions to limit inrush-current involves adding a resistor (like R_{LIM} in *Figure 5: "Solution using relays to limit the inrush-current and standby losses"*) in series with the DC capacitor (C in the same figure). This resistor must then be bypassed to limit power losses during steady-state operation, usually with a relay or a Triac (S1). To disconnect the DC bus during standby mode, a second switch (S2) is required.

To avoid using an R_{LIM} resistor, a different start-up procedure can be implemented. With the mixed SCR/diode rectifier bridge, the capacitor can be smoothly charged with progressive phase control. The bridge does not conduct any current and the DC bus capacitor is not charged while the SCRs are not triggered. To start charging the DC

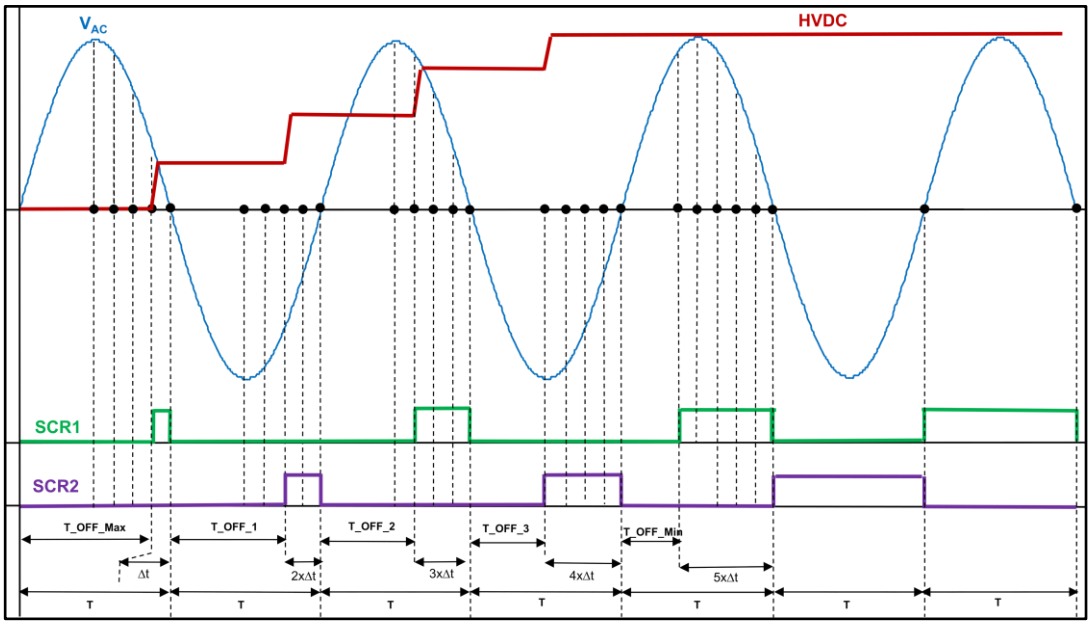
capacitor, SCR1 and SCR2 must be turned on according to the AC line voltage polarity (SCR1 is turned on when the AC line polarity is positive and SCR2 is turned on when the AC line polarity is negative). To reduce the inrush-current, SCR are alternately first triggered at the end of the line voltage cycle, just few hundred microseconds before the line zero voltage. This allows the output capacitor (C in *Figure 5: "Solution using relays to limit the inrush-current and standby losses"*) to be charged to a low level (around 10 to 30 V) and not directly to the peak line voltage. The current driven from the line is therefore much lower than for direct full-charging of the DC capacitor.

This soft-start solution can only work with an inductor on the line side as the rate of current increase must also be limited to avoid SCR damage. Such an inductor is already present for most applications, whereby the EMI filter usually embeds a common-mode choke which has a differential-mode parasitic inductor due to the copper turns of the windings. In our STEVAL-ISF003V1, the EMI filter involves C6-C7 X2 capacitors, C4-C8-C5-C9 Y2 capacitors, and an L1 common-mode inductor. This inductor features a 0.9 mH value in common-mode but also a 3 µH inductor in differential mode.

To completely charge this capacitor to the peak line voltage, the SCRs must be triggered on the following cycle with a shorter turn-on delay than the first one used to start charging (refer to *Figure 16: "HV capacitor charging controlled"*). Thus by reducing SCR turn-on delay by a few ten or hundred microseconds from half-cycle to half-cycle, the output capacitor is progressively charged while the line current is kept low. In STEVAL-ISF003V1 MCU firmware, the step of SCR turn-on delay reduction is constant from one half-cycle to the next. This step is called `Step_Phase_Control_µs` in the firmware. It is set by the `Max_Inrush_Current_Order` routine which reads the voltage set by the MAX_INRUSH CURRENT potentiometer.

The SCRs are turned on typically 100 µs after the VAC zero voltage. This value is defined by `SCRs_ON_Delay_us` in the firmware.

Figure 16: HV capacitor charging controlled



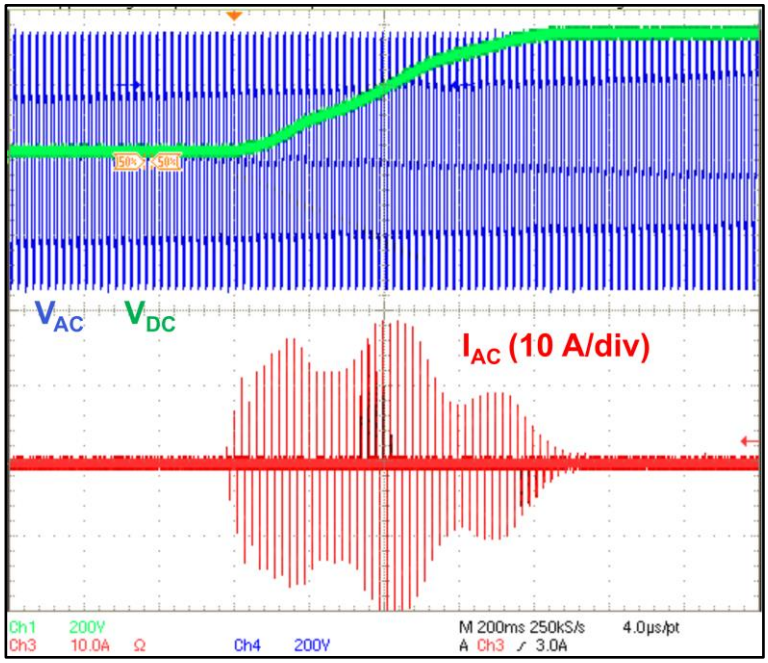
When the SCR turn-on delay is lower than 3 ms, the SCR gate pulse is directly set to a continuous DC pulse according to the AC line polarity (SCR1 is set to a continuous DC pulse when the AC line polarity is positive and SCR2 is set to a continuous DC pulse when the AC line polarity is negative). Indeed, below an approximate 5 ms or 4.2 ms delay (for 50 and 60 Hz line frequency, respectively), the output DC capacitor is fully charged, so it is

not necessary to ensure a soft-start for turn-on delays much lower than a fourth cycle. In the firmware, a minimum value of 3 ms is defined by the `Phase_Control_ON_Max_µs`, which sets the maximum ON time of SCRs (7 ms, refer to directive definitions in the firmware).

The figure below (and *Figure 4: "Inrush-current at STEVAL-ISF003V1 start-up on 230 V line (1 mF output DC capacitor)"*) shows an example of such progressive DC capacitor charging. The test is performed at start-up when the STEVAL-ISF003V1 board is connected to a 230 V 50 Hz grid, while the output DC capacitor is fully uncharged (i.e., its initial voltage is null), with a 1mF output DC capacitor connected.

The electrical parameters in the figure below are defined in *Figure 3: "Connection of a PFC at the HVDC output"* (arrow head gives the hot-point of the voltage). As no PFC is used, VDC is actually the voltage across the 1mF capacitor connected to the HVDC output.

Figure 17: SCR current zoom for the highest peak current during start-up



With the MCU firmware as the default program:

- First SCR turn-on is set to 150 µs before next line zero voltage, as the first gate current pulse lasts 50 µs. This allows the gate current to be removed 100 µs before next half cycle. This value is set by `SCRs_OFF_Delay_us` in the firmware. This 100 µs time margin takes into-account the ZVS signal delay (which could equal up to 50 µs, see *Section 7: "AC voltage monitoring and zero-voltage synchronization"*) and the delay required to un-saturate transistor Q3 or Q5 which drives the SCR1 and SCR2 (50 µs), respectively. Total delay time equals 150 µs, called `ICL_TRIAC_OFF_Delay_µs` in the firmware.
- SCR turn-on then progressively occurs 50 µs sooner when the MAX_INRUSH CURRENT potentiometer is set to the DEFAULT position. This minimum step value is defined in the directive section of the firmware (refer to `Step_Phase_Control_Min`). The DEFAULT position corresponds to the slower output DC capacitor charge, thus the shortest `Step_Phase_Control_µs` value. When the MAX_INRUSH CURRENT

potentiometer is turned clockwise from point 1, the Step_Phase_Control increases roughly linearly from around 50 µs (position 1) to 600 µs (position 6).

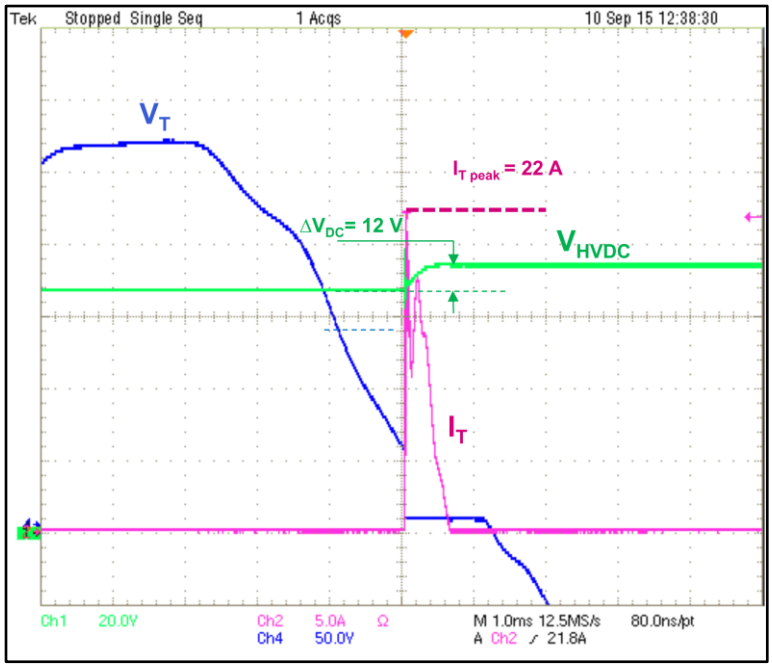
- When the SCR Triac turn-on delay is lower than 3 ms, SCR1 and SCR2 are triggered by a DC gate current according to the AC line voltage polarity.

The figure above (and *Figure 4: "Inrush-current at STEVAL-ISF003V1 start-up on 230 V line (1 mF output DC capacitor)"*) shows a maximum inrush peak current around 22 A. The RMS current is thus far below the 16.1 A limit. This means that the relative variation is below 3.3% and so checking the duration of the accumulated time of deviation exceeding 3.3 % is not required. The output capacitor is charged in 900 ms and compliance with the IEC 61000-3-3 standard is fulfilled.

The peak current during output capacitor charging is not constant; indeed, only the step reduction of the SCR turn-on delay is constant. Hence, according to the time this SCR turns on, the peak current can vary slightly from one period to another.

Note that we have limited the inrush peak current to below 22 A, but the IEC 61000-3-3 limit applies to the RMS current. As the SCRs conduct a few hundred microseconds at each half-cycle, the RMS current is much lower than the peak value. The figure below shows the Triac current for the highest peak current event measured in *Section 5.2: "STEVAL-ISF003V1 compliance with the IEC 61000-3-3 limit"*. The Triac conduction lasts 700 µs; its RMS current equals then 2.8 A, which is much lower than the measured 22 A peak current. The output DC voltage increases by 12 V during this single Triac conduction.

Figure 18: Triac current for the highest peak current during start-up



6 Mains voltage dips and interruptions

The IEC 61000-4-11 standard defines the tests to evaluate equipment immunity to a voltage dip or interrupt and is referenced by other standards. Product standards like EN55014-2 for appliances or EN 55024 for IT equipment sold on the European open market list tests to be performed according to IEC 61000-4-11 standard and expected results. The general electromagnetic standard is applied according to the use environment (e.g., residential or industrial environment for example) for products not listed in a specific standard.

As any appliance connected to the mains can suffer line voltage dips or interruptions, high input currents may occur when line voltages suddenly return to their nominal values for rectifier circuits charging DC capacitors. This high current may damage front-end components like bridge diodes, AC fuses, etc.

Table 5 Dip and interruption tests and STEVAL-ISF003V1 performance gives the different requirements in terms of line voltage dips and interruptions for the different electromagnetic immunity standards, and corresponding test results.

These tests results only apply to the inrush-current limitation function (SCR control).

The worst cases to take into account are:

- Voltage dips: 1 cycle with a 0% residual voltage, and 50 cycles with a 70% residual voltage
- Voltage interruptions: 0% residual voltage during 250 or 300 cycles respectively for 50 and 60 Hz line frequency.

Criteria B is requested for the 0% voltage test during 1 cycle, while the other tests only require only criteria C.

Table 5: Dip and interruption tests and STEVAL-ISF003V1 performance

Standard	Application	Test type	% residual voltage	Number of cycles	Required criteria by standard	STEVAL-ISF003V1 result
IEC 61000-6-1	Residential, commercial and light-industrial environments	Dips	0	0.5	B	A
			0	1	B	A
			70	25(1)/30(2)	C	A
		Interruptions	0	250(1)/300(2)	C	A
IEC 61000-2-1	industrial environments	Dips	0	1	B	A
			40	10(1)/12(2)	C	B
			70	25(1)/30(2)	C	A
		Interruptions	0	250(1)/300(2)	C	B
EN 55024	information technology equipment	Dips	less than 5	0.5	B	A
			70	25	C	A
		Interruptions	less than 5	250	C	B
EN 55014-2	Appliances, electric tools, etc.	Dips	0	0.5	C	A
			40	10	C	B
			70	50	C	A

Notes:

(1)50 Hz line frequency

(2)60 Hz line frequency

The STEVAL-ISF003V1 board MCU firmware is programmed to comply with these different tests thus:

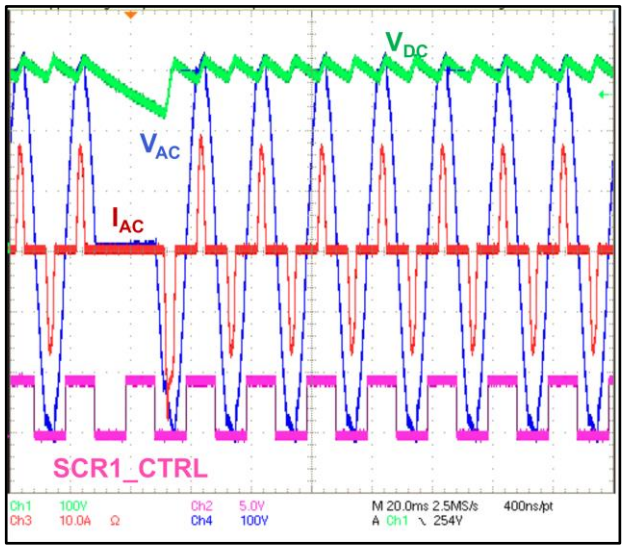
- If the line voltage remains higher than 70% of the reference voltage (measured at board start-up), no change applies to the SCR (T1 and T2) sequence.
- If the line voltage falls below 70% of the reference voltage during at least 1.5 cycles, SCRs (T1 and T2) are switched off. The DC bus voltage is discharged by its load current. When the line voltage is reapplied, the SCRs are controlled back in soft-start to ensure recharging current limitation. Clearly, SCR restart only occurs if the HVDC ON SPST switch (SW2) is kept at the ON position. Note that the 1.5 cycle duration to detect voltage dip that lasts too long is given by the parameter `Nb_Peak_VAC_Dips`, which is set to three by default (three times the measured low peak AC voltage). The ratio of voltage decrease from which an undervoltage is taken into account is set by the parameter `VAC_Variation_Dips` in the firmware (the default value is 0.3 for 30% maximum mains voltage reduction).

The same table also provides the test results of the STEVAL-ISF003V1 inrush-current-limitation function (i.e., SCR control). Criteria A is ensured for all dips, even with a 0% residual line voltage, shorter than 1 cycle. Criteria B is ensured for longer interruptions, including 300 cycles or more. The STEVAL-ISF003V1 board performance therefore comfortably exceeds international standard requirements.

The following figures illustrate board behavior at 230 V with a 1000 W DC resistive load, for two different voltage dips with a 0% residual voltage applied over 20 ms (*Figure 19: "Board operation during 1-cycle line interruption"*) and 40 ms (*Figure 20: "Board operation during 2-cycle line interruption"*).

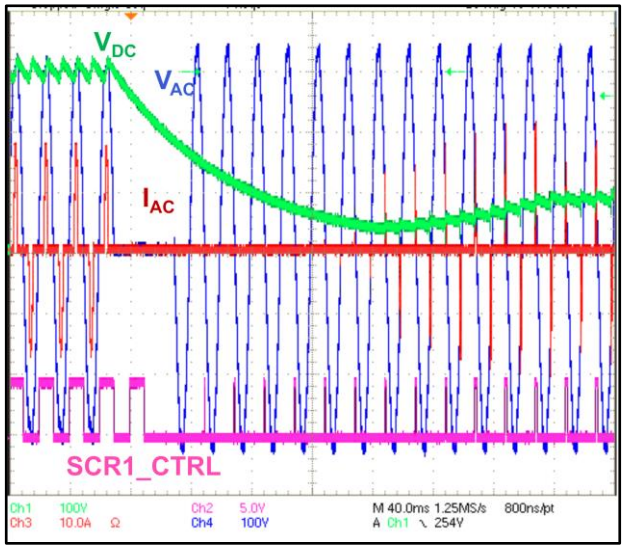
In the former, the SCRs are kept ON during the line interrupt. When the voltage is reapplied, the peak current is only 30 A as the DC voltage only decreased by 60 V during the lack of AC voltage. Only the SCR1 control is defined in this waveform.

Figure 19: Board operation during 1-cycle line interruption



In the latter, as the interrupt lasts more than 30 ms, the SCRs are retriggered when the AC voltage is reapplied. To avoid an excessive inrush-current due to a long interrupt, the SCRs are controlled in a soft-start procedure like for any system start-up. The DC capacitor therefore starts being recharged when the SCR gate current is applied while the AC voltage is higher than the C voltage. In the figure below, this point occurs around 45 ms after the line voltage is reapplied. The peak current is therefore only 27 A, which is only around 1.5 times the nominal current and well below any component damage levels.

Figure 20: Board operation during 2-cycle line interruption



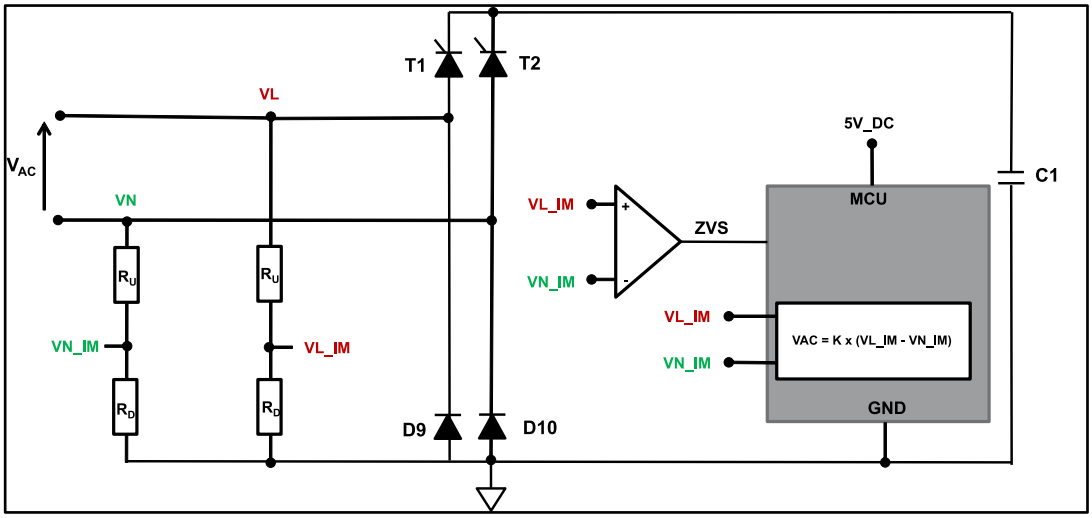
7 AC voltage monitoring and zero-voltage synchronization

7.1 Zero voltage and AC line voltage sensor circuits

The AC line voltage (V_{AC}) must be measured to detect the RMS AC line voltage level and to manage the AC line dips (as described in *Section 6: "Mains voltage dips and interruptions"*). As the MCU is connected after the diode bridge, a differential measurement must be performed to measure the AC line voltage (V_{AC}). The V_{AC} measurement is based on the line voltage (V_L) and the neutral voltage (V_N) measurement ($V_{AC} = V_L - V_N$).

The resistor divider bridge in the following figure id used to sense V_L and V_N.

Figure 21: AC line voltage measurement principle



Given V_L and V_N images, the MCU is able to deduce V_{AC} from Equation 1, where V_{AC_IM} is the image of the AC line voltage and K is the proportional coefficient between V_{AC} and V_{AC_IM} defined by the resistors divider bridge.

Equation 1

$$V_{AC} = (V_L - V_N) = K \times (V_{L\_IM} - V_{N\_IM}) = K \times V_{AC\_IM}$$

Equation 2 shows how to calculate resistance R_D from chosen resistance R_U, where $V_{AC\_RMS\_Max}$ is the maximum RMS AC line voltage which can be applied in the application and $V_{AC\_IM\_Max}$ is the maximum AC line voltage image voltage applied at the MCU ADC input.

Equation 2

$$R_D = R_U \left\{ \left(\frac{V_{AC\_IM\_Max}}{(\sqrt{2} \times V_{AC\_RMS\_Max}) - V_{AC\_IM\_Max}} \right) \right\}$$

Equation 3 gives the proportional coefficient between V_{AC} and V_{AC_IM}

Equation 3

$$K = \left(\frac{(R_U \times R_D)}{R_D} \right)$$

For example, with R_U = 2 MΩ, $V_{AC\_RMS\_Max}$ = 264 V, and $V_{AC\_IM\_Max}$ = 4 V, the following resistor and K values should be used (a 1% resistor tolerance is recommended):

- R_U = 2 MΩ
- R_D = 21.5 kΩ
- K=94.025

The actual resistor bridge values in the ICL board schematic are:

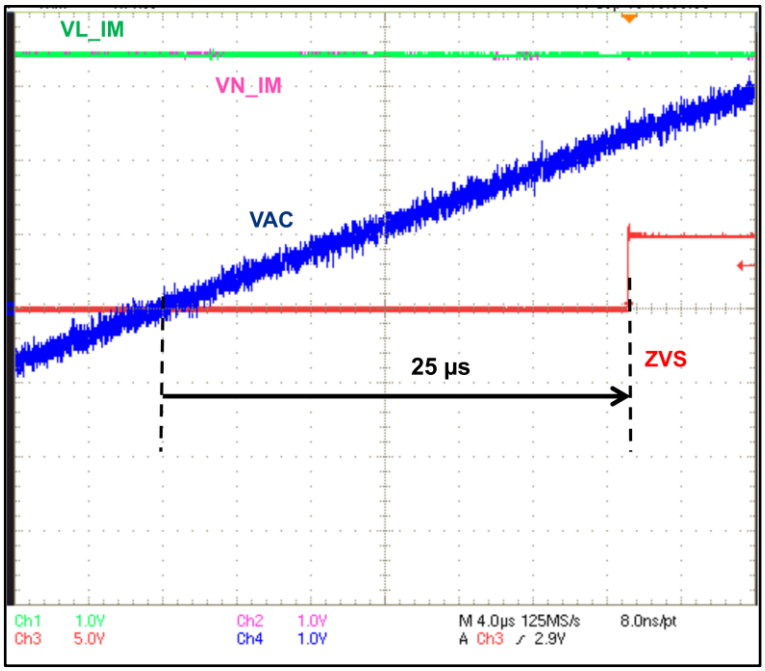
- $R_U/2 = R_{31} = R_{32} = R_{37} = R_{38}$ = 1 MΩ
- $R_D = R_{35} = R_{40}$ = 21.5 kΩ
- K=94.025

7.2 Zero AC line voltage detection

The SCR phase-control needs to be synchronized with the AC line voltage. The zero AC line voltage crossing detection uses the AC line voltage measurement. Indeed, the zero AC line voltage occurs when the line voltage (V_L) and the neutral voltage (V_N) are equal. In this case, a comparator (U3) connected to the pin 10 of the MCU, compares voltages V_{L_IM} and V_{N_IM}. As soon as V_{L_IM} is lower than V_{N_IM}, the output comparator switches to the low level, as shown below. This figure shows that the typical delay between the ZVS signal and the real V_{AC} zero is 36 µs for a 230 V 50 Hz grid voltage.

A 470 pf capacitor is added in parallel with resistors R35 and R40.

Figure 22: Zero AC line voltage crossing detection



8 SCR switch insulated control

The VIPer26LD Flyback provides a DC output voltage to control SCR1 (T1) and SCR2 (T2). The GND terminal (GND_AC) of this output is connected to the HVDC. The high terminal of this output is called VCC_AC.

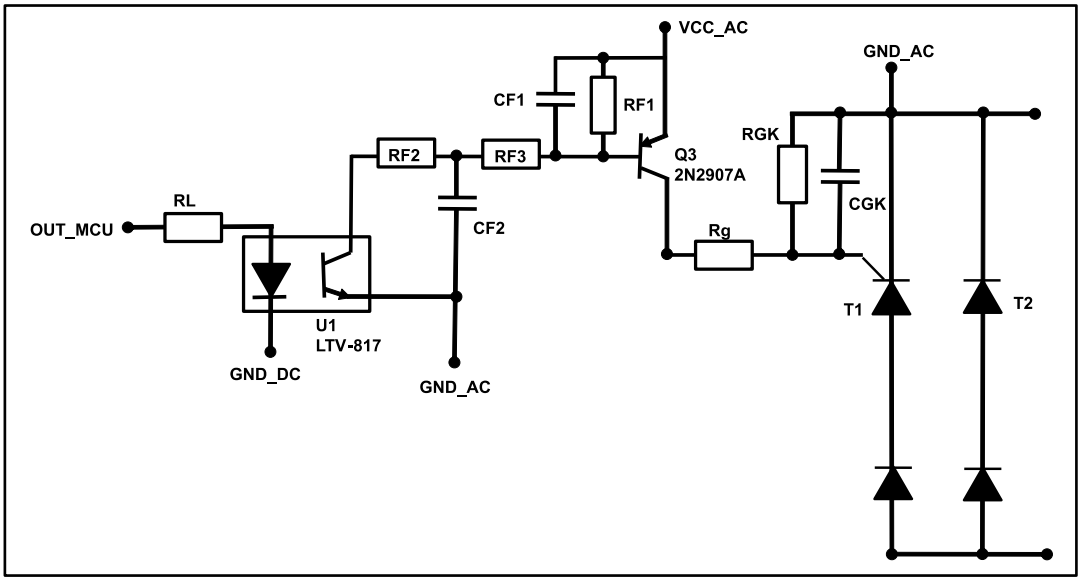
A positive supply is required to source the current to the SCR gates.

As the MCU is not on the same ground reference as the SCRs, optocouplers are needed to control them. To control T1 SCR switch, optocoupler (U1) associated with a PNP transistor (Q3) is used as per *Figure 23: "SCR switch insulated control"*.

Moreover, to improve the circuit control immunity:

- An RC filter is connected between the base and the emitter of the PNP transistors (RF1 = 1 kΩ and CF1 = 10nF).
- A capacitor associated with resistors RF3 and RF4 is used to improve optocoupler U1 immunity.

Figure 23: SCR switch insulated control



The gate resistor (Rg) to limit the given the SCR gate current (I_{GT}) can be defined according to Equation 4, where VCC_AC is the power supply to provide the gate current to the SCRs, VCE_SAT_{PNP} is the transistor collector-emitter of the PNP transistor, V_{GK} is the SCR gate triggering voltage and R_{GK} is the gate cathode resistor used to improve SCR immunity.

Equation 4

$$Rg < \frac{VCC\_AC - VCC\_SAT_{PNP} - V_{GK}}{I_{GT} + \frac{V_{GK}}{R_{GK}}}$$

Collector resistors RF2 and RF3 of the optocoupler are given by Equation 5, where RF1 is the PNP transistor resistor filter, VCC_AC is the power supply to provide the gate current to the AC switch, VCE_SAT_{Opto} is the transistor collector-emitter of the optocoupler, β is the PNP transistor gain and VBE_SAT_{PNP} is the PNP transistor base-emitter.

Equation 5

$$R_{F2} + R_{F3} = \frac{VCC_{AC} - VCE\_SAT_{OPTO} - VBE\_SAT_{PNP}}{\frac{VCC_{AC} - VCE\_SAT_{NPN} - V_{GK}}{\beta \times Rg} + \frac{VBE\_SAT_{PNP}}{R_{F1}}}$$

Given optocoupler CTR and resistors R_{F1} and R_{F2}, the LED resistor (R_L) of the optocoupler is defined by Equation 6, where VCC_AC is the power supply to provide the gate current to the AC switch, VCE_SAT_{Opto} is the transistor collector-emitter of the optocoupler, VBE_SAT_{PNP} is the PNP transistor base-emitter and VOH_Min_MCU is the output MCU voltage to drive the optocoupler.

Equation 6

$$R_L = \frac{VOH\_Min\_MCU - VF_{OPTO}}{\frac{1}{CTR} \times \frac{VCC\_AC - VCE\_SAT_{OPTO} - VBE\_SAT_{PNP}}{R_{F2} + R_{F3}}}$$

With the LTV-817 optocoupler and the 2N2907 PNP transistor, the resistors should be:

- R_{F1} = 1 kΩ
- R_{F2} = 390 Ω
- R_L = 270 kΩ
- C_{F2} = 10 nF
- C_{F1} = 10 nF

The actual values in the ICL board schematic are:

- $R_{F1} = R_{13} = R_{19}$ = 1 kΩ
- $R_{F2} = R_{F3} = R_{15} = R_{16} = R_{21} = R_{22}$ = 390 Ω
- $R_L = R_{14} = R_{20}$ = 270 kΩ
- $C_{F2} = C_{11} = C_{13}$ = 10 nF
- $C_{F1} = C_{10} = C_{12}$ = 10 nF

9 EN55014 test results

Figure 24: EMI noise test with 2000W load

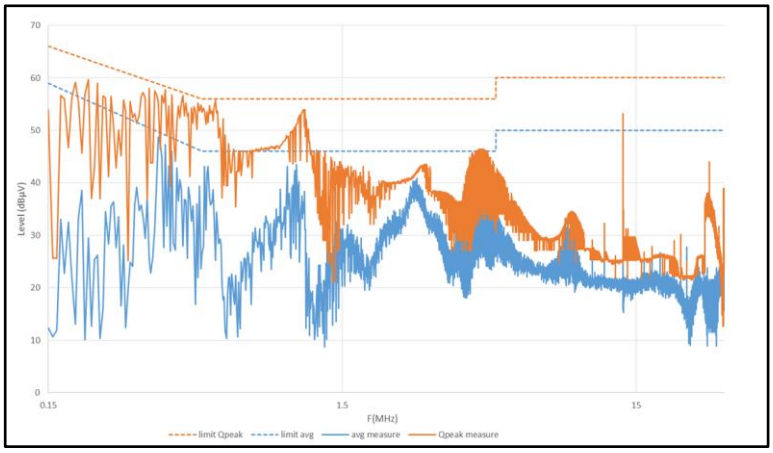
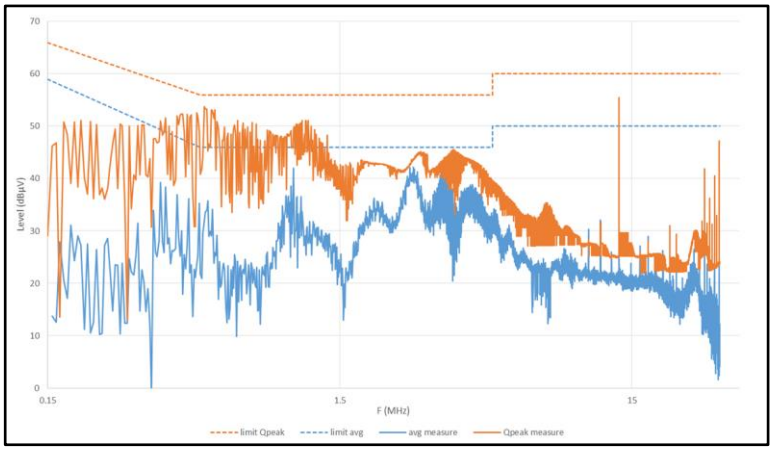
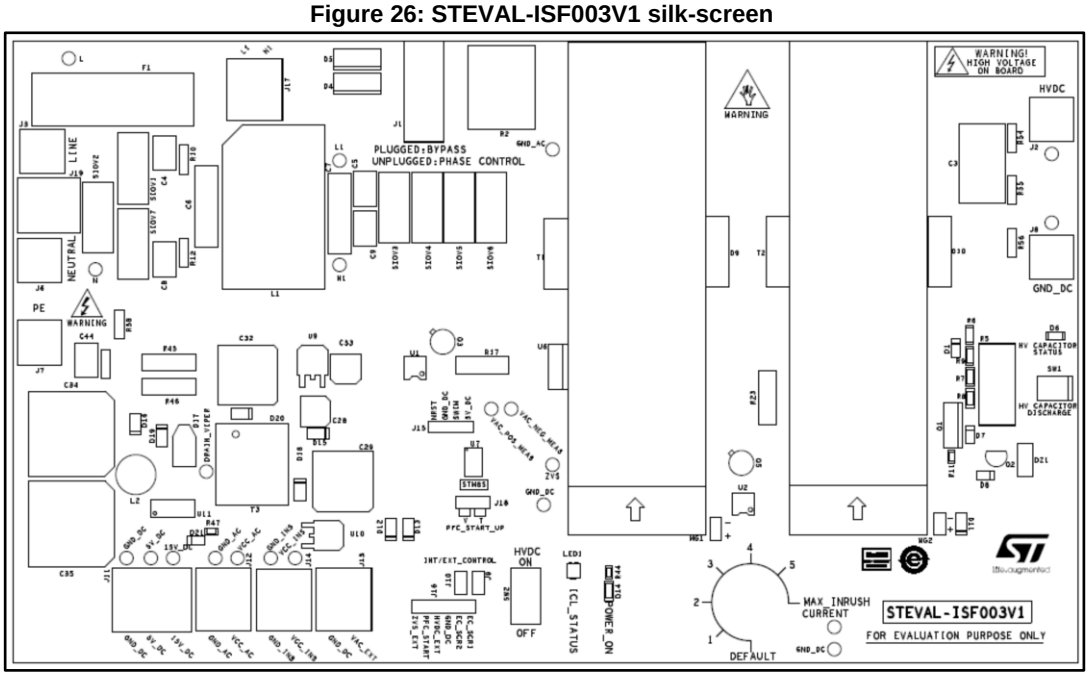


Figure 25: EMI noise test with no load



10 STEVAL-ISF003V1 silk-screen

Figure 26: STEVAL-ISF003V1 silk-screen



11 Bill of materials

Table 6: STEVAL-ISF003V1 bill of materials

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
1	4	C1, C2, C21, C38	100 nF, 50 V, ±10%, SMD 0805, X7R	Ceramic capacitor		
2	1	C3	47 nF, 600 V, ±20%	Radial metal film capacitor		
3	5	C4, C5, C8, C9, C44	2.2 nF, 440 V, ±20%	Disk ceramic Y2 capacitor		
4	2	C6, C7	68 nF, 300 V, ±20%	Disk ceramic X2 capacitor		
5	7	C10, C11, C12, C13, C20, C24, C25	10 nF, 50 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
6	1	C15	4.7 nF, 50 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
7	2	C16, C18	470 pF, 50 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
8	4	C14, C19, C26, C27	1 µF, 25 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
9	1	C22	1 µF, 25 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
10	1	C23	680 nF, 25 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
11	1	C28	220 µF, 16 V, ± 10%	SMD electrolytic capacitor		
12	1	C29	1.5 mF, 16 V, ± 10%	SMD electrolytic capacitor		
13	2	C30, C41	330 nF, 50 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
14	1	C32	220 µF, 63 V, ± 10%	SMD electrolytic capacitor		
15	3	C33, C39, C42	100 µF, 16 V, ± 10%	SMD electrolytic capacitor		
16	1	C34	10 µF, 450 V, ± 10%	SMD electrolytic capacitor		

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
17	1	C35	22 µF, 450 V, ± 10%	SMD electrolytic capacitor		
18	1	C36	2.2 µF, 63 V, ± 10%	SMD electrolytic capacitor		
19	1	C37	680 pF, 50 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
20	1	C40	1 nF, 50 V, ± 10%, SMD 0805, X7R	Ceramic capacitor		
21	1	DZ1	440 V, 600 W	TVS diode	ST	P6KE440A
22	1	D1	30 V, 50 0mW	Zener diode		BZX55C30
23	2	D4, D5	12 A, 1000 V	Automotive ultrafast recovery diode	ST	STTH1210-Y
24	2	D6, D14		Red LED	AVAGO TECHNOLOGIES	HLMP-Q156-H0031
25	1	D7	5.6 V, 500 mW	Zener diode		BZX55C5V6
26	1	D8	15 V, 500 mW	Zener diode		BZX55C15
27	2	D9, D10	60 A, 1200 V	Standard bridge rectifier diode	ST	STBR6012WY
28	4	D11, D12, D13, D16	1 A, 1000 V	Standard diode		1N4007
29	3	D15, D18, D20	1 A, 150 V	Power Schottky rectifier	ST	STPS1150
30	1	D17	1.5 kW, 300 V	TVS diode	ST	1.5KE300A
31	1	D19	1 A, 600 V	Ultrafast high voltage rectifier	ST	STTH1L06
32	1	D21	100 V, 0.15 A	Signal diode		1N4148
33	3	D22,D23,D24	30 V, 100 mA	Double series Schottky	ST	BAR43S
34	1	F1	32 A, 250 V	Fuseholder		
35	1	GT1	600 V , 5 kA	Gas tube discharge	EPCOS	GTD_EC600X
36	1	J1		Header		
37	5	J2, J3, J6, J7, J8		Wire-to-board through hole, pressfit connectors	WURTH ELEKTRONIK	7461383
38	2	J9, J10		Board-to-board connector		
39	1	J11		Wire-to-board connector	WAGO	236-403

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
40	5	J12, J13, J14, J17, J19		Wire-to-board connector	WAGO	236-402
41	1	J15		Board-to-board connector		
42	1	J16		Board-to-board connector		
43	1	LED1		Bicolor LED	VISHAY	VLMV3100-GS08
44	1	L1	0.9 mH, 32 A	Common mode choke	WURTH ELEKTRONIK	7448053201
45	1	L2	1 mH	Power inductor	WURTH ELEKTRONIK	744741102
46	2	MG1, MG2	1 K	Heatsink	FISHER ELEKTRONIK	LAM 3 K 100 12
47	1	Q1	800 V, 4 A	High voltage NPN		
48	1	Q2	800 V, 300 mA	N power MOSFET	ST	STQ1NK80ZR-AP
49	2	Q3, Q5	60 V, 600 mA	PNP bipolar		
50	1	Q4	30 V, 6.5 A	N MOSFET transistor	ST	STN4NF03L
51	1	R2	PTC_56R_440VAC	PTC thermistor	EPCOS	B59107J130A20
52	2	R3, R4	100 R, 0.125 W, SMD0805	Resistor		
53	1	R5	2.5 K, 5 W, SMD0805	Through hole resistor	VISHAY	CW0052K500JE73
54	4	R6, R7, R8, R9	250 K, 0.125 W, SMD0805	Resistor		
55	2	R10, R12	2.7 M, 0.33 W	Through-hole resistor		
56	1	R11	3.3 K, 0.125 W	Through-hole resistor		
57	3	R13, R19, R53	1 k, 0.125 W, SMD0805	Resistor		
58	2	R14, R20	270 R, 0.125 W, SMD0805	Resistor		
59	4	R15, R16, R21, R22	390 R, 0.125 W, SMD0805	Resistor		
60	2	R17, R23	30 R, 2 W	Through-hole resistor		
61	1	R18	10 R, 0.125 W, SMD0805	Resistor		
62	6	R24, R25, R31, R32, R37, R38	1 M, 0.25 W, SMD1206	Resistor		

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
63	2	R26, R27	300 R, 0.125 W, SMD1206	Resistor		
64	3	R28, R35, R40	21.5 K, 0.25 W, SMD1206	Resistor		
65	1	R39	39 K, 0.125 W, SMD0805	Resistor		
66	3	R41,R42,R52	10 K, 0.125 W, SMD0805	Resistor		
67	1	R43	75 R, 0.125 W, SMD0805	Resistor		
68	1	R44	1.5 K, 0.125 W, SMD0805	Resistor		
69	2	R45, R46	47 R, 1 W	Through-hole resistor	TE connectivity	EP1W47RJ
70	1	R47	36 K, 0.125 W, SMD0805	Resistor		
71	1	R48	10 K, 0.125 W, SMD0805	Resistor		
72	1	R49	20 K, 0.125 W, SMD0805	Resistor		
73	1	R50	22 K, 0.125 W, SMD0805	Resistor		
74	1	R51	150 R, 0.125 W, SMD0805	Resistor		
75	3	R54, R55, R56	470 K, 0.25 W	Through-hole resistor		
76	2	R57, R58	250 K, 0.25 W	Through-hole resistor		
77	1	R59	10 K, 0.05 W	Linear potentiometer	ALPS	RK09K1130AP5
78	2	SIOV1, SIOV7	250 V_{AC}	Varistor		S14K250
79	2	SIOV2, SIOV3	385 V_{AC}	Varistor		S14K385
80	1	SW1		DPDT ON-(ON)	RS	8UD8WR2C2M2RES
81	1	SW2	28 V, 5 A	SPDT ON-(ON)	RS	5MS1S402AM2QES
82	20	TP1 to TP20		Test point	VERO	20-136
83	2	T1, T2	1200 V, 50 A	Automotive SCR	ST	TN5050H-12WY
84	1	T3	12 W	Flyback transformer	MYRRA	74010
85	2	U1, U2	50 mA	Optocoupler	LITE ON	LTV-817M-A
86	1	U3	10 V	CMOS comparator	ST	TS861AIDT

Item	Q.ty	Ref.	Part/Value	Description	Manufacturer	Order code
87	1	U5	60 V, 0.15 mA	N MOSFET transistor		
88	1	U6		temp sensor TO-220	TI	LM35DT
89	1	U7	8 bits, 16 MHz, 8 kB, 1 kB	Microcontroller	ST	STM8S003F3P6
90	1	U8	12 V, 500 mA	Regulator	ST	L78M12CDT
91	2	U9, U10	5 V, 100 mA	Regulator	ST	LM2931ADT50R
92	1	U11		SMPS controller	ST	Viper26LD

12 Test points

Reference	Designation	Definition
TP1	L1	Line after EMI filter
TP2,TP21,TP33	VCC_AC	
TP3	HVDC	
TP4	L	Line before EMI filter
TP5	OUT_ICL	A2 output of T_ICL
TP6	OUT1	A2 output of T1
TP7	OUT2	A2 output of T2
TP8	OUT3	A2 output of T3
TP9	OUT4	A2 output of T4
TP10	OUT5	A2 output of T5
TP11	HVDC/2	
TP12	N	Neutral before EMI filter
TP13	N1	Neutral after EMI filter
TP14,TP24,TP29	GND_DC	
TP15	G1	Gate signal of T1
TP16	G2	Gate signal of T2
TP17	G3	Gate signal of T3
TP18	G4	Gate signal of T4
TP19	G5	Gate signal of T5
TP20	G_ICL	Gate signal of T_ICL
TP22	GND_AC	
TP23	15V_DC	
TP25	VCC_INS	
TP26	Drain_viper	
TP27	GND_INS	
TP28	5V_DC	
TP30	ZVS	
TP31	VL1_MEAS	MCU input for line measurement
TP32	VN1_MEAS	MCU input for neutral measurement
TP34	MAX INRUSH CURRENT ORDER	

13 Conclusion

This evaluation board provides an innovative front-end circuit providing inrush-current limitation and power loss reduction. The board is much more than the demonstration of the efficiency and the robustness of STMicroelectronics solution, this front-end circuit can be used as a starting element to build a whole system and accelerate the time-to-market of new application designs.

14 Revision history

Table 7: Document revision history

Date	Version	Changes
01-Jul-2016	1	Initial release.
18-Apr-2017	2	Minor text changes throughout document. Updated *Section 3: "Schematic diagrams"*.

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