ZL9101M

Digital DC/DC PMBus 12A Module

FN7669
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The ZL9101M is a 12A, variable output, step-down PMBus-compliant digital power supply. Included in the module is a high-performance digital PWM controller, power MOSFETs, an inductor, and all the passive components required for a highly integrated DC/DC power solution. This power module has built-in auto-compensation algorithms, which eliminate the need for manual compensation design work. The ZL9101M operates over a wide input voltage range and supports an output voltage range of 0.6V to 3.6V, which can be set by external resistors or through PMBus. This high-efficiency power module is capable of delivering 12A. Only bulk input and output capacitors are needed to finish the design. The output voltage can be precisely regulated to as low as 0.6V with ±1% output voltage regulation over line, load, and temperature variations.

The ZL9101M features auto compensation, internal soft-start, auto-recovery overcurrent protection, an enable option, and prebiased output start-up capabilities.

The ZL9101M is packaged in a thermally enhanced, compact (15mmx15mm) and low profile (3.5mm) overmolded QFN package module suitable for automated assembly by standard surface mount equipment. The ZL9101M is RoHS compliant.

Figure 1 represents a typical implementation of the ZL9101M. For PMBus operation, it is recommended to tie the Enable pin (EN) to SGND.

Features

- Complete digital switch mode power supply
- Fast transient response
- Auto compensating PID filter
- External synchronization
- Output voltage tracking
- Current sharing
- Programmable soft-start delay and ramp
- Overcurrent/undercurrent protection
- PMBus compliant

Applications

- Server, telecom, and datacom
- Industrial and medical equipment
- General purpose point-of-load

Related Literature

- For a full list of related documents, visit our website
  - ZL9101M product page

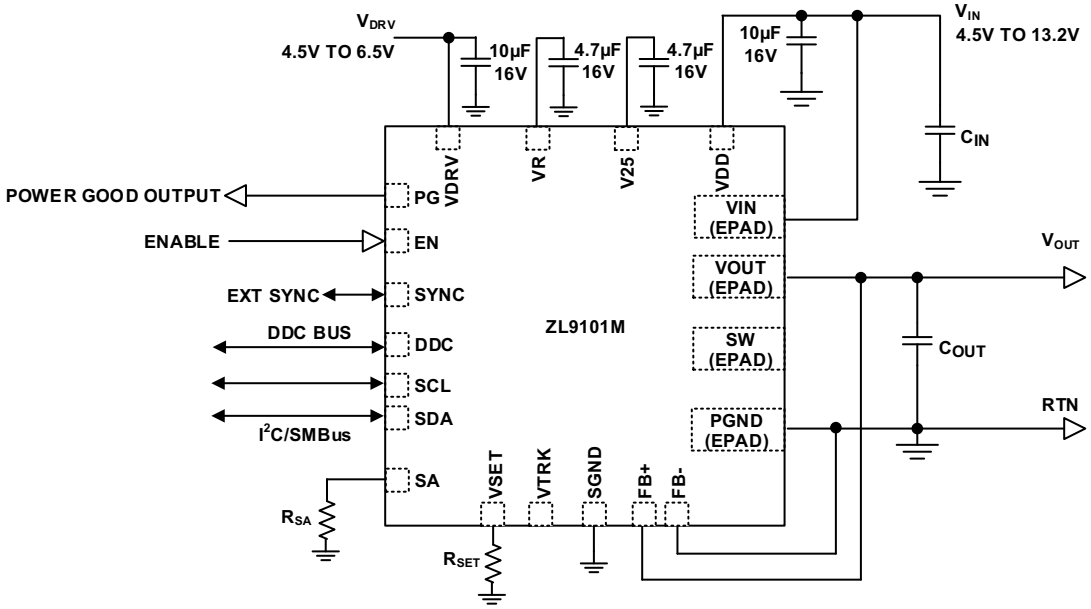

FIGURE 1. A COMPLETE DIGITAL SWITCH MODE POWER SUPPLY, ONLY BULK INPUT AND OUTPUT CAPACITORS ARE REQUIRED TO FINISH THE DESIGN

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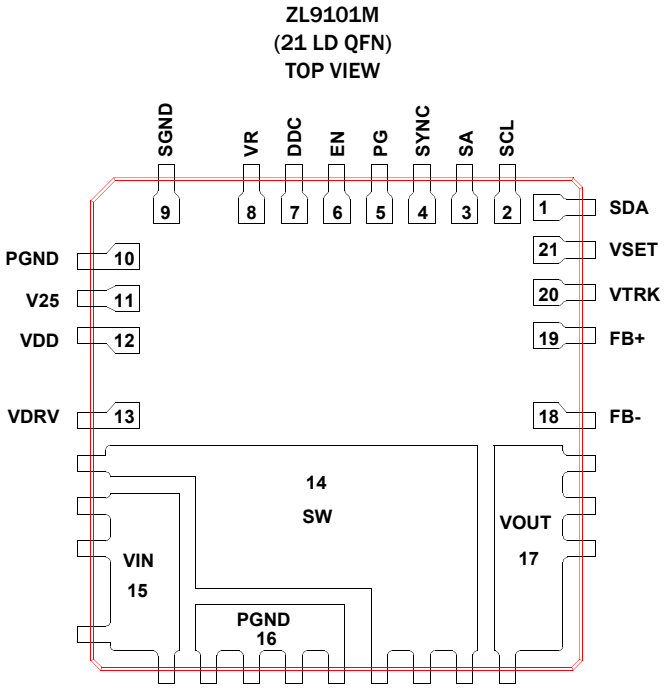
Pin Configuration



Pin Descriptions

PIN#	LABEL	TYPE	DESCRIPTION
1	SDA	I/O	Serial data. A pull-up resistor is required for this application.
2	SCL	I/O	Serial clock. A pull-up resistor is required for this application.
3	SA	I	Serial address select pin. Used to assign a unique SMBus address to each module.
4	SYNC	I/O	Clock synchronization. Used for synchronization to external frequency reference.
5	PG	O	Power-good output.
6	EN	I	Enable input (factory setting active high). Pull-up to enable PWM switching and pull-down to disable PWM switching.
7	DDC	I/O	Digital-DC bus (open drain). Interoperability between Intersil digital modules. A pull-up resistor is required for this application.
8	VR	PWR	Internal 5V reference used to power internal drivers. Connect a 4.7µF bypass capacitor to this pin.
9	SGND	PWR	Signal ground. Connect to low impedance ground plane.
10	PGND	PWR	Power ground. Connect to low impedance ground plane.
11	V25	PWR	Internal 2.5V reference used to power internal circuitry. Connect a 4.7µF bypass capacitor to this pin.
12	VDD	PWR	Input supply voltage for controller. Connect a 4.7µF bypass capacitor to this pin.
13	VDRV	PWR	Power supply for internal FET drivers. Connect a 10µF bypass capacitor to this pin.
14 (epad)	SW	PWR	Drive train switch node.
15 (epad)	VIN	PWR	Power supply input FET voltage.
16 (epad)	PGND	PWR	Power ground. Connect to low impedance ground plane.
17 (epad)	VOUT	PWR	Power supply output voltage. Output voltage from PWM.
18	FB-	I	Output voltage feedback. Connect to load return of ground regulation point.
19	FB+	I	Output voltage feedback. Connect to output regulation point.
20	VTRK	I	Tracking sense input. Used to track an external voltage source.
21	VSET	I	Output voltage selection pin. Used to set V_{OUT} set point and V_{OUT} maximum.

Internal Block Diagram

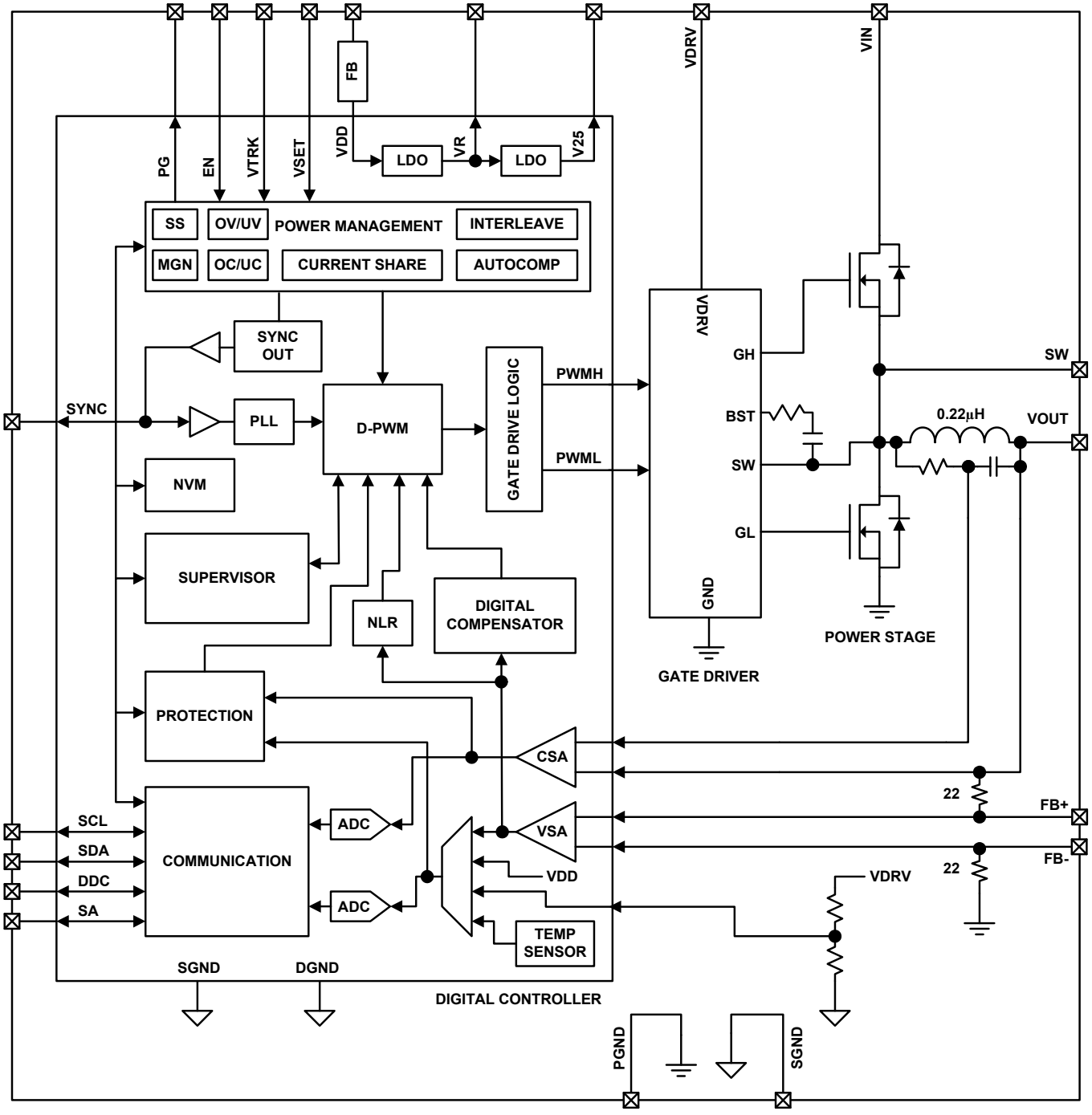
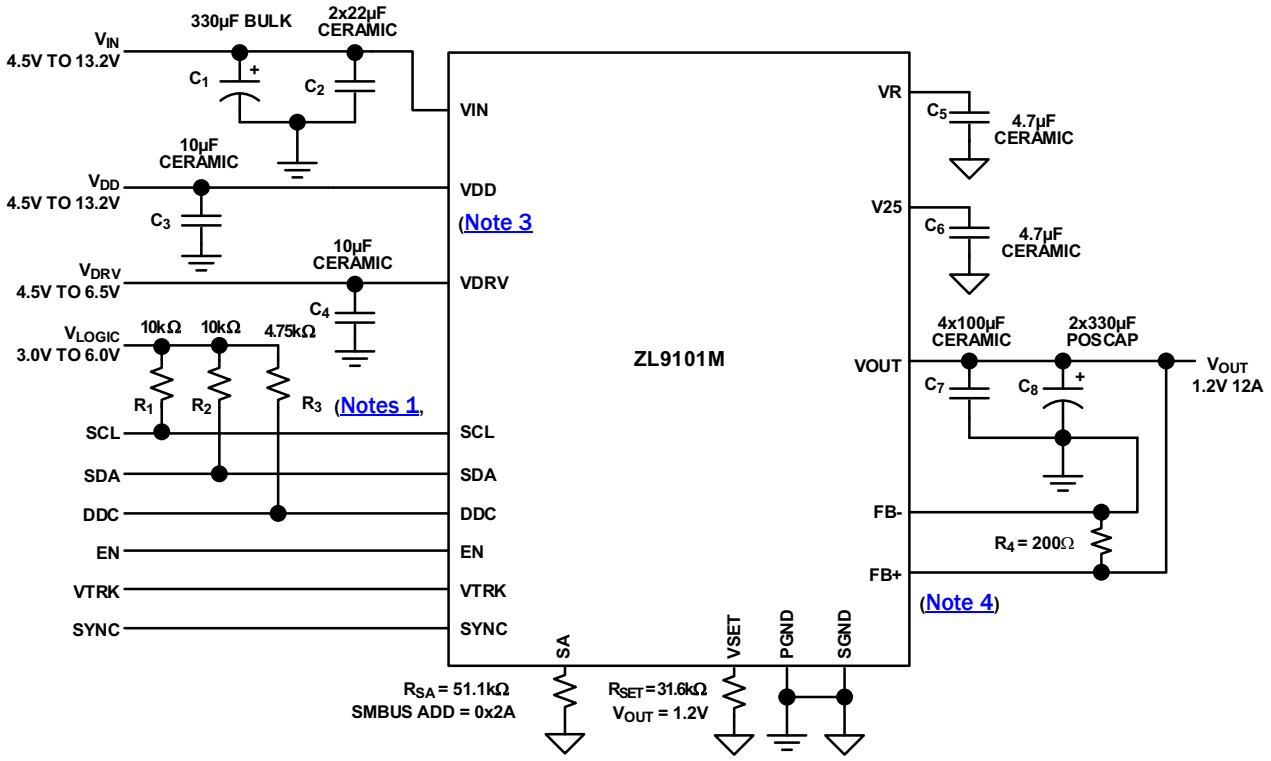


FIGURE 2. ZL9101M INTERNAL BLOCK DIAGRAM

Typical Application - Single Module



NOTES:

1. R_1 and R_2 are not required if the PMBus host already has I^2C pull-up resistors.
2. Only one R_3 per DDC bus is required when DDC bus is shared with other modules.
3. The VR, V25, VDRV, and VDD capacitors should be placed no farther than 0.5cm from the pin.
4. R_4 is optional but recommended to sink possible ~100µA backflow current from the FB+ pin. Backflow current is present only when the module is in a disabled state with power still available at the V_{DD} pin.

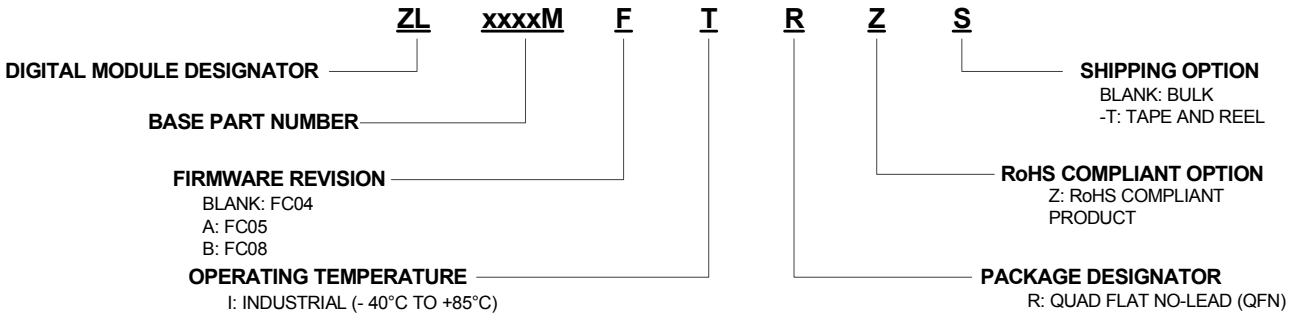
FIGURE 3. SINGLE MODULE

Ordering Information

PART NUMBER (Notes 5, 6, 7)	PART MARKING	FIRMWARE REVISION (Note 8)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ZL9101MIRZ	ZL9101M	FC04	-40 to +85	21 Ld 15x15 QFN	L21.15x15
ZL9101MAIRZ	ZL9101M	FC05	-40 to +85	21 Ld 15x15 QFN	L21.15x15
ZL9101MBIRZ	ZL9101M B	FC08	-40 to +85	21 Ld 15x15 QFN	L21.15x15
ZL9101EVAL1Z	Evaluation Board				

NOTES:

5. Add “-T” suffix for 500 unit tape and reel option. Refer to tech brief TB347 for details on reel specifications.
6. These Intersil plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3) termination finish which is compatible with both SnPb and Pb-free soldering operations. Intersil RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
7. For Moisture Sensitivity Level (MSL), see device information page for ZL9101M. For more information on MSL please see tech brief TB363.
8. See “Firmware Revision History” on page 59; only the latest firmware revision is recommended for new designs.



Absolute Maximum Ratings (Note 9)

DC Supply Voltage for VDD Pin . . . . . -0.3V to 15.7V
Input Voltage for VIN Pin . . . . . -0.3V to 15.7V
MOSFET Drive Reference for VR Pin . . . . . -0.3V to 6.5V
2.5V Logic Reference for V25 Pin. . . . . -0.3V to 3V
MOSFET Driver Power for VDRV Pin . . . . . -0.3V to 7.5V
Logic I/O Voltage for DDC, EN,
FB+, FB-, PG, SA, SCL, SDA, SYNC, VSET Pins . . . . . -0.3V to 6V
ESD Rating
  Human Body Model (Tested per JESD22-A114F) 2kV
  Machine Model (Tested per JESD22-A115C) 200V
  Charged Device Model (Tested per JESD22-C110D) 1kV
Latch-Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 12, 13)	11.5	2.2

Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see Figure 22 on page 19

Recommended Operating Conditions

Input Supply Voltage Range, V_{IN} . . . . . 4.5V to 13.2V
Input Supply for Controller, V_{DD} (Note 10) . . . . . 4.5V to 13.2V
Driver Supply Voltage, V_{DRV} . . . . . 4.5V to 6.5V
Output Voltage Range, V_{OUT} (Note 11) . . . . . 0.54V to 3.6V
Output Current Range, $I_{OUT(DC)}$ . . . . . 0A to 12A
Operating Junction Temperature Range, T_J . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

9. Voltage measured with respect to SGND
10. V_{IN} supplies the power FETs. V_{DD} supplies the controller. V_{IN} can be tied to V_{DD}. For $V_{DD} \le 5.5V$, V_{DD} should be tied to VR.
11. Includes ±10% margin limits.
12. θ_{JA} is simulated in free air with device mounted on a four-layer FR-4 test board (76.2 x 114.3 x 1.6mm) with 80%-coverage, 2-ounce Cu on top and bottom layers, plus two, buried, one-ounce Cu layers with coverage across the entire test board area. Multiple vias were used, with via diameter = 0.3mm on 1.2mm pitch.
13. For θ_{JC}, the "case" temperature is measured at the center of the package underside.

Electrical Specifications

V_{DD} = 12 V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP (Note 15)	MAX (Note 14)	UNIT
INPUT AND SUPPLY CHARACTERISTICS					
Input Bias Supply Current, I_{DD}	f_{SW} = 571kHz, No load	–	20	**40**	mA
Input Bias Shutdown Current, I_{DDS}	EN = 0 V; no I^2C/SMBus activity	–	15.5	**20.0**	mA
Input Supply Current, I_{VIN}	V_{IN} = 13.2V, I_{OUT} = 12A, V_{OUT} = 1.2V	–	1.32	–	A
Driver Supply Current, I_{VDRV}	V_{DRV} = 6V, V_{OUT} = 1.0V, f_{SW} = 571kHz, I_{OUT} = 12A	–	30	–	mA
	Non switching	–	190	**250**	µA
VR Reference Output Voltage (Note 16)	V_{DD} > 6V, I_{VR} < 20mA	**4.5**	5.2	**5.7**	V
V25 Reference Output Voltage (Note 16)	V_R > 3V, I_{V25} < 20mA	**2.25**	2.50	**2.75**	V
OUTPUT CHARACTERISTICS					
Output Load Current	V_{IN} = 12V, V_{OUT} = 1.2V	–	–	**12**	A
Output Voltage Accuracy (Notes 16, 17)	Include line, load, temperature	**–1**	–	**+1**	%
Peak-to-Peak Output Ripple Voltage, ΔV_{OUT} (Note 17)	I_{OUT} = 12A, V_{OUT} = 1.2V, C_{OUT} = 3000µF	–	6	–	mV
Soft-Start Delay Duration Range (Notes 16, 18)	Set using I^2C/SMBus	**2**	–	**200**	ms
Soft-Start Delay Duration Accuracy (Note 16)	Turn-on delay (precise mode) (Notes 18, 19)	–	±0.25	–	ms
	Turn-on delay (normal mode) (Note 20)	–	-0.25/+4	–	ms
	Turn-off delay (Note 20)	–	-0.25/+4	–	ms
Soft-Start Ramp Duration Range (Note 16)	Set using I^2C	**0**	–	**200**	ms
Soft-Start Ramp Duration Accuracy (Note 16)		–	100	–	µs
DYNAMIC CHARACTERISTICS					
Voltage Change for Positive Load Step	ΔI_{OUT} = 6A, slew rate = 2.5A/µs, V_{OUT} = 1.2V, C_{OUT} = 3000µF	–	3	–	%
Voltage Change for Negative Load Step	ΔI_{OUT} = 6A, slew rate = 2.5A/µs, V_{OUT} = 1.2V, C_{OUT} = 3000µF	–	3	–	%

Electrical Specifications V_{DD} = 12 V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP (Note 15)	MAX (Note 14)	UNIT
OSCILLATOR AND SWITCHING CHARACTERISTICS (Note 16)					
Switching Frequency Range		**400**	571	**1000**	kHz
Maximum PWM Duty Cycle	Factory setting	**95**	–	–	%
Minimum SYNC Pulse Width		**150**	–	–	ns
Input Clock Frequency Drift Tolerance	External clock source	**-13**	–	**13**	%
LOGIC INPUT/OUTPUT CHARACTERISTICS (Note 16)					
Logic Input Bias Current	EN, PG, SCL, SDA pins	**-10**	–	**10**	µA
Logic Input Low, V_{IL}		–	–	**0.8**	V
Logic Input High, V_{IH}		**2.0**	–	–	V
Logic Output Low, V_{OL}	I_{OL} ≤ 4mA (Note 22)	–	–	**0.4**	V
Logic Output High, V_{OH}	I_{OH} ≥ -2mA (Note 22)	**2.25**	–	–	V
FAULT PROTECTION CHARACTERISTICS (Note 16)					
UVLO Threshold Range	Configurable through I^2C/SMBus	**2.85**	–	**16.00**	V
UVLO Set-Point Accuracy		**-150**	–	**150**	mV
UVLO Hysteresis	Factory setting	–	3	–	%
	Configurable through I^2C/SMBus	**0**	–	**100**	%
UVLO Delay		–	–	**2.5**	µs
Power-Good V_{OUT} Threshold	Factory setting	–	90	–	% V_{OUT}
Power-Good V_{OUT} Hysteresis	Factory setting	–	5	–	%
Power-Good Delay (Note 21)	Configurable through I^2C/SMBus	**0**	–	**200**	ms
VSEN Undervoltage Threshold	Factory setting	–	85	–	% V_{OUT}
	Configurable through I^2C/SMBus	**0**	–	**110**	% V_{OUT}
VSEN Overvoltage Threshold	Factory setting	–	115	–	% V_{OUT}
	Configurable through I^2C/SMBus	**0**	–	**115**	% V_{OUT}
VSEN Undervoltage Hysteresis		–	5	–	% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory setting	–	16	–	µs
	Configurable through I^2C/SMBus	**5**	–	**60**	µs
Thermal Protection Threshold (Controller Junction Temperature)	Factory setting	–	125	–	°C
	Configurable through I^2C/SMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		–	15	–	°C

NOTES:

14. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
15. Parameters with TYP limits are not production tested unless otherwise specified.
16. Parameters are 100% tested for internal controller prior to module assembly.
17. V_{OUT} measured at the termination of the FB+ and FB- sense points.
18. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approximately 2ms, where in normal mode it may vary up to 4ms.
19. Precise ramp timing mode is only valid when using the EN pin to enable the device rather than PMBus enable.
20. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the deassertion of the enable signal.
21. Factory setting for power-good delay is set to the same value as the soft-start ramp time.
22. Nominal capacitance of logic pins is 5pF.

Typical Performance Curves

Operating conditions: T_A = +25°C, no air flow, f_{SW} = 571kHz. V_{DRV} = 5V, C_{OUT} = 3000µF. Typical values are used unless otherwise noted.

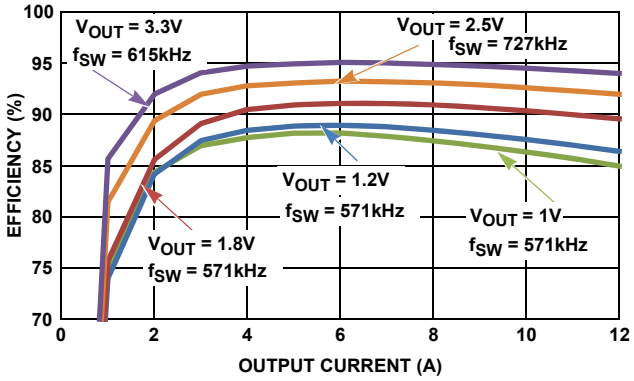


FIGURE 4. EFFICIENCY, V_{IN} = 5V, FOR VARIOUS OUTPUT VOLTAGES

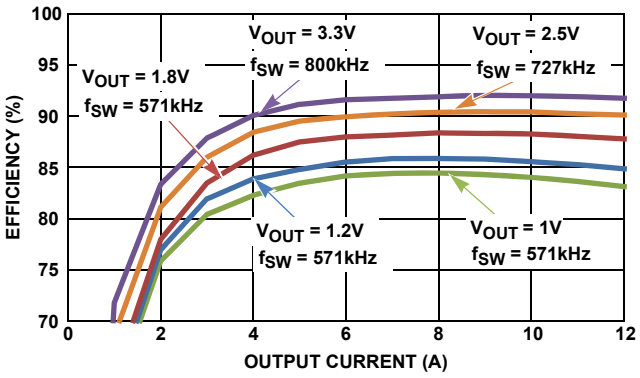


FIGURE 5. EFFICIENCY, V_{IN} = 9V, FOR VARIOUS OUTPUT VOLTAGES

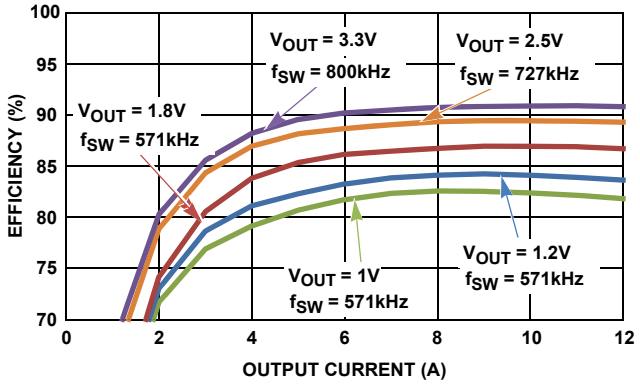


FIGURE 6. EFFICIENCY, V_{IN} = 12V, FOR VARIOUS OUTPUT VOLTAGES

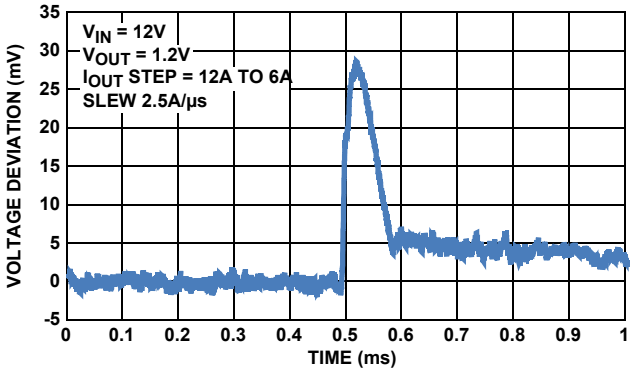


FIGURE 7. DYNAMIC RESPONSE, UNLOAD

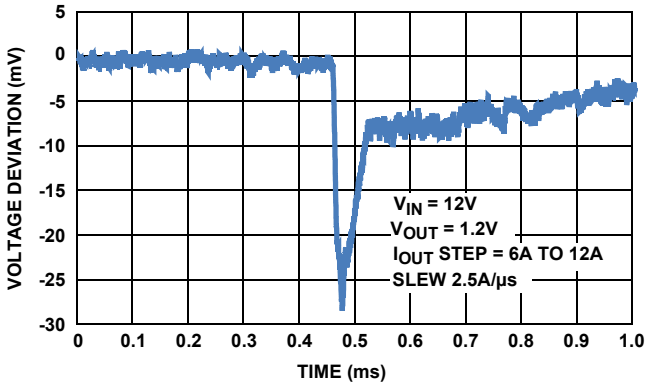


FIGURE 8. DYNAMIC RESPONSE, LOAD

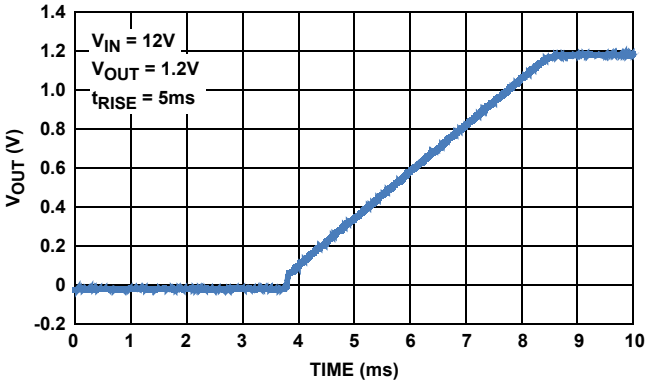


FIGURE 9. SOFT-START RAMP-UP

Typical Performance Curves

Operating conditions: T_A = +25°C, no air flow, f_{SW} = 571kHz. V_{DRV} = 5V, C_{OUT} = 3000µF.
Typical values are used unless otherwise noted. **(Continued)**

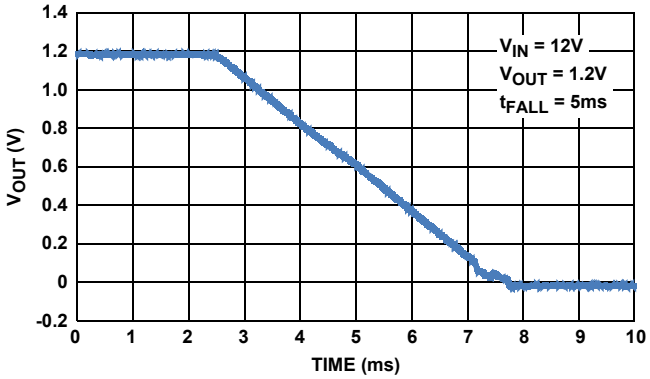


FIGURE 10. RAMP-DOWN

Derating Curves

Operating conditions: T_A = +25°C, no air flow, f_{SW} = 571kHz, V_{DRV} = 5V, C_{OUT} = 3000µF.
Typical values are used unless otherwise noted.

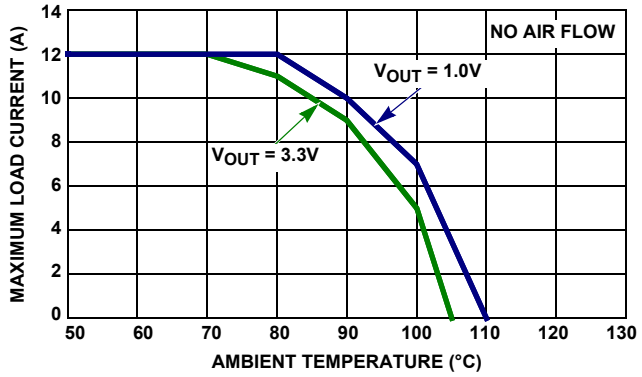


FIGURE 11. DERATING CURVE, $5V_{IN}$, FOR VARIOUS OUTPUT VOLTAGES LISTED

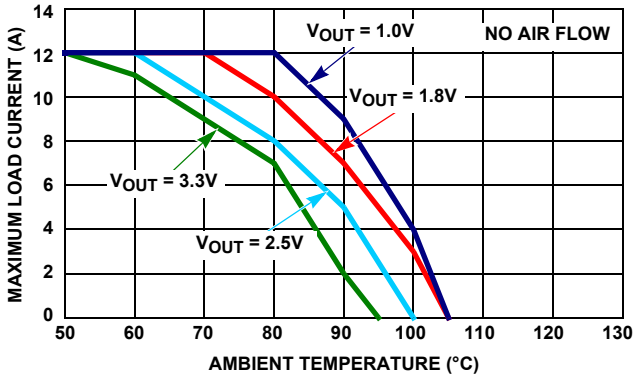


FIGURE 12. DERATING CURVE, $12V_{IN}$, FOR VARIOUS OUTPUT VOLTAGES LISTED

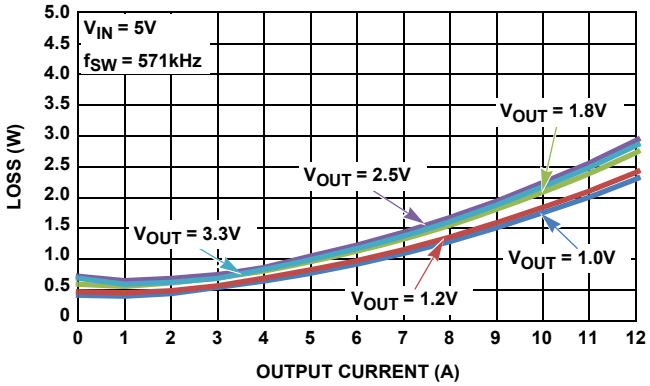


FIGURE 13. POWER LOSS CURVE, $5V_{IN}$, FOR VARIOUS OUTPUT VOLTAGES LISTED

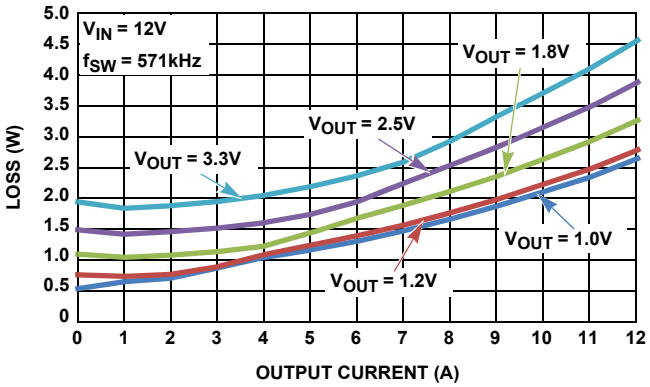


FIGURE 14. POWER LOSS CURVE, $12V_{IN}$, FOR VARIOUS OUTPUT VOLTAGES LISTED

Functional Description

I²C/SMBus Communications

The ZL9101M provides an I²C/SMBus digital interface that enables the user to configure all aspects of the module operation as well as monitor the input and output parameters. The ZL9101M can be used with any I²C host device. In addition, the module is compatible with SMBus version 2.0. Pull-up resistors are required on the I²C/SMBus as specified in the SMBus 2.0 specification. The ZL9101M accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin be tied to SGND.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set through the I²C/SMBus. The device address is set using the SA pin. VOUT_MAX is determined as 10% greater than the voltage set by the VSET pin. Standard 1% resistor values are used between the respective pin and SGND.

Output Voltage Selection

The output voltage can be set to a voltage between 0.6V and 3.6V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification.

The VSET pin is used to set the output voltage to levels as shown in Table 1. The R_{SET} resistor is placed between the VSET pin and SGND.

TABLE 1. OUTPUT VOLTAGE RESISTOR SETTINGS

V_{OUT} (V)	R_{SET} (kΩ)
0.60	10
0.65	11
0.70	12.1
0.75	13.3
0.80	14.7
0.85	16.2
0.90	17.8
0.95	19.6
1.00	21.5
1.05	23.7
1.10	26.1
1.15	28.7
1.20	31.6
1.25	34.8
1.30	38.3
1.40	42.2
1.50	46.4
1.60	51.1
1.70	56.2

TABLE 1. OUTPUT VOLTAGE RESISTOR SETTINGS (Continued)

V_{OUT} (V)	R_{SET} (kΩ)
1.80	61.9
1.90	68.1
2.00	75
2.10	82.5
2.20	90.9
2.30	100
2.50	110
2.80	121
3.00	133
3.30	147

The output voltage can also be set to any value between 0.6V and 3.6V using a PMBus command over the I²C/SMBus interface. The R_{SET} resistor program places an upper limit in output voltage setting through PMBUS programming to 10% above the value set by the resistor.

Soft-Start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL9101M gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp times are set to custom values through the I²C/SMBus interface. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

Power-Good

The ZL9101M provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the polarity of the pin can be changed through the I²C/SMBus interface.

A PG delay period is defined as the time from when all conditions within the ZL9101M for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic.

Switching Frequency and PLL

The ZL9101M incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source.

If a clock signal is present, the ZL9101M's oscillator will synchronize the rising edge of the external clock. If no incoming clock signal is present, the ZL9101M will configure the switching frequency according to the state of the SYNC pin as listed in Table 2. The internal switching frequency of the ZL9101M is 571kHz. ZL9101M will only read the SYNC pin connection during the start-up sequence. Changes to the SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

TABLE 2. SWITCHING FREQUENCY SELECTION

SYNC PIN	FREQUENCY
LOW	400kHz
OPEN	571kHz
HIGH	1MHz
Resistor	See Table 3

If the user wants to configure other frequencies not listed in Tables 2 or 3, the switching frequency can also be set to any value between 400kHz and 1MHz using the I^2C/SMBus interface.

TABLE 3. R_{SYNC} RESISTOR VALUES

R_{SYNC} (kΩ)	FREQUENCY (kHz)
19.6, or connect to SGND	400
21.5	421
23.7	471
26.1	533
28.7, or Open	571
31.6	615
34.8	727
37.3	800
46.4	889
51.1, or connect to V25 or VR	1000

If a value other than f_{SW} = 8MHz/N is entered using a PMBus command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 10).

When multiple Intersil digital devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. One of the devices must be configured as a Sync source and the remaining devices must be configured as a Sync input. The I^2C/SMBus must be used to configure the Sync pin.

NOTE: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected values in Tables 2 and 3. The difference is due to hardware quantization.

Loop Compensation

The ZL9101M operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. The module is internally compensated through the I^2C/SMBus interface.

The ZL9101M has an auto compensation feature that measures the characteristics of the power train and calculates the proper tap coefficients. By default, auto compensation is configured to execute one time after ramp with 50% auto compensation gain with power-good asserted immediately after the first auto compensation cycle finishes.

Adaptive Diode Emulation

Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

NOTE: The overall bandwidth of the device may be reduced when in diode emulation mode. Disabling the diode emulation before applying significant load steps is recommended.

Input Undervoltage Lockout

The input Undervoltage Lockout (UVLO) prevents the ZL9101M from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways, as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device remains in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault is cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the module. The controller continuously checks for the presence of the fault condition. If the fault condition is no longer present, the ZL9101M is re-enabled.

Output Overvoltage Protection

The ZL9101M offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the FB+ pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the FB+ voltage exceeds this threshold, the PG pin deasserts and the controller can then respond in a number of ways, as follows:

1. Initiate an immediate shutdown until the fault is cleared. The user can select a specific number of retry attempts.

2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The controller continuously checks for the presence of the fault condition and when the fault condition no longer exists, the device is re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ZL9101M provides prebias protection by sampling the output voltage prior to initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage, however, the total time elapsed from when the delay period expires and when the output reaches its target value will match the preconfigured ramp time (see Figure 15).

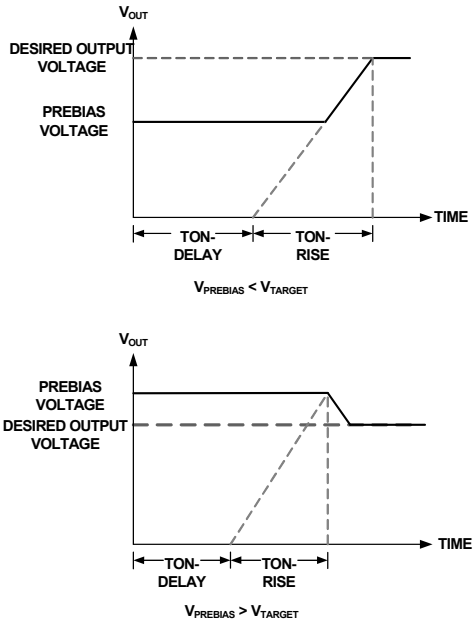


FIGURE 15. OUTPUT RESPONSES TO PREBIAS VOLTAGES

If a prebias voltage higher than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

After the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage higher than the overvoltage limit exists, the device does not initiate a turn-on sequence and declares an overvoltage fault condition to exist. In this case, the device responds based on the output overvoltage fault response method that has been selected. See "Output Overvoltage Protection" on page 12 for response options due to an overvoltage condition.

Note that prebias protection is not offered for current sharing groups, which also have tracking enabled. VDD must be tied to VIN for proper prebias start-up in single module operation.

Output Overcurrent Protection

The ZL9101M can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the controller. The controller continuously checks for the presence of the fault condition, and if the fault condition no longer exists, the device is re-enabled.

Thermal Overload Protection

The ZL9101M includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but the user can set the limit to a different value if desired. Note that setting a higher thermal limit through the I^2C/SMBus interface may result in permanent damage to the controller. Once the module has been disabled due to an internal temperature fault, the user can select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the module to restart, the controller waits the preset delay period (if configured to do so) and then checks the

module temperature. If the temperature has dropped below a threshold that is approximately +15°C lower than the selected temperature fault limit, the controller attempts to restart. If the temperature still exceeds the fault limit, the controller waits the preset delay period and retries again.

The default response from a temperature fault is an immediate shutdown of the module. The controller continuously checks for the fault condition and once the fault has cleared, the ZL9101M is re-enabled.

I²C/SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 4 lists the available module addresses.

TABLE 4. SMBus ADDRESS RESISTOR SELECTION

R_{SA} (kΩ)	SMBus ADDRESS
10	0x19
11	0x1A
12.1	0x1B
13.3	0x1C
14.7	0x1D
16.2	0x1E
17.8	0x1F
19.6	0x20
21.5	0x21
23.7	0x22
26.1, or connect to SGND	0x23
28.7, or Open	0x24
31.6, or connect to V25 or VR	0x25
34.8	0x26
38.3	0x27
42.2	0x28
46.4	0x29
51.1	0x2A
56.2	0x2B
61.9	0x2C
68.1	0x2D
75	0x2E
82.5	0x2F
90.9	0x30
100	0x31

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil Digital modules and devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to ensure the rise time as shown in Equation 1:

$$\text{Rise Time} = R_{PU} * C_{LOAD} \approx 1\mu s \quad \text{(EQ. 1)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor can be tied to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As a rule of thumb, each device connected to the DDC bus presents approximately 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approximately 2pF. The ideal design uses a central pull-up resistor that is well matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that ensures a logic 0 (typically 0.8V at the device monitoring point), given the pull-up voltage and the pull-down current capability of the ZL9101M (nominally 4mA).

Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time, can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset of each device can also be set to any value between 0° and 360° in 22.5° increments through the I²C/SMBus interface.

Output Voltage Tracking

High performance systems place stringent demands on the order in which the power supply voltages turn on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications. Voltage tracking protects these sensitive ICs by limiting the differential voltage among multiple power supplies during the power-up and power-down sequence.

The ZL9101M integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no additional components required. The VTRK pin is an analog input that, when tracking mode is enabled configures the voltage applied to the VTRK pin to act as a reference for the member device's output regulation.

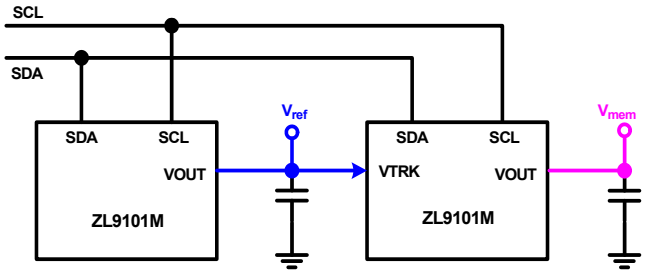


FIGURE 16. PMBUS TRACKING CONFIGURATION

Voltage tracking can be configured by PMBus only. An example is shown in Figure 16.

The ZL9101M offers two modes of tracking: coincident and ratiometric. Figures 17 and 18 illustrate the output voltage waveform for the two tracking modes.

Coincident: This mode configures the ZL9101M to ramp its output voltage at the same rate as the voltage applied to the VTRK pin. Two options are available for this mode:

1. Track at 100% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches its target voltage, Figure 17 (A).
2. Track at 100% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin, Figure 17 (B).

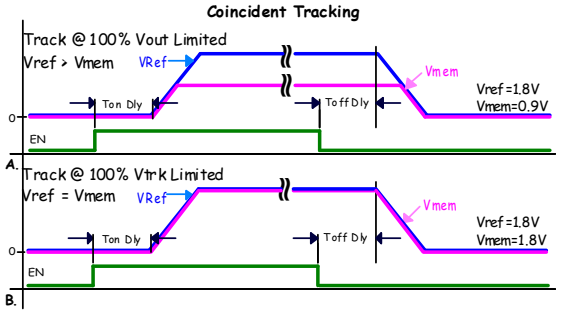


FIGURE 17. COINCIDENT TRACKING

Ratiometric: This mode configures the ZL9101M to ramp its output voltage as a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor or PMBus command can be used to configure a different tracking ratio.

1. Track at 50% V_{OUT} limited. Member rail tracks the reference rail and stops when the member reaches 50% of the target voltage, Figure 18(A).
2. Track at 50% VTRK limited. Member rail tracks the reference at the instantaneous voltage value applied to the VTRK pin until the member rail reaches 50% of the reference rail voltage, or if the member is configured to less than 50% of the reference the member will achieve its configured target, Figure 18(B).

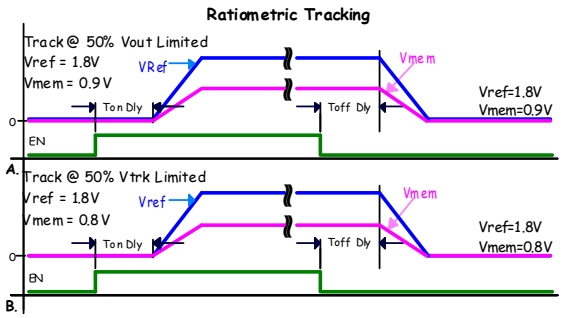


FIGURE 18. RATIOMETRIC TRACKING

Output Sequencing

A group of Digital-DC modules or devices can be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, (FPGAs and ASICs that require one supply to reach its operating voltage); before another supply reaching its operating voltage to avoid latch-up. Multidevice sequencing can be achieved by configuring each device through the I^2C/SMBus interface.

Multiple device sequencing is configured by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that follows in the sequencing chain.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turn-off of the group.

Fault Spreading

Digital-DC modules and devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a nondestructive fault occurs and the device is configured to shut down on a fault, the device shuts down and broadcasts the fault event over the DDC bus. The other devices on the DDC bus shut down simultaneously if configured to do so, and attempt to restart in their prescribed order.

Active Current Sharing

Multiple ZL9101M modules can be used in parallel to increase the output current capability of a single power rail. By connecting the DDC pins of each module together and configuring the modules as a current sharing rail, the units share the current equally within a few percent. Figure 19 illustrates a typical connection for two modules.

The ZL9101M uses a low-bandwidth, first-order digital current sharing technique to balance the unequal module output loading by aligning the load lines of member modules to a reference module.

Droop resistance is used to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PCB layout.

Upon system start-up, the module with the lowest member position as selected in ISHARE_CONFIG is defined as the reference module. The remaining modules are members. The reference module broadcasts its current over the DDC bus. The members use the reference current information to trim their voltages (V_{MEMBER}) to balance the current loading of each module in the system

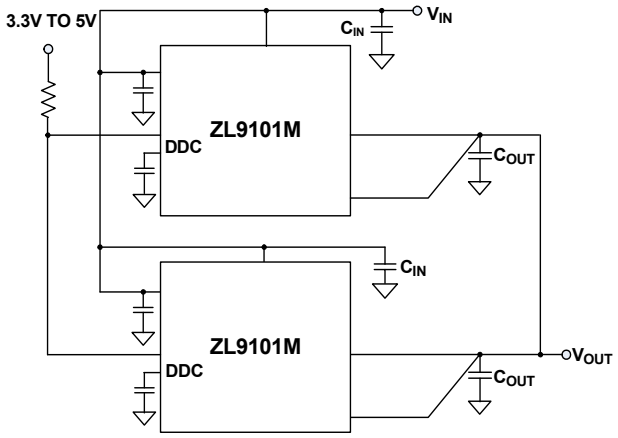


FIGURE 19. CURRENT SHARING GROUP

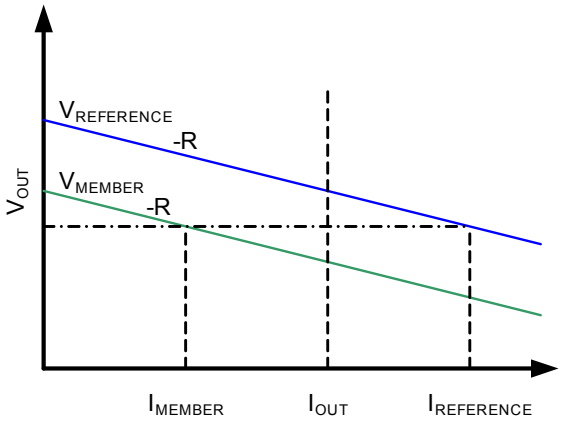


FIGURE 20. ACTIVE CURRENT SHARING

Figure 20 shows that, for load lines with identical slopes, the member voltage is increased towards the reference voltage which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by Equation 2:

$$V_{MEMBER} = V_{OUT} + R \times (I_{REFERENCE} - I_{MEMBER}) \quad \text{(EQ. 2)}$$

where R is the value of the droop resistance.

The ISHARE_CONFIG command is used to configure the module for active current sharing. The default setting is a stand-alone noncurrent sharing module. A current sharing rail can be part of a system sequencing group.

For fault configuration, the current share rail is configured in a quasi-redundant mode. In this mode, when a member module fails, the remaining members continue to operate and attempt to maintain regulation. Of the remaining modules, the module with the lowest member position becomes the reference. If fault spreading is enabled, the current share rail failure is not broadcast until the entire current share rail fails.

The phase offset of (multiphase) current sharing modules is automatically set to a value between 0° and 337.5° in 22.5° increments as in Equation 3:

$$\text{Phase Offset} = \text{SMBus Address}[4:0] - \text{Current Share Position} * 22.5° \quad \text{(EQ. 3)}$$

Please refer to application note AN2034 for additional details on current sharing.

Phase Adding/Dropping

The ZL9101M allows multiple power converters to be connected in parallel to supply higher load currents than can be addressed using a single-phase design. In doing so, the power converter is optimized at a load current range that requires all phases to be operational. During periods of light loading, it may be beneficial to disable one or more phases to eliminate the current drain and switching losses associated with those phases, resulting in higher efficiency.

The ZL9101M offers the ability to add and drop phases using a PMBus command in response to an observed load current change. All phases in a current share rail are considered active prior to the current sharing rail ramp to power-good.

Any member of the current sharing rail can be dropped. If the reference module is dropped, the remaining active module with the lowest member position becomes the new reference.

Additionally, any change to the number of members of a current sharing rail will precipitate autonomous phase distribution within the rail where all active phases realign their phase position based on their order within the number of active members.

If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail attempt to restart simultaneously after the fault has cleared.

Monitoring Through I^2C/SMBus

A system controller can monitor a wide variety of different ZL9101M system parameters through the I^2C/SMBus interface.

The module can be monitored for any number of power conversion parameters including but not limited to the following:

- Input voltage/output voltage
- Output current
- Internal temperature
- Switching frequency
- Duty cycle

SnapShot Parameter Capture

The ZL9101M offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The SnapShot functionality is enabled by setting bit 1 of MISC_CONFIG command to 1. The SnapShot feature enables the user to read parameters through a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 32 bytes occupies the SMBus for a period of time.

The SNAPSHOT_CONTROL command enables the user to store the SnapShot parameters to flash memory in response to a pending fault, as well as to read the stored data from flash memory after a fault has occurred. In order to read the stored data from flash memory, two conditions must apply:

1. The module should be disabled.
2. SnapShot mode should be disabled by changing bit 1 of MISC_CONFIG to 0. This is to prevent firmware from updating RAM values after the fault with current values.

Table 5 describes the usage of SNAPSHOT_CONTROL command. Automatic writes to flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to flash memory is not allowed if the device is configured to retry following the specific fault conditions).

TABLE 5. SNAPSHOT_CONTROL COMMAND

DATA VALUE	DESCRIPTION
1	Copies current SNAPSHOT values from flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to flash memory. Only available when device is disabled.

It should be noted that the device's VDD voltage must be maintained during the time when the device is writing the data to flash memory; a process that requires up to 1400µs. Undesirable results may be observed if the device's VDD supply drops below 3.0V during the process.

The following is a recommended procedure for using the SnapShot parameter capture after a fault:

1. Configure the module using config file (optional).
2. Enable the SnapShot mode by setting bit 1 of MISC_CONFIG command to 1. This can be done before or after the module is enabled. Note: do not store MISC_CONFIG: SNAPSHOT setting in default/user store.
3. At this point the module starts capturing operational parameters in RAM for SNAPSHOT, every firmware cycle.
4. The module is configured to capture operational parameters after a fault during operation.
5. After the fault, disable the SnapShot mode by setting bit 1 of MISC_CONFIG command to 0. This is to prevent firmware from updating RAM values after the fault with current values.
6. Disable the module.
7. Send SNAPSHOT_CONTROL command 1 to read the stored data from flash memory into RAM at any time. Issue a SNAPSHOT command to read the data from RAM through SMBus.
8. Repeat Step 7 to retrieve SNAPSHOT parameters after a power cycle. It is important to make sure SnapShot mode is disabled in MISC_CONFIG command.

Nonvolatile Memory and Device Security Features

The ZL9101M has internal nonvolatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the module to a level that has been made available to them.

During the initialization process, the ZL9101M checks for stored values contained in its internal nonvolatile memory. The ZL9101M offers two internal memory storage units that are accessible by the user as follows:

1. Default Store: The ZL9101M has a default configuration that is stored in the default store in the controller. The module can be restored to its default settings by issuing a RESTORE_DEFAULT_ALL command over the SMBus.
2. User Store: The user can modify certain power supply settings as described in this datasheet. The user stores their configuration in the user store.

Output Capacitor Selection

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in Equations 4 and 5:

$$C_{OUT} = \frac{\Delta I_{L(P-P)}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad \text{(EQ. 4)}$$

$$ESR = \frac{V_{orip}}{2 \times I_{L(P-P)}} \quad \text{(EQ. 5)}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using Equation 6:

$$V_{orip} = \Delta I_{L(P-P)} \times ESR + \frac{\Delta I_{L(P-P)}}{8 \times f_{sw} \times C_{out}} \quad \text{(EQ. 6)}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

Usually, at higher output voltages, inductor ripple current is very high so it is recommended to use a combination of several ceramic capacitor with low ESR bulk capacitors to ensure low output ripple voltage and loop stability. Inadequate amount of capacitance at the output can cause instability to the control loop.

Input Capacitor Selection

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V “bulk” supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from Equation 7:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad \text{(EQ. 7)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2 times the ripple current calculated in Equation 7 to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1 times the maximum expected input voltage are recommended.

Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary.

- Establish a separate ground plane for SGND (Pin 9) and PGND (Pin 10 and Pin 16) and connect them at a single point as shown in Figure 21. CV25, CVR, RSA, and RVSET are placed on the bottom layer and are connected to a single SGND plane that is connected to the PGND at a single point. This will help to block the high frequency noise from entering to the controller through SGND.
- Place a high frequency ceramic capacitor between (1) VIN and PGND (Pin 16), (2) VOUT and PGND (Pin 16), and (3) bypass capacitors between VDRV, VDD, V25, VR, and the ground plane, as close to the module as possible to minimize high frequency noise. High frequency ceramic capacitors close to the module between VOUT and PGND will help to minimize noise at the output ripple.
- Use large copper areas for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Connect remote sensed traces to the regulation point to achieve a tight output voltage regulation and keep them in parallel. Route a trace from FB- to a location near the load ground and a trace from FB+ to the point-of-load where the tight output voltage is desired.
- Avoid routing any sensitive signal traces, such as the VOUT, FB+, FB- sensing point near the PHASE pin.

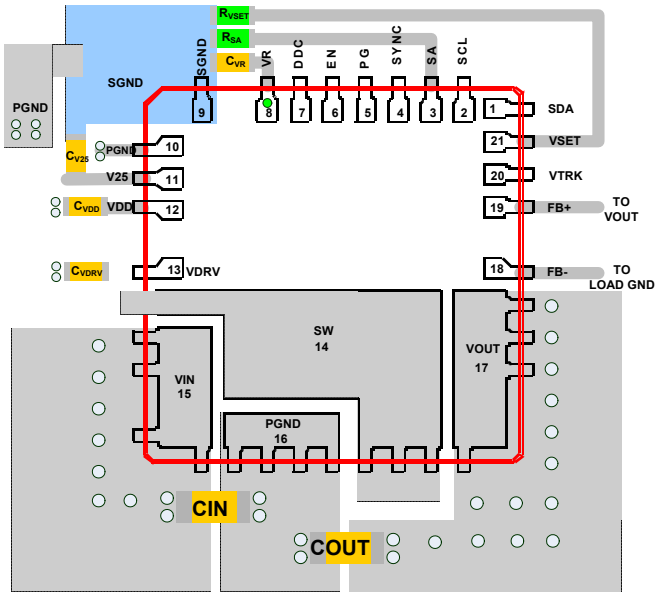


FIGURE 21. RECOMMENDED LAYOUT

Thermal Consideration

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

Package Description

The structure of the ZL9101M belongs to the Quad Flatpack No-lead package (QFN). This kind of package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The QFN package is applicable for surface mounting technology and is being more readily used in the industry. The ZL9101M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ZL9101M is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown on the second page of the “Package Outline Drawing” on page 62. The module has a small size of 15mmx15mmx3.5mm. Figure 22 shows typical reflow profile parameters. These guidelines are general design rules. Users could modify parameters according to their application.

PCB Layout Pattern Design

The bottom of ZL9101M is a leadframe footprint, which is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on the second page of the "Package Outline Drawing" on page 62. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and I/O termination dimensions, except for the PCB lands being a slightly extended distance of 0.2mm (0.4mm max) longer than the QFN terminations, which allows for solder filleting around the periphery of the package. This ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. Stencil aperture size to land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown on the second page of the "Package Outline Drawing" on page 62. The gap width between pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing smooths the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick-like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) QFN.

Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in Figure 22 is provided as a guideline, to be customized for varying manufacturing practices and applications.

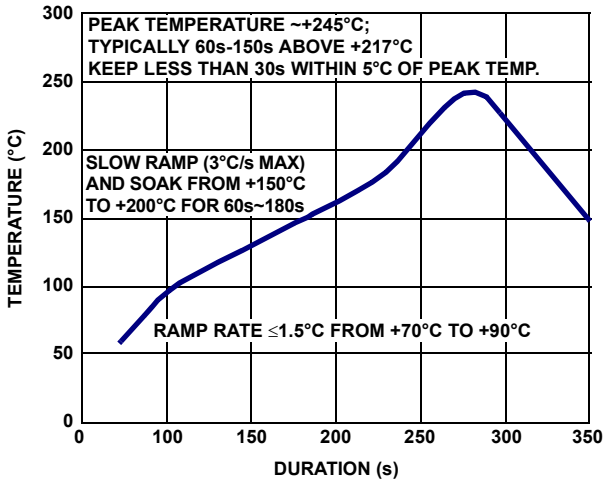


FIGURE 22. TYPICAL REFLOW PROFILE

PMBus Command Summary

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
01h	OPERATION	Sets enable, disable, and V_{OUT} margin modes.	R/W BYTE	BIT			page 25
02h	ON_OFF_CONFIG	Configures device to enable from EN pin or OPERATION command.	R/W BYTE	BIT	16h	Pin Enable Soft Off	page 25
03h	CLEAR_FAULTS	Clear fault indications.	SEND BYTE				page 25
11h	STORE_DEFAULT_ALL	Stores all PMBus values written since last restore at default level.	SEND BYTE				page 26
12h	RESTORE_DEFAULT_ALL	Restores PMBus settings that were stored at default level.	SEND BYTE				page 26
15h	STORE_USER_ALL	Stores all PMBus values written since last restore at user level.	SEND BYTE				page 26
16h	RESTORE_USER_ALL	Restores PMBus settings that were stored in user level.	SEND BYTE				page 26
20h	VOUT_MODE	Preset to defined data format of V_{OUT} commands.	READ BYTE	BIT	13h	Linear Mode, Exponent = -13	page 26
21h	VOUT_COMMAND	Sets the nominal value of V_{OUT}.	R/W WORD	L16u		Pin-Strap	page 27
22h	VOUT_TRIM	Sets trim value on V_{OUT}.	R/W WORD	L16s	0000h	0V	page 27
23h	VOUT_CAL_OFFSET	Applies a fixed offset voltage to the VOUT_COMMAND.	R/W WORD	L16s	0000h	0V	page 27
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}.	R/W WORD	L16u		1.1*V_{OUT} Pin-Strap	page 27
25h	VOUT_MARGIN_HIGH	Sets the value of the V_{OUT} during a margin high.	R/W WORD	L16u		1.05*V_{OUT} Pin-Strap	page 27
26h	VOUT_MARGIN_LOW	Sets the value of the V_{OUT} during a margin low.	R/W WORD	L16u		0.95*V_{OUT} Pin-Strap	page 28
27h	VOUT_TRANSITION_RATE	Sets the transition rate during margin or other change of V_{OUT}.	R/W WORD	L11	BA00h	1V/ms	page 28
28h	VOUT_DROOP	Sets the loadline (V/I Slope) resistance for the rail.	R/W WORD	L11	0000h	0mV/A	page 28
32h	MAX_DUTY	Sets the maximum allowable duty cycle.	R/W WORD	L11	EADBh	91.375%	page 28
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W WORD	L11		Pin-Strap	page 28
37h	INTERLEAVE	Sets a phase offset between devices sharing a SYNC clock.	R/W WORD	BIT		Pin-Strap Setting	page 29
38h	IOUT_CAL_GAIN	Sense resistance for inductor DCR current sensing.	R/W WORD	L11	BA2Ah	1.083mΩ	page 29
39h	IOUT_CAL_OFFSET	Sets the current-sense offset.	R/W WORD	L11	BE00h	-1A	page 29
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W WORD	L16u		1.15 * V_{OUT} Pin-Strap	page 29
41h	VOUT_OV_FAULT_RESPONSE	Configures the V_{OUT} overvoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	page 30
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W WORD	L16u		0.85*V_{OUT} Pin-Strap	page 30
45h	VOUT_UV_FAULT_RESPONSE	Configures the V_{OUT} undervoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	page 31
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold.	R/W WORD	L11	E200h	32A	page 31
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold.	R/W WORD	L11	E600h	-32A	page 31
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W WORD	L11	EBE8h	+125°C	page 32

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
50h	OT_FAULT_RESPONSE	Configures the over-temperature fault response.	R/W BYTE	BIT	80h	Disable and No Retry	page 32
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit.	R/W WORD	L11	EB70h	+110°C	page 32
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit.	R/W WORD	L11	E4E0h	-50°C	page 33
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W WORD	L11	E490h	-55°C	page 33
54h	UT_FAULT_RESPONSE	Configures the under-temperature fault response.	R/W BYTE	BIT	80h	Disable and No Retry	page 33
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W WORD	L11	D3A0h	14.5V	page 34
56h	VIN_OV_FAULT_RESPONSE	Configures the V_{IN} overvoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	page 34
57h	VIN_OV_WARN_LIMIT	Sets the V_{IN} overvoltage warning limit.	R/W WORD	L11	D34Dh	13.2V	page 34
58h	VIN_UV_WARN_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W WORD	L11	CA30h	4.38V	page 35
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage warning limit.	R/W WORD	L11	CA00h	4V	page 35
5Ah	VIN_UV_FAULT_RESPONSE	Configures the V_{IN} undervoltage fault response.	R/W BYTE	BIT	80h	Disable and No Retry	page 35
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication.	R/W WORD	L16u		0.9 * V_{OUT} Pin-Strap	page 35
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W WORD	L11	CA80h	5ms	page 36
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W WORD	L11	D280h	10ms	page 36
64h	TOFF_DELAY	Sets the delay time from DISABLE to START of V_{OUT} fall.	R/W WORD	L11	CA80h	5ms	page 36
65h	TOFF_FALL	Sets the fall time of V_{OUT} after DISABLE and TOFF_DELAY.	R/W WORD	L11	D280h	10ms	page 36
78h	STATUS_BYTE	Summary of most critical faults.	READ BYTE	BIT	00h	No faults	page 37
79h	STATUS_WORD	Summary of critical faults.	READ WORD	BIT	0000h	No faults	page 37
7Ah	STATUS_VOUT	Reports V_{OUT} warnings/faults.	READ BYTE	BIT	00h	No faults	page 38
7Bh	STATUS_IOUT	Reports I_{OUT} warnings/faults.	READ BYTE	BIT	00h	No faults	page 38
7Ch	STATUS_INPUT	Reports input warnings/faults.	READ BYTE	BIT	00h	No faults	page 38
7Dh	STATUS_TEMPERATURE	Reports temperature warnings/faults.	READ BYTE	BIT	00h	No faults	page 39
7Eh	STATUS_CML	Reports communication, memory, logic errors.	READ BYTE	BIT	00h	No faults	page 39
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock sync faults.	READ BYTE	BIT	00h	No faults	page 40
88h	READ_VIN	Reports input voltage measurement.	READ WORD	L11			page 40
8Bh	READ_VOUT	Reports input current measurement.	READ WORD	L16u			page 40
8Ch	READ_IOUT	Reports output current measurement.	READ WORD	L11			page 40
8Dh	READ_TEMPERATURE_1	Reports temperature reading internal to the device	READ WORD	L11			page 40
94h	READ_DUTY_CYCLE	Reports actual duty cycle.	READ WORD	L11			page 41
95h	READ_FREQUENCY	Reports actual switching frequency.	READ WORD	L11			page 41
98h	PMBUS_REVISION	Returns the revision of the PMBus.	READ BYTE	HEX			page 41
99h	MFR_ID	Sets a user defined identification.	R/W BLOCK	ASC		<null>	page 41

PMBus Command Summary (Continued)

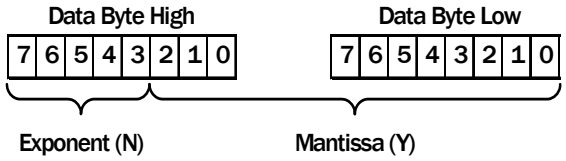
COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
9Ah	MFR_MODEL	Sets a user defined model.	R/W BLOCK	ASC		<null>	page 41
9Bh	MFR_REVISION	Sets a user defined revision.	R/W BLOCK	ASC		<null>	page 41
9Ch	MFR_LOCATION	Sets a user defined location identifier.	R/W BLOCK	ASC		<null>	page 42
9Dh	MFR_DATE	Sets a user defined data.	R/W BLOCK	ASC		<null>	page 42
9Eh	MFR_SERIAL	Sets a user defined serialized identifier.	R/W BLOCK	ASC		<null>	page 42
B0h	USER_DATA_00	Sets a user defined data.	R/W BLOCK	ASC		<null>	page 42
BCh	AUTO_COMP_CONFIG	Configures the auto compensation features.	R/W BYTE	CUS	69h	Auto comp enabled gain = 70%	page 43
BDh	AUTO_COMP_CONTROL	Causes the auto comp algorithm to initiate.	SEND BYTE	BIT			page 43
BFh	DEADTIME_MAX	Sets the maximum dead time values.	R/W WORD	CUS	3838h	HIGH to LOW = 56ns LOW to HIGH = 56ns	page 43
D0h	MFR_CONFIG	Configures several manufacturer level features.	R/W WORD	BIT	6A11h	Refer to description	page 44
D1h	USER_CONFIG	Configures several user level features.	R/W WORD	BIT	2011h	Refer to description	page 45
D2h	ISHARE_CONFIG	Configures the device for current sharing mode.	R/W WORD	BIT	0000h	Current share disabled	page 46
D3h	DDC_CONFIG	Configures the DDC bus.	R/W WORD	BIT		Set based on PMBus Address	page 46
D4h	POWER_GOOD_DELAY	Sets the delay PG threshold and asserting the PG pin.	R/W WORD	L11	BA00h	1ms	page 46
D5h	PID_TAPS	Configures the control loop compensator coefficients.	R/W BLOCK	CUS		Calculated by auto comp	page 47
D6h	INDUCTOR	Sets the inductor value	R/W WORD	L11	B0E1h	0.22µH	page 47
D7h	NLR_CONFIG	Configures the nonlinear response (NLR) control.	R/W WORD	BIT	00000000h	Refer to description section	page 48
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection.	R/W BYTE	BIT	00h	Fastest response no crowbar	page 48
DCh	TEMPCO_CONFIG	Sets tempco settings.	R/W BYTE	CUS	2Ch	4400 ppm/°C	page 49
DDh	DEADTIME	Sets default dead time settings.	R/W WORD	CUS	1018h	HIGH to LOW = 16ns LOW to HIGH = 24ns	page 49
DEh	DEADTIME_CONFIG	Configures the adaptive dead time optimization mode.	R/W WORD	CUS	8686h	Adaptive dead time disabled	page 50
E0h	SEQUENCE	DDC rail sequencing configuration.	R/W WORD	BIT	0000h	Prequel and sequel disabled	page 50
E1h	TRACK_CONFIG	Configures voltage tracking modes.	R/W BYTE	BIT	00h	Tracking disabled	page 51
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION, and V_{OUT}.	R/W BLOCK	BIT	00000000h	Ignore fault spread	page 51
E4h	DEVICE_ID	Returns the device identifier string,	READ BLOCK	ASC		Reads device version	page 51

PMBus Command Summary (Continued)

COMMAND CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING	PAGE
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 52
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W BYTE	BIT	80h	Disable and no retry	page 52
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W WORD	L11	DA80h	20A	page 53
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the IOUT average undercurrent fault threshold.	R/W WORD	L11	DD80h	-20A	page 53
E9h	MISC_CONFIG	Sets options pertaining to advanced features.	R/W WORD	BIT	0400h	Broadcast disabled	page 53
EAh	SNAPSHOT	32-byte read-back of parametric and status values	READ BLOCK	BIT		N/A	page 54
EBh	BLANK_PARAMS	Indicates recently saved parameter values	READ BLOCK	BIT	FF...FFh		page 54
F0h	PHASE_CONTROL	Controls phase adding/dropping for current sharing configuration.	R/W BYTE	BIT	00h	All phases active	page 54
F3h	SNAPSHOT_CONTROL	Controls how snapshot values are handled.	R/W BYTE	BIT			page 55
F4h	RESTORE_FACTORY	Restores device to the hard coded default values	SEND BYTE				page 55
F5h	MFR_VMON_OV_FAULT_LIMIT	Sets the VDRV overvoltage fault threshold	R/W WORD	L11	CB80h	7V	page 55
F6h	MFR_VMON_UV_FAULT_LIMIT	Sets the VDRV undervoltage fault threshold	R/W WORD	L11	CA40h	4.5V	page 55
F7h	MFR_READ_VMON	Reads the VDRV voltage	READ WORD	L11			page 55
F8h	VMON_OV_FAULT_RESPONSE	Configures the VDRV overvoltage fault response	R/W BYTE	BIT	80h	Disable and no retry	page 56
F9h	VMON_UV_FAULT_RESPONSE	Configures the VDRV undervoltage fault response	R/W BYTE	BIT	80h	Disable and no retry	page 56
FAh	SECURITY_LEVEL	Reports the security level	READ BYTE	HEX	01h	Public security level	page 57
FBh	PRIVATE_PASSWORD	Sets the private password string	R/W BLOCK	ASC	000...00h		page 58
FCh	PUBLIC_PASSWORD	Sets the public password string	R/W BLOCK	ASC	00...00h		page 58
FDh	UNPROTECT	Identifies which commands are protected	R/W BLOCK	CUS	FF...FFh		page 58

PMBus Data Formats

Linear-11 (L11)
The L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal value (X).



The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{N}$

Linear-16 Unsigned (L16u)
The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$

Linear-16 Signed (L16s)
The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N, and Y is: $X = Y \cdot 2^{-13}$

Bit Field (BIT)
A breakdown of Bit Field is provided in the following "PMBus Commands Description" section.

Custom (CUS)
A breakdown of the Custom data format is provided in the following "PMBus Commands Description" section. A combination of Bit Field and integer are common type of Custom data format.

ASCII (ASC)
A variable length string of text characters uses the ASCII data format.

PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

When sending the STORE_DEFAULT_ALL, STORE_USER_ALL, RESTORE_DEFAULT_ALL, and RESTORE_USER_ALL commands, it is recommended that no other commands are sent to the device for 100ms after sending STORE or RESTORE commands.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Commands not listed in the PMBus command summary are not allowed for customer use, and may be reserved for factory use only.

Summary

All commands can be read at any time.

Always disable the device when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a change to a device setting has taken effect, write the STORE_USER_ALL command, then cycle input power and re-enable.

PMBus Commands Description

OPERATION (01h)

Definition: Sets Enable, Disable, and V_{OUT} Margin settings. If multiple ZL9101M modules are configured as a current sharing rail and at the mean time are configured to start/shutdown from ENABLE pin (in the ON_OFF_CONFIG), then the margining of the current sharing rail should follow this procedure: The desired OPERATION command should be sent to all the member modules first, then the same OPERATION command is sent to the reference module at last.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: N/A

Units: N/A

SETTINGS	ACTIONS
04h	Immediate off (no sequencing)
44h	Soft-off (with sequencing)
84h	On - Nominal
94h	On - Margin low
A4h	On - Margin high

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 16h (Device starts/shutdown from ENABLE pin with soft off)

Units: N/A

SETTINGS	ACTIONS
00h	Device starts any time power is present regardless of ENABLE pin or OPERATION command states.
16h	Device starts/shutdowns from ENABLE pin with soft off option.
17h	Device starts/shutdowns from ENABLE pin with immediate off option.
1Ah	Device starts/shutdowns from OPERATION command.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

STORE_DEFAULT_ALL (11h)

Definition: Stores all current PMBus values from the operating memory into the nonvolatile DEFAULT Store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. This command should not be used during device operation, the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

RESTORE_DEFAULT_ALL (12h)

Definition: Restores PMBus settings from the nonvolatile DEFAULT Store memory into the operating memory. These settings are loaded at power-up if not superseded by settings in USER store. Security level is changed to Level 1 following this command. This command should not be used during device operation.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus settings from the operating memory to the nonvolatile USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command can be used during device operation, but the device will be unresponsive for 20ms while storing values.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus settings from the USER store memory to the operating memory. Command performed at power-up. Security level is changed to Level 1 following this command. This command can be used during device operation.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings. Fixed with linear mode with default exponent (N) = -13.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 13h (Linear Mode, N = -13)

Units: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than either VOUT_MAX or 110% of the pin-strap V_{OUT} setting.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: Pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_TRIM (22h)

Definition: Sets a trim value on V_{OUT}.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W Word

Default Value: 0000h

Units: Volts

Range: -4V to 4V

VOUT_CAL_OFFSET (23h)

Definition: Applies a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit.

Data Length in Bytes: 2

Data Format: L16s

Type: R/W Word

Default Value: 0000h

Units: Volts

Range: -4V to 4V

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 1.10 x VOUT_COMMAND pin-strap setting

Units: Volts

Range: 0V to 4V

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default value: 1.05 x VOUT_COMMAND pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the VOUT during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default value: 0.95 x VOUT_COMMAND pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_TRANSITION_RATE (27h)

Definition: Sets the rate at which the output should change voltage when the device receives an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default value: BA00h (1.0V/ms)

Units: V/ms

Range: 0.1 to 4V/ms

VOUT_DROOP (28h)

Definition: Sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A, at which the output voltage decreases (or increases) with increasing (or decreasing) output current for use with adaptive voltage positioning requirements and passive current sharing schemes.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default value: 0000h (0mV/A)

Units: mV/A

Range: 0 to 40mV/A

MAX_DUTY (32h)

Definition: Sets the maximum allowable duty cycle

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: EADBh (91.375%)

Units: %

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command through PMBus. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: Pin-strap setting

Units: kHz

Range: 400kHz to 1000kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A value of 0 for the Number in Group field is interpreted as 16, to allow for phase spreading groups of up to 16 devices. For current sharing rails, INTERLEAVE is used to set the initial phase of the rail. The current share devices then automatically distribute their phase relative to the INTERLEAVE. setting.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: Set based on pin-strap PMBus address

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:2	Reserved	0	Reserved
11:8	Group Number	0 to 15	Sets a number to a group of interleaved rails.
7:4	Number in Group	0 to 15	Sets the number of rails in the group A value of 0 is interpreted as 16.
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group.

IOUT_CAL_GAIN (38h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating output current at +25°C.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: BA2Ah (1.083mΩ)

Units: mΩ

IOUT_CAL_OFFSET (39h)

Definition: Used to null out any offsets in the output current sensing circuit and to compensate for delayed measurements of current ramp due to Isense blanking time.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: BE00h (-1A)

Units: A

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 1.15 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response. Note that the device cannot be set to ignore this fault mode. The retry time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when the device is disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 0.85 x VOUT_COMMAND pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable, no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the inductor peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. A fault occurs after this limit is exceeded for the number of consecutive samples as defined in MFR_CONFIG.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: E200h (32A)

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the inductor valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the current sense blanking time has expired. A fault occurs after this limit is exceeded for the number of consecutive samples as defined in MFR_CONFIG.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: E600h (-32A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: EBE8h (+125°C)

Units: Celsius

Range: 0°C to +175°C

OT_FAULT_RESPONSE (50h)

Definition: Instructs the device on what action to take in response to an over-temperature fault. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

OT_WARN_LIMIT (51h)

Definition: Sets the temperature at which the device should indicate an over-temperature warning alarm. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the OT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: EB70h (+110°C)

Units: Celsius

Range: 0°C to +175°C

UT_WARN_LIMIT (52h)

Definition: Sets the temperature at which the device should indicate an under-temperature warning alarm. In response to the UT_WARN_LIMIT being exceeded, the device sets the TEMPERATURE bit in STATUS_WORD, sets the UT_WARNING bit in STATUS_TEMPERATURE, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: E4E0h (-50°C)

Units: Celsius

Range: -55°C to +25°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature at which the device should indicate an under-temperature fault. Note that the temperature must rise above UT_WARN_LIMIT to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: E490h (-55°C)

Units: Celsius

Range: -55°C to +25°C

UT_FAULT_RESPONSE (54h)

Definition: Instructs the device on what action to take in response to an under-temperature fault. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable, no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: D3A0h (14.5V)

Units: V

Range: 0 to 16V

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold. In response to the VIN_OV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_OV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: D34Dh (13.2V)

Units: V

Range: 0V to 19V

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. If a VIN_UV_FAULT occurs, the input voltage must rise above VIN_UV_WARN_LIMIT to clear the fault, which provides hysteresis to the fault threshold. In response to the UV_WARN_LIMIT being exceeded, the device sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, sets the VIN_UV_WARNING bit in STATUS_INPUT, and notifies the host.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: CA30h (4.38V)

Units: V

Range: 0V to 19V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: CA00h (4V)

Units: V

Range: 0V to 12V

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response. The delay time is the time between restart attempts.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and Retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No Retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W Word

Default Value: 0.9 x VOUT_COMMAND pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: CA80h (5ms)
Units: ms
Range: 0 to 500ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: D280h (10ms)
Units: ms
Range: 0 to 200ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: CA80h (5ms)
Units: ms
Range: 0 to 500ms

TOFF_FALL (65h)

Definition: Sets the fall time for VOUT after DISABLE and TOFF_DELAY.
Data Length in Bytes: 2
Data Format: L11
Type: R/W Word
Default Value: D280h (10ms)
Units: ms
Range: 0 to 200ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default Value: 00h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read Word

Default Value: 0000h

Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT/POUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	FANS	A fan or airflow fault or warning has occurred.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in Bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	NONE OF THE ABOVE	A fault or warning not listed in Bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.
Data Length in Bytes: 1
Data Format: BIT
Type: Read Byte
Default Value: 00h
Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	Indicates an output overvoltage warning.
5	VOUT_UV_WARNING	Indicates an output undervoltage warning.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.
Data Length in Bytes: 1
Data Format: BIT
Type: Read Byte
Default Value: 00h
Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_OC_WARNING (not used)	Reserved
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns input voltage and input current status information.
Data Length in Bytes: 1
Data Format: BIT
Type: Read Byte
Default Value: 00h
Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	N/A	These bits are not used.

STATUS_TEMPERATURE (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults or warnings.
Data Length in Bytes: 1
Data Format: BIT
Type: Read Byte
Default Value: 00h
Units: N/A

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and memory errors.
Data Length in Bytes: 1
Data Format: BIT
Type: Read Byte
Default Value: 00h
Units: N/A

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus Command was received.
6	The PMBus command was sent with Invalid or Unsupported data.
5	A packet error was detected in the PMBus command.
4:2	Not Used
1	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not Used

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults. VDRV OV/UV warnings are set at ±10% of the VMON_OV_FAULT/VMON_UV_FAULT commands.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Byte

Default value: 00h

Units: N/A

BIT NUMBER	FIELD NAME	MEANING
7:6	Reserved	
5	VDRV UV Warning	The voltage on the VMON pin has dropped 10% below the level set by VDRV_UV_FAULT.
4	VDRV OV Warning	The voltage on the VMON pin has risen 10% above the level set by VDRV_OV_FAULT.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Reserved	
1	VDRV UV Fault	The voltage on the VMON pin has dropped below the level set by VDRV_UV_FAULT.
0	VDRV OV Fault	The voltage on the VMON pin has risen above the level set by VDRV_OV_FAULT.

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: L16u

Type: Read Word

Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Default Value: N/A

Units: A

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Units:%

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Units: kHz

PMBUS_REVISION (98h)

Definition: Returns the revision of the PMBus implemented in the device.

Data Length in Bytes: 1

Data Format: HEX

Type: Read Byte

Units: N/A

MFR_ID (99h)

Definition: Sets a user defined identification. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_MODEL (9Ah)

Definition: Sets a user defined model. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_REVISION (9Bh)

Definition: Sets a user defined revision. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_LOCATION (9Ch)

Definition: Sets a user defined location identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_DATE (9Dh)

Definition: Sets a user defined date. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

MFR_SERIAL (9Eh)

Definition: Sets a user defined serialized identifier. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASC

Type: Block R/W

Default Value: null

Units: N/A

USER_DATA_00 (B0h)

Definition: Sets a user defined data. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL, and USER_DATA_00 plus one byte per command cannot exceed 128 characters. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: user defined

Data Format: ASCII

Type: Block R/W

Default Value: null

Units: N/A

AUTO_COMP_CONFIG (BCh)

Definition: Controls configuration of auto compensation features.

Data Length in Bytes: 1

Data Format: CUS

Type: R/W Byte

Default Value: 69h (Auto Comp Once, Do not store results, PG assertion after Auto Comp, and Gain = 70%)

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
7:4	Auto Comp Gain Percentage	G	Scale the Gain of the Auto-Compensation results by a factor of (G+1)*10%, where 0 ≤ G ≤ 9. G = 0 yields lowest jitter; G = 9 yields tightest transient response.
3	Power Good Assertion	0	Use PG_DELAY
		1	Assert PG after Auto Comp completes
2	Auto Comp Store	0	Do not store Auto Comp results.
		1	Store Auto Comp results for use on future ramps.
1:0	Auto Comp Mode	0	Off (Disabled). Compensation stored in PID_TAPS will be used.
		1	Once (results are storable)
		2	Repeat every ~1 second (only the first results are storable).
		3	Repeat every ~1 minute (only the first results are storable).

AUTO_COMP_CONTROL (BDh)

Definition: Causes the Auto Comp algorithm to initiate when the Auto Comp feature is enabled in AUTO_COMP_CONFIG.

Data Length in Bytes: 0

Data Format: BIT

Type: Send Byte

Default Value:

Units: N/A

DEADTIME_MAX (BFh)

Definition: Sets the maximum dead time value for the PWMH and PWML outputs. This limit applies during frozen or adaptive dead time algorithm modes (see DEADTIME_CONFIG).

Data Length in Bytes: 2

Data Format: CUS

Type: R/W Word

Default Value: 3838h (56ns/56ns)

Units: ns

Range: 0 to 60ns

BITS	PURPOSE	VALUE	DESCRIPTION
15	Not Used	0	Not used
14:8	Sets the maximum HIGH to LOW dead time	H	Limits the maximum allowed HIGH to LOW dead time when using the adaptive dead time algorithm. Dead time = Hns (signed)
7	Not Used	0	Not used
6:0	Sets the maximum LOW to HIGH dead time	L	Limits the maximum allowed LOW to HIGH dead time when using the adaptive dead time algorithm. Dead time = Lns (signed)

MFR_CONFIG (D0h)

Definition: Configures several manufacturer-level features.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 6A11h (416ns, 5 Count, Down Slope, NLR wait for PG, PG Open-Drain, Sync Push-Pull)

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:11	Current Sense Blanking Delay	D	Sets the delay, D, in 32ns steps
10:8	Current Sense Fault Count	C	Sets the number of consecutive OC or UC violations required for a fault to 2C+1.
7:6	Reserved		
5:4	Current Sense Control	00	Current sense uses GND-referenced, down-slope sense
		01	Current sense uses V_{OUT}-referenced, down-slope sensing
		10	Current sense uses V_{OUT}-referenced, up-slope sensing
		11	Reserved
3	NLR During Ramp	0	Wait for PG
		1	Always on
2	Alternate Ramp Control	0	Alternate ramp disabled
		1	Alternate ramp enabled
1	PG Pin Output Control	0	PG is open-drain
		1	PG is push-pull
0	SYNC Pin Output Control	0	SYNC is open-drain
		1	SYNC is push-pull

USER_CONFIG (D1h)

Definition: Configures several user-level features.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 2011h (Min Duty Enabled = 1* t_{SW}/256, PID feed forward correct for VDD, Ignore Fault spread, Clock SYNC pin-strap mode, use internal clock, low-side MOSFET off when disabled, Monitor mode enabled).

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:14	Minimum Duty Cycle	N	Sets the minimum duty cycle ((N+1)/(2^8)) during a ramp when "Minimum Duty Cycle" (Bit 13) is enabled. For example, if Minimum Duty Cycle input N is set to 3, the minimum duty cycle is (3+1)/(2^8) = (1/64).
13	Minimum Duty Cycle Control	0	Minimum duty cycle is disabled.
		1	Minimum duty cycle is enabled.
12	Reserved	0	
11	SYNC Time-out Enable	0	SYNC output remains on after device is disabled.
		1	SYNC turns off 500ms after device is disabled.
10	Reserved	-	Reserved
9	PID Feed-Forward Control	0	PID coefficients are corrected for V_{DD} variations.
		1	PID coefficients are not corrected for V_{DD} variations.
8	Fault Spreading Mode	0	If sequencing is disabled, this device will ignore faults from other devices. If sequencing is enabled, the devices will sequence down from the failed device outward.
		1	Faults received from any device selected by the DDC_GROUP command will cause this device to shut down immediately.
7	SMBus Transmit Clk Rate	0	SMBus transmit is always disabled in DDC devices.
6	SYNC Utilization Control	0	Auto-configure using the SYNC pin and FREQUENCY_SWITCH parameter
		1	Switch using the SYNC input.
5	SYNC Output Control	0	Configure the SYNC pin as an input only.
		1	Drive the switch clock out of SYNC when using the internal oscillator.
4	SMBus Transmit Inhibit	0	SMBus transmit is always disabled in DDC devices.
3	SMBus Timeout Inhibit	0	SMBus transmit is always disabled in DDC devices.
2	OFF Low-side Control	0	The low-side drive is off when device is disabled.
		1	The low-side drive is on when device is disabled.
1:0	Standby Mode	00	Enter low-power mode when device is disabled (no READ_xxxx data available).
		01	Monitor for faults when device is disabled (READ_xxxx data available).
		10	Reserved
		11	Monitor for faults using pulsed mode. (READ_xxxx data available upon read command).

ISHARE_CONFIG (D2h)

Definition: Configures the device for current sharing communication over the DDC bus.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 0000h (Device configured to operate in signal phase mode)

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:8	IShare DDC ID	0 to 31 (0x00 to 0x1F)	Sets the current share rail's DDC ID for each device within a current share rail. Set to the same DDC ID as in DDC_CONFIG. This DDC ID is used for sequencing and fault spreading when used in a current share rail.
7:5	Number of Members	0 to 7	Number of devices in current share rail -1. Example: 3 device current share rail, use 3 – 1 = 2
4:2	Member Position	0 to 7	Position of device within current share rail.
1	Reserved	0	Reserved
0	I-Share Control	1	Device is a member of a current share rail.
		0	Device is not a member of a current share rail.

DDC_CONFIG (D3h)

Definition: Configures the DDC bus.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 5 bit LSB of SMBus address

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15:13	Reserved	0	Reserved
12:8	Broadcast Group	0 to 31	Group number used for broadcast events. (i.e., Broadcast Enable and Broadcast Margin) Set this number to the same value for all rails/devices that should respond to each other's broadcasted event. This function is enabled by the Bits 15 and 14 in the MISC_CONFIG command.
7:6	Reserved	0	Reserved
5	DDC TX Inhibit	1	DDC transmission inhibited.
		0	DDC transmission enabled.
4:0	DDC ID	0 to 31	Sets the rail's DDC ID for sequencing and fault spreading. For the current-sharing applications, set this value the same as the ID value in ISHARE_CONFIG for all devices in the current sharing rail.

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 5s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: BA00h (1ms)

Units: ms

Range: 0ms to 5s

PID_TAPS (D5h)

Definition: Configures the control lop compensator coefficients.

The PID algorithm implements the following Z-domain function in Equation 8:

$$\frac{A + Bz^{-1} + Cz^{-2}}{1 - z^{-1}} \quad \text{(EQ. 8)}$$

The coefficients A, B, and C are represented using a pseudo-floating point format similar to the V_{OUT} parameters (with the addition of a sign bit), defined as Equation 9:

$$A = (-1)^{S} \bullet 2^{E} \bullet M \quad \text{(EQ. 9)}$$

where M is a two-byte unsigned mantissa, S is a sign-bit and E is a 7-bit two's-complement signed integer. The 9-byte data field is defined in the table below. S is stored as the MSB of the E byte.

Data Length in Bytes: 9

Data Format: CUS

Type: R/W Block

Default Value: Auto Comp stores when algorithm is initiated during start-up. When Auto Comp is disabled PID_TAPS can be stored through PMBus.

Units: N/A

BYTE	PURPOSE	DEFINITION
8	Tap C - E	Coefficient C exponent + S
7	Tap C - M [15:8]	Coefficient C mantissa, high-byte
6	Tap C - M [7:0]	Coefficient C mantissa, low-byte
5	Tap B - E	Coefficient B exponent + S
4	Tap B - M [15:8]	Coefficient B mantissa, high-byte
3	Tap B - M [7:0]	Coefficient B mantissa, low-byte
2	Tap A - E	Coefficient A exponent + S
1	Tap A - M [15:8]	Coefficient A mantissa, high-byte
0	Tap A - M [7:0]	Coefficient A mantissa, low-byte

NOTE: Data bytes are transmitted on the PMBus in the order of Byte 0 through Byte 8.

INDUCTOR (D6h)

Definition: Informs the device of the circuit's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: B0E1h (0.22µH)

Units: µH

NLR_CONFIG (D7h)

Definition: Configures the nonlinear response control parameters.
Data Length in Bytes: 4
Data Format: BIT
Type: R/W
Default Value: 00000000h
Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
31:30	Outer Threshold Multiplier	O	Sets multiplier of inner threshold for outer threshold setting, O*LI and O*UI.
29:27	NLR Comparator Threshold: Loading-Inner	LI	Sets inner threshold for a loading event to ~0.5%*(LI+1)*V_{OUT}.
26:24	NLR Comparator Threshold: Unloading-Inner	UI	Sets inner threshold for an unloading event to ~0.5%*(UI+1)*V_{OUT}.
23:20	Loading-Outer Threshold Max Correction Time	LOT	Sets outer threshold, maximum correction time for a loading event to LOT*t_{SW}/64 (s).
19:16	Loading-Inner Threshold Max Correction Time	LIT	Sets inner threshold, maximum correction time for a loading event to LIT*t_{SW}/64 (s).
15:12	Unloading-Outer Threshold Max Correction Time	UOT	Sets outer threshold, maximum correction time for an unloading event to UOT*t_{SW}/64 (s).
11:8	Unloading-Inner Threshold Max Correction Time	UIT	Sets inner threshold, maximum correction time for an unloading event to UIT*t_{SW}/64 (s).
7:4	Load Blanking Time Control	LB	Sets NLR blanking time for a loading event.
3:0	Unload Blanking Time Control	UB	Sets NLR blanking time for an unloading event.

TABLE 6. LOADING/UNLOADING BLANKING TIMES

LB OR UB	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
t_{SW}/64 UNITS	1	2	3	5	9	17	33	49	65	81	97	129	161	177	193	225

OVUV_CONFIG (D8h)

Definition: Configures the output voltage OV and UV fault detection feature. The default value of 00h is recommended.
Data Length in Bytes: 1
Data Format: Bit
Type: R/W Byte
Default Value: 00h (One violation trigger V_{OUT} fault, OV fault does not enable low-side power device)
Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
7	Controls How an OV Fault Response Shutdown Sets the Output Driver State	0	An OV fault does not enable low-side power device
		1	An OV fault enables the low-side power device
6:4	Not Used	0	Not used
3:0	Defines the Number of Consecutive Limit Violations Required to Declare an OV or UV Fault	N	N+1 consecutive OV or UV violations initiate a fault response

TEMPCO_CONFIG (DCh)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values are applied as negative correction to a positive temperature coefficient.

Data Length in Bytes: 1

Data Format: CUS

Type: R/W Byte

Protectable: Yes

Default Value: 2Ch (4400ppm/°C)

Equation: To determine the hex value of the Tempco Correction factor (TC) for current scale of a power stage current sensing, first determine the temperature coefficient of resistance for the sensing element, α. This is found with Equation 10:

$$\alpha = \frac{R_{REF} - R}{R_{REF}(T_{REF} - T)} \quad \text{(EQ. 10)}$$

where:

R = Sensing element resistance at temperature "T"
R_{REF} = Sensing element resistance at reference temperature T_{REF}
α = Temperature coefficient of resistance for the sensing element material
T = Temperature measured by temperature sensor, in °C
T_{REF} = Reference temperature that α is specified at for the sensing element material

After α is determined, convert the value in units of 100ppm/°C. This value is then converted to a hex value with Equation 11:

$$TC = \frac{\alpha \times 10^6}{100} \quad \text{(EQ. 11)}$$

Typical Values: Copper = 3900ppm/°C (27h), silicon = 4800ppm/°C (30h)

Range: 0 to 6300ppm/°C

BITS	PURPOSE	VALUE	DESCRIPTION
7	Selects the Temp Sensor Source for Tempco Correction	0	Selects the internal temperature sensor
6:0	Sets the Tempco Correction in Units of 100ppm/°C for IOUT_CAL_GAIN	TC	RSEN (DCR) = IOUT_CAL_GAIN x (1+TC x (T-25)) where RSEN = resistance of sense element

DEADTIME (DDh)

Definition: Sets the non-overlap between PWM transitions using a 2-byte data field. The most significant byte controls the high-side to low-side dead time value as a single 2's-complement signed value in units of ns. The least significant byte controls the low-side to high-side dead time value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. The device will operate at the dead time values written to this command when adaptive dead time is disabled, between the minimum dead time specified in DEADTIME_CONFIG and the maximum dead time specified in DEADTIME_MAX. When switching from adaptive dead time mode to frozen mode (by writing to bit 15 of DEADTIME_CONFIG) the frozen dead time will be whatever the last dead time was before the device switches to frozen dead time mode.

Data Length in Bytes: 2

Data Format: CUS

Type: R/W Word

Default Value: 1018h (H-L = 16ns, L-H = 24ns)

Units: ns

Range: -15ns to 60ns

DEADTIME_CONFIG (DEh)

Definition: Configures the adaptive dead time optimization mode. Also sets the minimum dead time value for the adaptive dead time mode range.

Data Length in Bytes: 2

Data Format: CUS

Type: R/W Word

Default Value: 8686h (Adaptive dead time disabled)

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15	Sets the HIGH to LOW Transition Dead Time Mode	0	Adaptive HIGH to LOW dead time control
		1	Freeze the HIGH to LOW dead time
14:8	Sets the Minimum HIGH to LOW Dead Time	0-126d	Limits the minimum allowed HIGH to LOW dead time when using the adaptive dead time algorithm (2ns resolution)
7	Sets the LOW to HIGH Transition Dead Time Mode	0	Adaptive LOW to HIGH dead time control
		1	Freeze the LOW to HIGH dead time
6:0	Sets the Minimum LOW to HIGH Dead Time	0-126d	Limits the minimum allowed LOW to HIGH dead time when using the adaptive dead time algorithm (2ns resolution)

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multirail sequencing. The device will enable its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a power-down event on the DDC bus. The data field is a two-byte value. The most significant byte contains the 5-bit Rail DDC ID of the prequel device. The least significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode. This command overrides the corresponding sequence configuration set by the CONFIG pin settings.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 0000h (Prequel and Sequel disabled)

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail.
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8.
14:13	Reserved	0	Reserved	Reserved
12:8	Prequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the prequel rail.
7	Sequel Enable	0	Disable	Disable, no sequel following this rail.
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0.
6:5	Reserved	0	Reserved	Reserved
4:0	Sequel Rail DDC ID	0-31	DDC ID	Set to the DDC ID of the sequel rail.

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 00h (Tracking disabled)

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7	Voltage Tracking Control	0	Disable	Tracking is disabled.
		1	Enable	Tracking is enabled.
6:3	Reserved		Reserved	Reserved
2	Tracking Ratio Control	0	100%	Output tracks at 100% ratio of VTRK input.
		1	50%	Output tracks at 50% ratio of VTRK input.
1	Tracking Upper Limit	0	Target Voltage	Output voltage is limited by target voltage.
		1	VTRK Voltage	Output voltage is limited by VTRK voltage.
0	Ramp-Up Behavior	0	Track after PG	The output is not allowed to track VTRK down before power-good.
		1	Track always	The output is allowed to track VTRK down before power-good.

DDC_GROUP (E2h)

Definition: Sets which rail DDC IDs a device should listen to for fault spreading information. A device can follow multiple DDC ID rails. Example is provided in following table.

DDC ID	CONFIGURATION	DDC_GROUP	DESCRIPTION
0	3xZL9101M Current Sharing	0000000Ah	This rail will listen to Rail-1 and Rail-3.
1	2xZL9101M Current Sharing	00000004h	This rail will listen to Rail-2.
2	1xZL9101M Single Phase	00000000h	This rail will ignore fault spread.
3	1xZL9101M Single Phase	00000002h	This rail will listen to Rail-1.

The device/rail's own DDC ID should not be set within the DDC_GROUP command for that device/rail.

All devices in a current share rail must shutdown for the rail to report a shutdown.

If fault spread mode is enabled in USER_CONFIG (Bit 8 set to 1), the device will immediately shut down if one of its DDC_GROUP members fail. The device/rail will attempt its configured restart only after all devices/rails within the DDC_GROUP have cleared their faults.

If fault spread mode is disabled in USER_CONFIG (Bit 8 cleared to 0), the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the DDC_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Data Length in Bytes: 4

Data Format: BIT

Type: R/W Block

Default Value: 00000000h (Ignore fault spread)

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASC

Type: Read Block

Default Value: Current firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the table below. Sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the table below. Sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: DA80h (20A)

Units: A

Range: -100A to 25A

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the I_{OUT} average undercurrent fault threshold. For down slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: DD80h (-20A)

Units: A

Range: -100A to 100A

MISC_CONFIG (E9h)

Definition: Sets options pertaining to advanced features.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W Word

Default Value: 0400h

Units: N/A

BITS	PURPOSE	VALUE	DESCRIPTION
15	Broadcast Margin (see DDC_CONFIG)	0	Disabled
		1	Enabled
14	Broadcast Enable (see DDC_CONFIG)	0	Disabled
		1	Enabled
13:12	Reserved	00	Reserved
11:10	I-sense Gain Factor	00	DCR = 25mV
		01	DCR = 35mV
		10	DCR = 50mV
		11	Reserved
9:7	Reserved	000	Reserved
6	Diode Emulation	0	Disabled
		1	Enabled, enter diode emulation at light loads to improve efficiency.
5:2	Reserved	0000	Reserved
1	Snapshot	0	Disabled
		1	Enabled
0	Reserved	0	Reserved

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash either during a fault condition or through a system-defined time using the SNAPSHOT_CONTROL command. In case of a fault, last updated values are stored to the flash memory. Use SNAPSHOT_CONTROL command to read stored values.

Data Length in Bytes: 32

Data Format: BIT

Type: Read Block

BYTE NUMBER	VALUE	PMBUS COMMAND	FORMAT
31:22	Reserved	Reserved	00h
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	External Temperature	READ_TEMPERATURE_2 (8Eh)	L11
11:10	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Peak Current	N/A	L11
5:4	Load Current	READ_IOUT (8Ch)	L11
3:2	VOUT	READ_VOUT (8Bh)	L16u
1:0	VIN	READ_VIN (88h)	L11

BLANK_PARAMS (EBh)

Definition: Returns a 16-byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. Index to read BLANK_PARAM is provided in "PMBus Command Summary" on page 20. One indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Data Length in Bytes: 16

Data Format: BIT

Type: Read Block

Default Value: FF....FFh

PHASE_CONTROL (F0h)

Definition: Controls Phase adding/dropping when the device is setup for current sharing.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

VALUE	DESCRIPTION
00h	The device phase is disabled or dropped
01h	The device phase is active or added

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01 will cause the device to copy the current snapshot values from NVRAM to the 32-byte snapshot parameters. Writing a 02 will cause the device to write the current snapshot values to NVRAM. Read from NVRAM (writing a 01) does not work if SNAPSHOT is enabled in MISC_CONFIG. To read from NVRAM, the device has to be disabled.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

VALUE	DESCRIPTION
01h	Move parametric and status values from Flash to the RAM
02h	Move latest parametric and status values from RAM to the Flash

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hardcoded Factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Data Length in Bytes: 0

Data Format: N/A

Type: Send Byte

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Reads the VDRV OV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: CB80h (7V)

Units: V

Range: 0V to 19V

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Reads the VDRV UV fault threshold

Data Length in Bytes: 2

Data Format: L11

Type: R/W Word

Default Value: CA40h (4.5V)

Units: V

Range: 0V to 19V

MFR_READ_VMON (F7h)

Definition: Reads the VDRV voltage.

Data Length in Bytes: 2

Data Format: L11

Type: Read Word

Default Value: N/A

Units: V

MFR_VMON_OV_FAULT_RESPONSE (F8h)

Definition: Configures the VDRV overvoltage fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

MFR_VMON_UV_FAULT_RESPONSE (F9h)

Definition: Configures the VDRV undervoltage fault response.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W Byte

Default Value: 80h (Disable and no retry)

Units: N/A

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Continuous operation (Ignore fault).
		01	Delay, disable, and retry. Delay time is specified by Bits [2:0] and retry attempt is specified in Bits [5:3].
		10	Disable and retry according to the setting in Bits [5:3].
		11	Output is disabled while the fault is present. Output is enabled when the fault condition no longer exists.
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	The PMBus device attempts to restart the number of times set by these bits. The time between the start is set by the value in Bits [2:0].
		111	Attempts to restart continuously, without checking if the fault is still present, until it is disabled, bias power is removed, or another fault condition causes the unit to shut down.
2:0	Retry and Delay Time	000-111	This time count is used for both the amount of time between retry attempts and for the amount of time a rail is to delay its response after a fault is detected. The retry time and delay time units are defined by the type of fault within each device.

SECURITY_LEVEL (FAh)

Definition: The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writeable (commands are always readable). If a command is not writeable, a password must be entered in order to change its parameter (i.e., to enable writes to that command). There are two types of passwords, public and private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as non-writeable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting Default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as non-writeable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT Store must be sent in order to change that command. If a command is writeable according to the Default UNPROTECT parameter, it may still be marked as non-writeable in the User Store UNPROTECT parameter. In this case, the User private password can be sent to make the command writeable.

The device supports four levels of security. Each level is designed to be used by a particular class of users, ranging from module manufacturers to end users, as discussed below. Levels 0 and 1 correspond to the public password. All other levels require a private password. Writing a private password can only raise the security level. Writing a public password will reset the level down to 0 or 1.

Figure 23 shows the algorithm used by the device to determine if a particular command write is allowed.

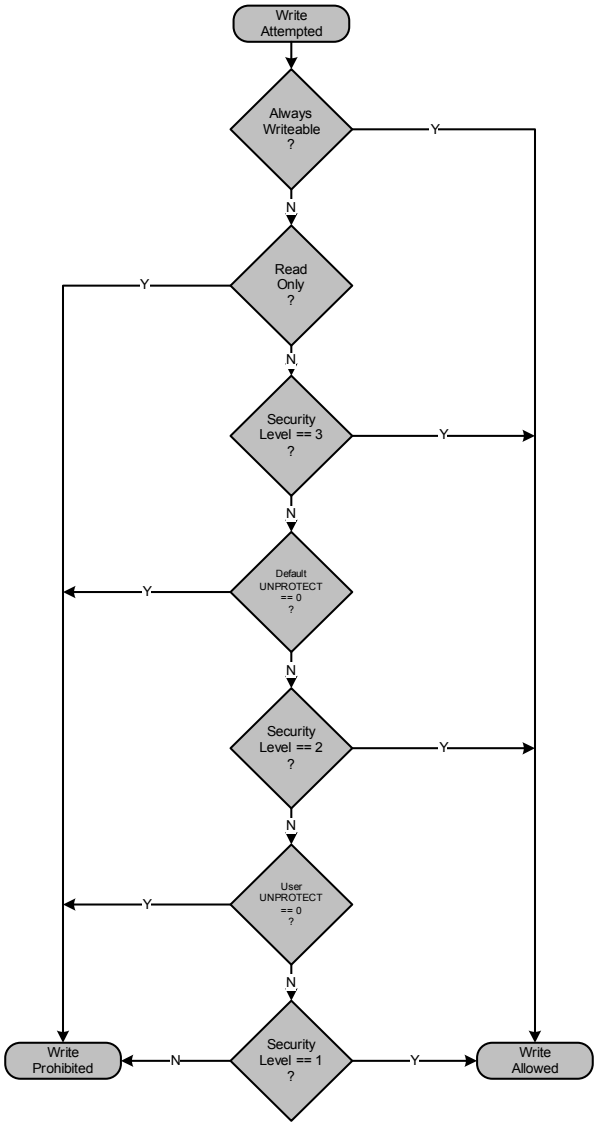


FIGURE 23. ALGORITHM USED TO DETERMINE WHEN A COMMAND IS WRITEABLE

Security Level 3 – Module Vendor

Level 3 is intended primarily for use by Module vendors to protect device configurations in the Default Store. Clearing a UNPROTECT bit in the Default Store implies that a command is writeable only at Level 3 and above. The device's security level is raised to Level 3 by writing the private password value previously stored in the Default Store. To be effective, the module vendor must clear the UNPROTECT bit corresponding to the STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 3 protection is ineffective since the entire store could be replaced by the user, including the enclosed private password.

Security Level 2 – User

Level 2 is intended for use by the end user of the device. Clearing a UNPROTECT bit in the User Store implies that a command is writeable only at Level 2 and above. The device's security level is raised to Level 2 by writing the private password value previously stored in the User Store. To be effective, the user must clear the UNPROTECT bit corresponding to the STORE_USER_ALL, RESTORE_DEFAULT_ALL, STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 2 protection is ineffective since the entire store could be replaced, including the enclosed private password.

Security Level 1 – Public

Level 1 is intended to protect against accidental changes to ordinary commands by providing a global write-enable. It can be used to protect the device from erroneous bus operations. It provides access to commands whose UNPROTECT bit is set in both the Default and User Store. Security is raised to Level 1 by writing the public password stored in the User Store using the PUBLIC_PASSWORD command. The public password stored in the Default Store has no effect.

Security Level 0 - Unprotected

Level 0 implies that only commands which are always writeable (e.g., PUBLIC_PASSWORD) are available. This represents the lowest authority level and hence the most protected state of the device. The level can be reduced to 0 by using PUBLIC_PASSWORD to write any value which does not match the stored public password.

Data Length in Bytes: 1

Data Format: Hex

Type: Read Byte

Default Value: 01h

PRIVATE_PASSWORD (FBh)

Definition: Sets the private password string.

Data Length in Bytes: 9

Data Format: ASCII. ISO/IEC 8859-1

Type: R/W Block

Default Value: 000...00h

PUBLIC_PASSWORD (FCh)

Definition: Sets the public password string.

Data Length in Bytes: 4

Data Format: ASCII. ISO/IEC 8859-1

Type: R/W Block

Default Value: 00...00h

UNPROTECT (FDh)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access at lower security levels. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE) is protected by the least significant bit of the least significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are protected or supported by the device. Clearing a command's UNPROTECT bit indicates that write access to that command is only allowed if the device's security level has been raised to an appropriate level. The UNPROTECT bits in the DEFAULT store require a security level 3 or greater to be writeable. The UNPROTECT bits in the USER store require a security level of 2 or higher.

Data Length in Bytes: 32

Data Format: CUS

Type: Block R/W

Default Value: FF...FFh

Firmware Revision History

FIRMWARE REVISION CODE	CHANGE DESCRIPTION	NOTE
FC04	Initial release	Not recommended for new designs.
FC05	1. Fixed bug: clear VMON_UV_WARNING when VMON (VDRV) voltage is ramped up with a delay of >50ms from VIN 2. Fixed bug: PID Taps in DEFAULT STORE does not work if PID. Taps are stored in USER STORE on issuing RESTORE DEFAULT 3. Fixed bug: added ADC flash trim registers in the calibration table 4. MAX_DUTYB = 91.375% 5. OVUV_CONFIG = 00h 6. FREQUENCY_SWITCH = 571kHz (SYNC pin open) 7. VOUT_OV_FAULT_LIMIT = 1.15 x VOUT_COMMAND 8. VOUT_UV_FAULT_LIMIT = 0.85 x VOUT_COMMAND 9. IOUT_OC_FAULT_LIMIT = 32A 10. IOUT_UC_FAULT_LIMIT = -32A 11. VIN_OV_FAULT_LIMIT = 14.5V 12. VIN_OV_WARN_LIMIT = 13.2V 13. VIN_UV_WARN_LIMIT = 4.375V 14. VIN_UV_FAULT_LIMIT = 4V 15. TON_RISE = 10ms 16. TON_FALL = 10ms 17. AUTO_COMP_CONFIG = 69h 18. MFR_CONFIG = 6A11h 19. USER_CONFIG = 2011h 20. INDUCTOR = 0.22µH 21. TEMPCO_CONFIG = 2Ch 22. DEADTIME = 1018h (H-L = 16ns, L-H = 24ns) 23. DEADTIME_CONFIG = 8686h, freeze deadtimes 24. DEVICE_ID = ZL9101M-002-FC05 25. IOUT_AVG_OC_FAULT_LIMIT = 20A 26. IOUT_AVG_UC_FAULT_LIMIT = -20A 27. MISC_CONFIG = 2400h	Not recommended for new designs.
FC06	Skip	–
FC07	Skip	–
FC08	1. Supporting 14µs ADC settling time for V_{MON} reading. 2. Disable state detection function for the controller's floating pins inside of the module.	Recommended for new designs.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Jun 20, 2017	FN7669.8	Added the last sentence to “PMBus Use Guidelines” on page 24. Updated the definition for “STATUS_CML (7Eh)” on page 39. Changed the range of IOUT_AVG_OC_FAULT_LIMIT from “-100A to 100A” to “-100A to 25A”.
Mar. 16, 2016	FN7669.7	Added “PMBus Use Guidelines” on page 24.
Feb. 3, 2016	FN7669.6	Added part number ZL9101MBIRZ to the ordering information table on page 6. Updated the Firmware information on page 6 and page 59.
Feb. 12, 2015	FN7669.5	Removed AN2033 throughout the datasheet. Figure 1 on page 1: Changed 2x22µF 16 V to CIN and changed 3x47µ to 16 V to COUT. Removed the notes under Figure 1. On page 3, Pin Description, added “A pull-up resistor is required for this application.” For SCL, SDA and DDC. On page 4: Added ZL9101M Internal Block Diagram. On page 5: Added Typical Application- Single Module along with the notes. Ordering Information table on page 6: Added Firmware Revision column and a note. Ordering Information table on page 6: Added part numbers ZL9101MAIRZ and ZL9101EVAL1Z. Electrical spec table on page 7, under Driver Supply Current, IVDRV: Added another row showing the test conditions VDRV = 6V, V_{OUT} = 1.0V, f_{SW} = 571kHz, I_{OUT} = 12A and typical value 30mA. Electrical spec table on page 7, combined “line regulation accuracy” and “load regulation accuracy” into “Output Voltage Accuracy”. Electrical spec table under “Switching Frequency Range” on page 8; changed: the Minimum value from 500 to 400. In “Typical Performance Curves” on page 9, updated figures 2, 3 and 4. On page 12, Switching Frequency and PLL, added text and tables after 1st paragraph. On page 14, added “Output Voltage Tracking” section. On page 17, added “Output Capacitor Selection” section and “Input Capacitor Selection” section. On page 20, added PMBus Command Summary and Description. Updated “Layout Guide” section and figure 21 recommended layout on page 18. On page 59: Added Firmware revision table.
Nov. 23, 2011	FN7669.4	On page 1 1st paragraph - changed the output voltage range from 4V to 3.6V.
Oct. 18, 2011	FN7669.3	On page 1, added 3rd sentence: “This power module has built-in auto-compensation algorithms, which eliminates the need for manual compensation design work.” Under “Features,” added 3rd bullet, “Auto Compensating PID Filter” On page 2, “Pin Descriptions”: add “Connect 4.7µF bypass capacitor to this pin.” to Description column for Pins 8, 11, and 12. On page 5, “Recommended Operating Conditions”: changed “Output Voltage Range, VOUT” from “0.54V to 4V” to “0.54V to 3.6V”; changed “Output Current Range, $I_{OUT(DC)}$” from “0A to 15A” to “0A to 12A”. On page 5, “Electrical Specifications”: - Input Bias Shutdown Current, IDDS EN = 0 V: changed TYP from 9.5 to 15.5; changed MAX from 12 to 20. - Input Supply Current, IVIN: changed Conditions from VIN = 13.2V, IOUT = 15A, VOUT = 1.2V to VIN = 13.2V, IOUT = 12A, VOUT = 1.2V. Changed TYP from 1.5 to 1.32. Removed MAX value of 2. - Driver Supply Current, IVDRV: changed MAX from 220 to 250. - Added new parameter: Output Load Current On page 6, Electrical Specs (cont.) for Switching Frequency Range: changed MIN from 590 to 500, TYP from 615 to 571, MAX from 630 to 1000 kHz. From page 9, “Functional Description” to end of datasheet: replaced content. On page 7: replaced Figures 2, 3, and 4 (efficiency curves). On page 8: replaced Figures 9 & 10 (derating curves); added new Figures 11 and 12 (power loss curves). On page 18: “Package Outline Drawing” “L21.15x15 21 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN) Rev 2, 8/11”: replaced Rev 0, 10/10, with Rev 2, 8/11. Change reason, Rev 1: Updated POD to include two decimal places for dimensions to resolve round off error in alignment of package and recommended land pattern. Change reason, Rev 2: In Bottom View on page 1: Changed 17 x 0.80 To: 16 x0.80. Added in a new width dimension on pin 11 of "1 x 0.76". Global: changed frequency from 615kHz to 571kHz, including in Electrical Spec table, Conditions column for Input Bias Supply Current, IDD; and TYP value for Switching Frequency Range. Changed 17A to 12A throughout.
Mar. 18, 2011	FN7669.2	On page 1 in Figure 1, changed VIN in upper right from “5V to 12V” to “4.5V to 13.2V” In “Recommended Operating Conditions” on page 5: Changed “Input Supply Voltage Range, VIN” from “5V to 13.2V” to “4.5V to 13.2V” Changed “Input Supply for Controller, VDD” from “5V to 13.2V” to “4.5V to 13.2V”

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
Jan. 26, 2011	FN7669.1	On page 5 Electrical Spec Table under Input and Supply Characteristic - Parameter “Input Supply Current, I_{VIN}” conditions column changed from “V_{IN} = 14V, I_{OUT} = 15A, V_{OUT} = 1.2V” to “V_{IN} = 13.2V, I_{OUT} = 15A, V_{OUT} = 1.2V. Under Output Characteristics - Parameter “Line Regulation Accuracy” conditions column changed from “V_{OUT} = 1.2V, I_{OUT} = 0A, V_{IN} = 5V to 14V” to “V_{OUT} = 1.2V, I_{OUT} = 0A, V_{IN} = 5V to 13.2V”. On page 1, under Features, changed “Tracking” to “Output Voltage Tracking” On page 1, Figure 1, added footnote 4. “The VR, V25, VDRV, and VDD capacitors should be placed no further than 0.5 cm from the pin.” On page 5, under “Absolute Maximum Ratings”, changed value: DC Supply Voltage for VDD Pin from 16V to 15.7V On page 5, under “Absolute Maximum Ratings”, changed value: Input Voltage for VIN Pin from 16V to 15.7V On page 5, under Recommended Operating Conditions, changed value: Input Supply Voltage Range, Vin from 14V to 13.2V On page 5, under Recommended Operating Conditions, changed value: Input Supply For Controller, VDD from 14V to 13.2V. On page 6, Note 11, changed “... for internal IC prior ...” to “... for internal controller prior ...” On page 7, Figure 7, changed title from “Ramp-up” to “Soft-start Ramp-up”. On page 8, Figure 9, changed labels to from V to V_{OUT} (e.g. $3.3V_{OUT}$, $1.0V_{OUT}$) On page 8, Figure 10, changed labels to from V to V_{OUT} (e.g. $3.3V_{OUT}$, $1.0V_{OUT}$)
Dec. 20, 2010	FN7669.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

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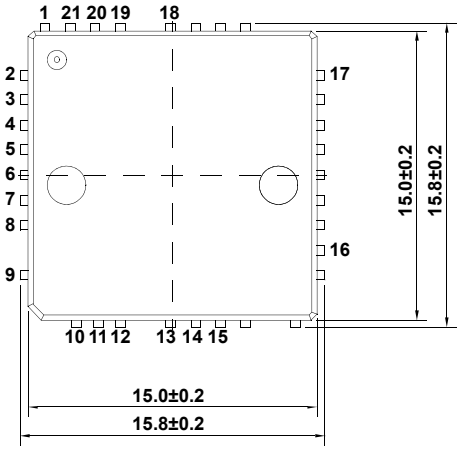
Package Outline Drawing

L21.15x15

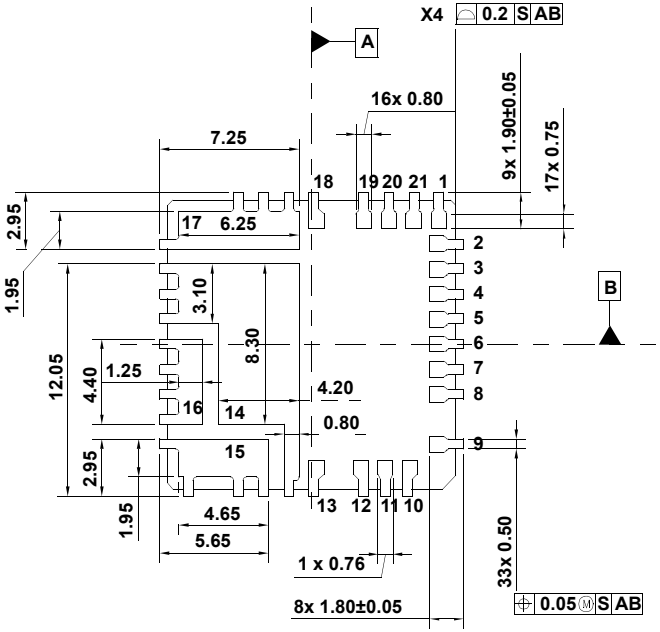
21 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

Rev 2, 8/11

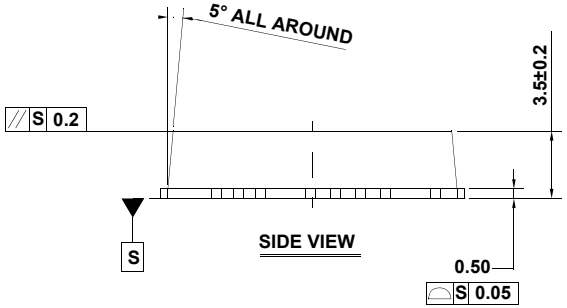
For the most recent package outline drawing, see L21.15x15.



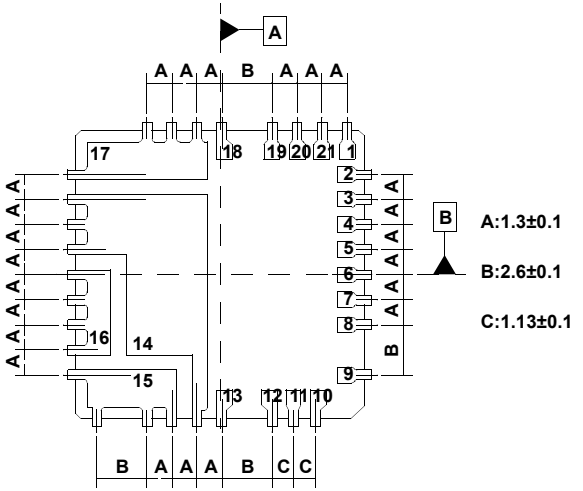
TOP VIEW

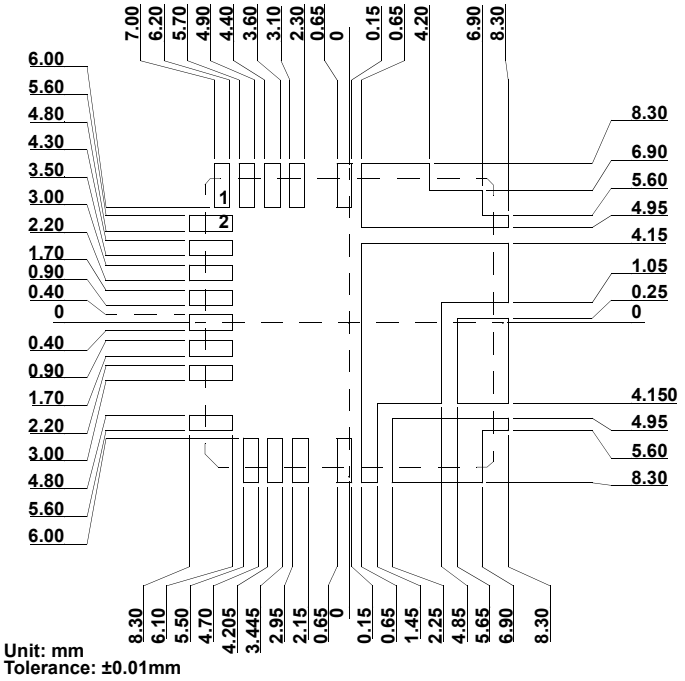


BOTTOM VIEW



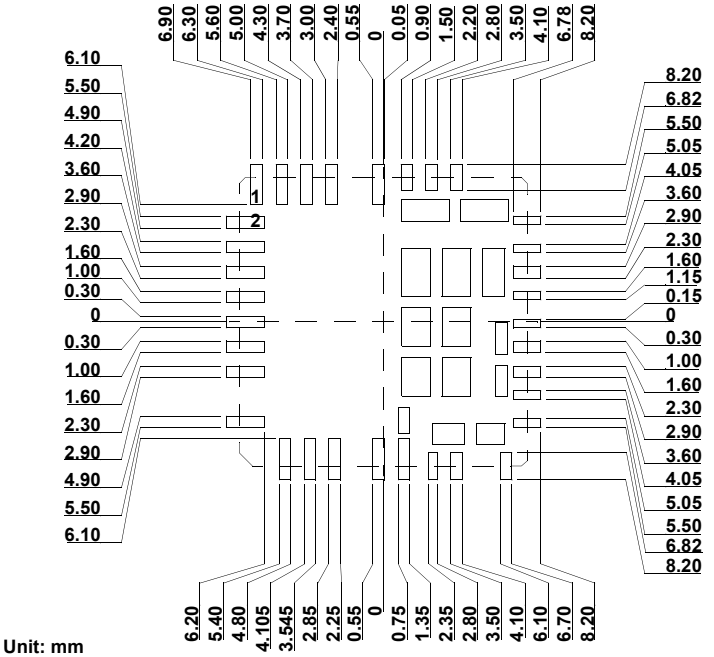
SIDE VIEW





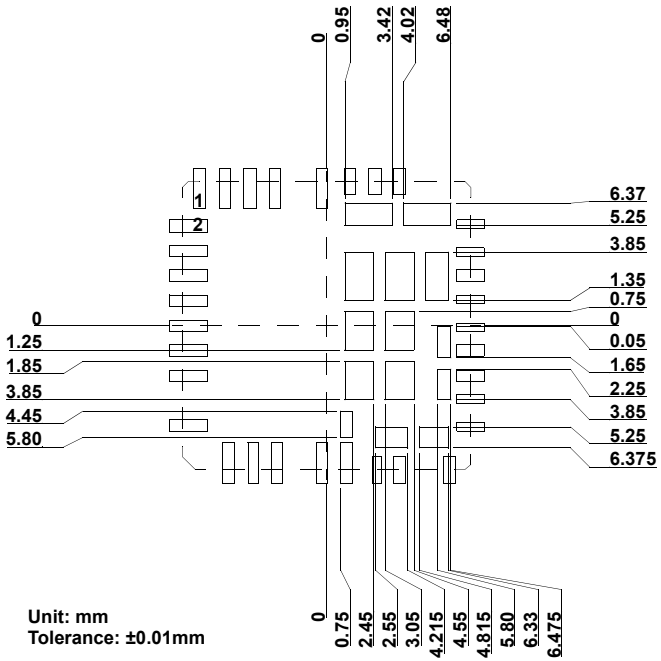
Unit: mm
Tolerance: ±0.01mm

TYPICAL RECOMMENDED LAND PATTERN



Unit: mm
Tolerance: ±0.01mm

STENCIL PATTERN WITH SQUARE PADS-1



Unit: mm
Tolerance: ±0.01mm

STENCIL PATTERN WITH SQUARE PADS-2

NOTES:

1. Dimensions are in millimeters.
2. Unless otherwise specified, tolerance : Decimal ± 0.2;
   Body Tolerance ±0.2mm
3. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.