Dual PowerPath Switch Driver

DESCRIPTION

Demonstration circuit DC145 is a protected dual PowerPath™ switch that routes two power sources into one output. This circuit is designed for low loss switching at the "front end" of a power management system, where two power sources need to be connected or disconnected from the load. Applications include notebook and palmtop computers and other portable systems requiring low loss switching of multiple power sources.

The dual PowerPath switch is formed by two sets of back-to-back N-channel MOSFET switches. One end of each switch is tied to the output while the other two ends are tied to each power source. The PowerPath switches can be controlled with three external TTL/CMOS level signals into an LTC®1473 driving the MOSFET switches.

PERFORMANCE SUMMARY

SYMBOL	PARAMETER	CONDITIONS	VALUE
V_{BAT1}, V_{BAT2}	BAT1, BAT2 Supply Range (Note 1)		4.2V to 24V
I_Q	Supply Current	IN1 = 3V, IN2 = 0V, $\overline{DIODE}$ = Floating	130µA
IN1, IN2	Input Threshold Voltage		1.4V
$\overline{DIODE}$	Input Threshold Voltage		1.4V
I_{LIMIT}	Inrush and Short-Circuit Current Limit	OUT = 0V, IN1 = 3V, IN2 = 0V, $\overline{DIODE}$ = Floating	6A
t_{FAULT}	Fault Timer Delay	OUT = 0V, IN1 = 3V, IN2 = 0V, $\overline{DIODE}$ = Floating	1.1ms
R_{PP}	PowerPath Resistance	Resistance from BAT1 (or BAT2) to OUT	0.1Ω
I_{RMS}	Maximum RMS PowerPath Current	BAT1 (or BAT2) = 24V	3A
$C_{OUT(MAX)}$	Maximum OUT Capacitance (Note 2)		100µF

Note 1: BAT1, BAT2 supply range is limited by the Si4936DY safe operating area. See the Operation section for more information.

Note 2: $C_{OUT(MAX)}$ on the DC145 is limited by the value of the timer capacitor C6. See the Operation section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

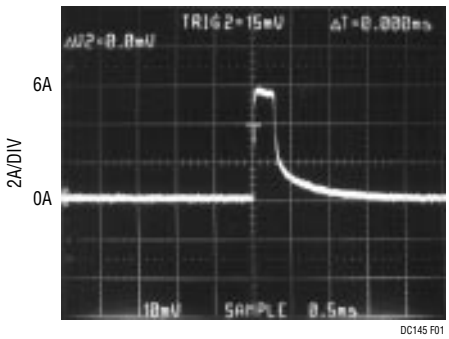


Figure 1. Inrush Current from a 24V Battery into a 100µF Capacitor

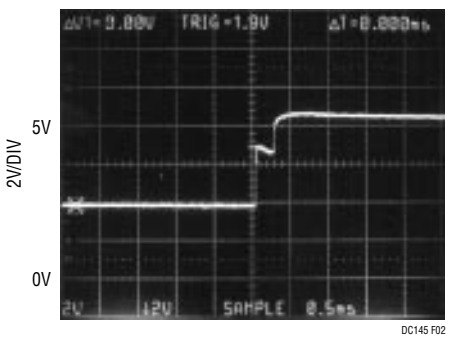
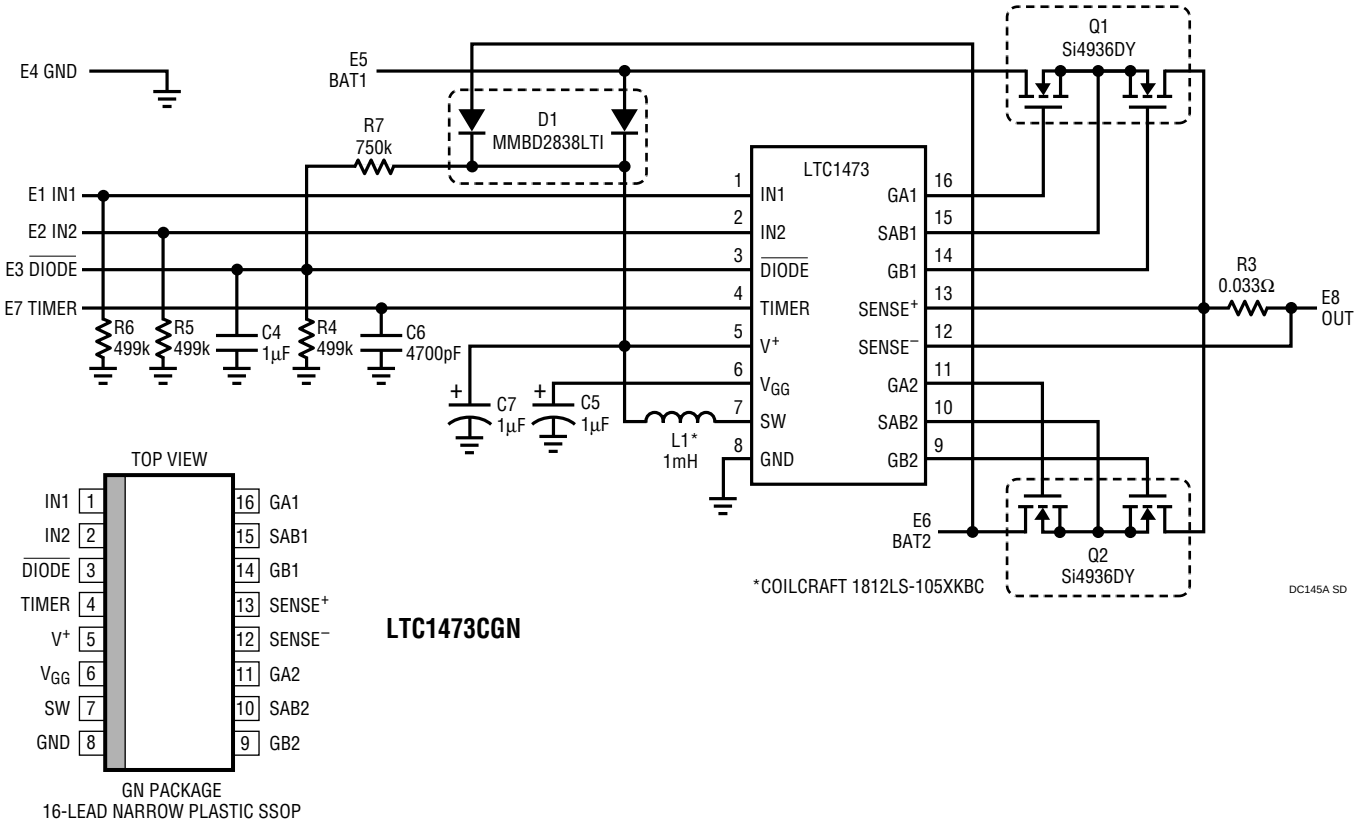


Figure 2. V_{GS} of N-Channel MOSFET Switch Being Turned On

Dual PowerPath Switch Driver Demo Board

PACKAGE A ND SCHEMATIC DIAGRAMS



LTC1473CGN

Figure 3. LTC1473 Dual PowerPath Switch Driver

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C4, C5, C7	3	18125C105MATMA	1µF 50V X7R 20% Chip Capacitor	AVX	(803) 946-0362
C6	1	08055C472KATMA	4700pF 50V X7R 10% Chip Capacitor	AVX	(803) 946-0362
D1	1	MMBD2838LT1	Dual Diode (SOT-23)	Motorola	(602) 244-3576
L1	1	1812LS-105XKBC	1000µH Chip Inductor	Coilcraft	(847) 639-6400
Q1, Q2	2	Si4936DY	4.7A 30V Dual N-Channel MOSFET (SO-8)	Siliconix	(408) 567-8151
R3	1	LR2512-01-R033-J	0.033Ω 1W 5% Chip Resistor	IRC	(512) 992-7900
R4 to R6	3	CR10-4993FT	499k 1/8W 1% Chip Resistor	TAD	(800) 508-1521
R7	1	CR10-7503FT	750k 1/8W 1% Chip Resistor	TAD	(800) 508-1521
U1	1	LTC1473CG	Dual PowerPath Switch Driver	LTC	(408) 432-1900

INTRODUCTION

A protected dual PowerPath switch is implemented using the LTC1473. Figure 3 is the schematic for this demonstration board. The PowerPath switch can be used at the "front end" of a power management system where two power sources need to be connected or disconnected from the load.

Small spring-clip leads are very convenient for small-signal bench testing and voltage measurements, but they should not be used with the high currents associated with this circuit. Soldered wire connections are required in the PowerPath pins (E4 to E6 and E8). If E8 connects to a large bypass capacitor, this capacitor should be soldered to the demonstration board.

This demonstration board is intended for the evaluation of the LTC1473 dual N-channel switch driver and was not designed for any other purpose.

QUICK START GUIDE

Demonstration board DC145 is easily set up for evaluation of the LTC1473 IC. Please follow the procedure outlined below for error-free operation.

- For optimum results, solder a 10µF electrolytic capacitor across terminals BAT1 (E5) and GND (E4). Repeat for terminals BAT2 (E6) and GND (E4).
- Connect the first battery or power supply to BAT1 (E5) and GND (E4) terminals. Do not exceed 24V or the MOSFET(s) may be damaged.
- Connect the second battery or power supply to BAT2 (E6) and GND (E4) terminals. As above, do not exceed 24V.
- Connect the driving signals into IN1 (E1) and IN2 (E2). Taking IN1 high and IN2 low connects BAT1 to OUT (E8). Taking IN1 low and IN2 high connects BAT2 to OUT. When both inputs are either high or low, all the MOSFET switches are off. Both inputs have a 499k resistor pull-down to ground and accept TTL/CMOS compatible level signals.
- Allow $\overline{\text{DIODE}}$ (E3) and TIMER (E7) to float.
- Connect the output load to OUT (E8). Typically, the output "load" is the V_{IN} of a switching regulator. The V_{IN} bypass capacitor must be very close to OUT (E8). Solder the V_{IN} bypass capacitor to the demo board if possible. If not, solder a 10µF capacitor across OUT (E8) and GND (E4).

OPERATION

The PowerPath switches are implemented with 8-lead surface mounted N-channel MOSFET(s). These MOSFET(s) from Siliconix (Si4936DY) have an $R_{DS(ON)}$ of 0.040Ω and maximum allowable drain-source voltage ($V_{DS(MAX)}$) of 30V. A number of similar N-channel MOSFET(s), available from different manufacturers, are well suited for this type of application. As a general rule, select the switch with the lowest $R_{DS(ON)}$ at the maximum allowable V_{DS}. This will minimize the heat dissipated in the switches while increasing the overall system efficiency.

The V^+ pin of the LTC1473 is supplied by BAT1 (E5) or BAT2 (E6) through two OR-connected diodes. When both power supplies are present at BAT1 and BAT2, the one with the highest potential flows to the LTC1473.

The gate drive for the low loss N-channel switches is supplied by a micropower boost regulator, which regulates at approximately 8.5V above V^+ (up to 37V maximum). The boosted voltage, V_{GG}, can supply about 300μA to 400μA, which is enough to allow a second LTC1473 to share V_{GG} with the first one. In this configuration, the one boosting the voltage must have at least the same or higher V^+ of the two LTC1473s.

A 0.033Ω sense resistor (R3) limits the inrush current to 6A. The LTC1473's bidirectional current sensing and limiting circuit determines when the voltage drop across R3 reaches ±200mV. The gate-to-source voltage, V_{GS}, of the appropriate switch is limited during the transition period (see Figure 2) until the inrush current subsides, generally within a few hundred microseconds for capacitor values ≤100μF at OUT (E8).

The value of timer capacitor C6 must be chosen so that the fault timer does not time out during a normal inrush event. C6 = 4700pF programs the fault timer to 1.1ms. In the event of a short at OUT (E8), the LTC1473's current limit loop limits the inrush of current into the short for 1.1ms, after which the MOSFET switches are latched off, protecting them from overdissipation. To reset the latch, deselect the gate drive input IN1 (E1) or IN2 (E2). C6 can be monitored by placing a scope probe on TIMER (E7).

The gate-drive inputs, IN1 (E1) and IN2 (E2), control the gates of the MOSFET switches via the LTC1473. These inputs each have a 499k resistor pull-down to ground and accept TTL/CMOS compatible level signals. The gate drives are noninverting, that is, taking IN1 high and IN2 low connects BAT1 to OUT (E8). Conversely, taking IN1 low and IN2 high connects BAT2 to OUT. When both inputs are either high or low, all the MOSFET switches are off.

A third gate drive input, $\overline{\text{DIODE}}$ (E3), overrides IN1 and IN2. Taking $\overline{\text{DIODE}}$ low turns the two MOSFET switches into two virtual diodes. In this "2-diode" mode, the first half of each PowerPath switch pair is turned on and the second half is turned off. The two diodes are formed by the body diodes of the MOSFET switches that are turned off. The direction of the two diodes allows power to flow from whichever of BAT1 or BAT2 has the higher potential to OUT. A resistor divider pulls up $\overline{\text{DIODE}}$ to 2/5 of V^+. Thus, when $\overline{\text{DIODE}}$ is allowed to float, it defaults to high and does not interfere with the normal operation of the gate-drive inputs, IN1 and IN2. A 1μF capacitor (C4) on $\overline{\text{DIODE}}$ slows its rise and fall time with a time constant of 300ms. This ensures that the "2-diode" mode is selected for at least a few milliseconds after power is plugged in, and allows power to flow to OUT (E8), regardless of the states of IN1 and IN2.

Although the LTC1473 and the Si4936DY have ≥30V maximum supply ratings, the maximum supply for this demo board is 24V. This limitation is due to the power dissipation rating of the Si4936DY when in current limit. When OUT is shorted to ground, the energy dissipated by the Si4936DY is given by ($I \bullet V \bullet t_{FAULT}$), where I = 200mV/R3 = 6A, t_{FAULT} = (C6 • 1.2V)/5μA = 1.1ms and V = BAT1 or BAT2. If a supply voltage greater than 24V but less than 28V is desired, I or t_{FAULT} in the equation can be decreased. To decrease I, R3 can be increased; to decrease t_{FAULT}, C6 can be decreased. Decreasing the values of either I or t_{FAULT} will decrease $C_{OUT(MAX)}$, the maximum capacitance value that can be connected at OUT. I and $C_{OUT(MAX)}$ determine the maximum transition time given by $t_{SW(MAX)} = (V \bullet C_{OUT})/I$, which should be about 1/3 or less than the

OPERATION

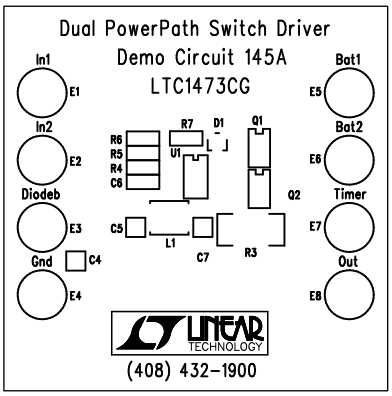
fault timer delay, t_{FAULT}. With t_{FAULT} = 1.1ms and I = 6A, the circuit on this demonstration board is designed for use with $C_{OUT} \leq 100\mu F$. Charging C_{OUT} to 24V from 0V with I = 6A takes 0.4ms which is about 1/3 of t_{FAULT}.

If a C_{OUT} >100µF is needed, C6 must be replaced with a larger value capacitor. This increases the fault timer delay to allow more time for C_{OUT} to charge without tripping the protection circuit. However, the supply voltage must also be reduced or larger power MOSFETs used due to the increased energy dissipation on the Si4936DY if OUT is shorted to ground.

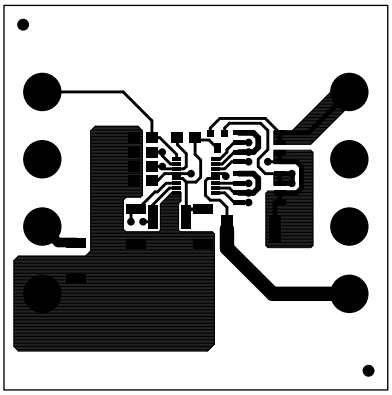
If either C_{OUT} or the supply voltage must be greater than the maximum values specified for this demonstration board, the two Si4936DYs can be replaced with four Si4410DY single N-channel MOSFETs. These MOSFETs, because of a larger die size, have half the R_{DSON} of the Si4936DY and can safely dissipate twice the energy.

See the LTC1473 data sheet for more information on external component selection.

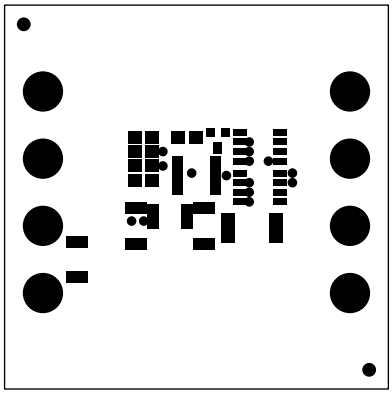
PCB LAYOUT AND FILM



Component Side Silkscreen

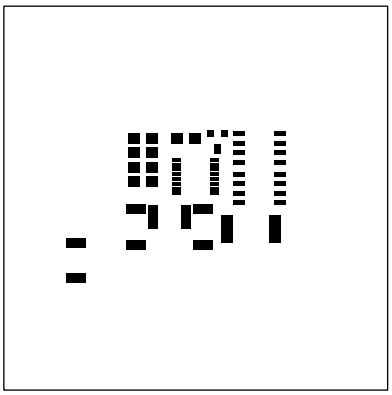


Component Side

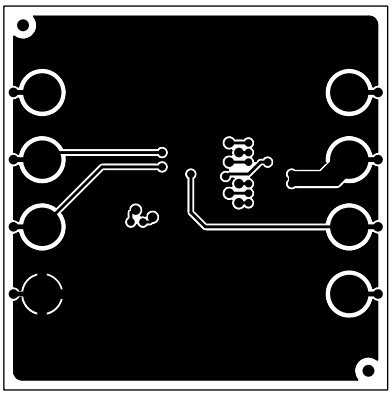


Component Side Solder Mask

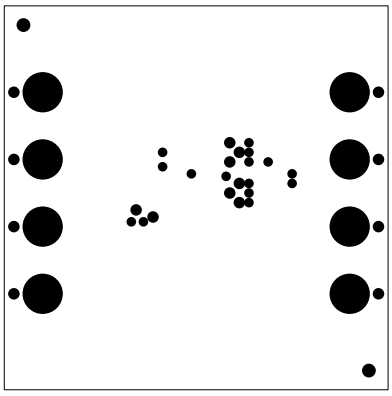
PCB LAYOUT AND FILM



Component Side Pastmask

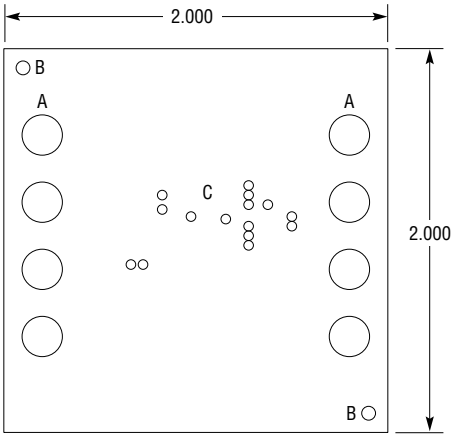


Solder Side



Solder Side Solder Mask

PC FAB DRAWING



NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIAL: FR4 OR EQUIVALENT EPOXY,
   2 OZ COPPER CLAD, THICKNESS 0.062 ±0.006
   TOTAL OF 2 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015 MAX
   COPPER PLATE, ELECTRODEPOSITED TIN-LEAD COMPOSITION
   BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING SR1020 OR EQUIVALENT
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. ALL DIMENSIONS ARE IN INCHES

SYMBOL	DIAMETER	NUMBER OF HOLES
A	0.95	8
B	0.72	2
C	0.20	15
	TOTAL HOLES	25

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