MIC24066/7

36V, 6A High Performance Switching Buck Regulators

Features

- Input Voltage Range: 4.5V to 36V
- Adjustable Output from 0.6V to 32V (also limited by Duty Cycle)
- High Current Capability of 6A for MIC24066/7
- Adaptive Constant On Time Control
- 0.6V Internal Reference with ±1% Accuracy
- Up to 800 kHz Switching Frequency
- High Voltage Internal LDO for Single Supply Operation
- Secondary LDO to Improve System Efficiency
- Supports Start-up to Pre-bias Output
- Internal Compensator for Tight Output Regulation
- Enable Function for Low Stand-by Current
- Programmable HLL/CCM Operation (**MIC24067**)
- Programmable Soft Start Time (**MIC24066**)
- Programmable Current Limit and Hiccup Short Circuit Protection
- Thermal Shut Down with Hysteresis
- Compact Size: 5 mm x 6 mm 36-Pin Wettable Flank VQFN
- -40°C to +125°C Junction Temperature Ranges

Applications

- Servers and Workstations
- Routers, Switches and Telecom Equipment
- Base Stations
- High Power Density Point-of-Load Conversion

General Description

The MIC24066/7 is a family of commercial 36V synchronous switching regulators delivering 6A of load current.

The MIC24066/7 are wide input range (4.5V-36V) integrated FET switching regulator which supports 6A load. These devices have an enhanced high voltage COT controller co-packaged with a pair of N-Channel FETS with improved avalanche rating.

The output voltage is adjustable down to 0.6V with ±1% accuracy. The Hyper Speed Control® proprietary architecture allows for ultra-fast transient response while reducing the output capacitance.

These devices feature programmable switching frequency from 270 kHz to 800 kHz. The operating mode under light load conditions can be selected between HyperLight Load® (HLL) mode and Continuous Conduction Mode (CCM) in MIC24067. HLL mode results in higher efficiency than that of the CCM mode under light load conditions while the CCM mode keeps the switching frequency almost constant over the entire load current range. The enable pin (EN) allows user to enable/disable the device operation. The secondary LDO (powered by EXTVDD) allows user to operate the system at increased efficiency by supplying the device bias power from the output of the switching regulator.

An open drain PGOOD pin provides a power good signal to indicate output voltage is within ±10% of the target level.

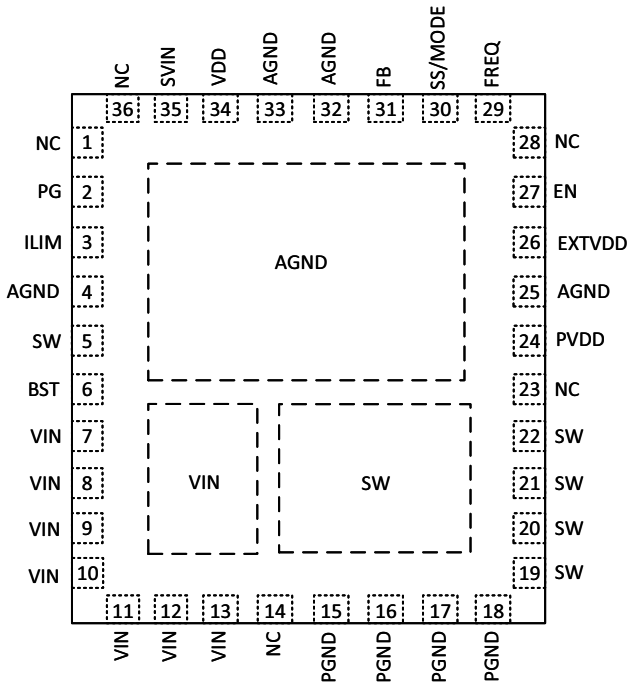
These devices offer a full suite of protection features to ensure safe operation of the IC during fault conditions. These include UVLO, hiccup current limit short circuit protection and thermal shutdown.

These devices are available in a 36-pin 5 mm x 6 mm, Wettable Flank VQFN with a junction operating range from -40°C to +125°C.

Package Type

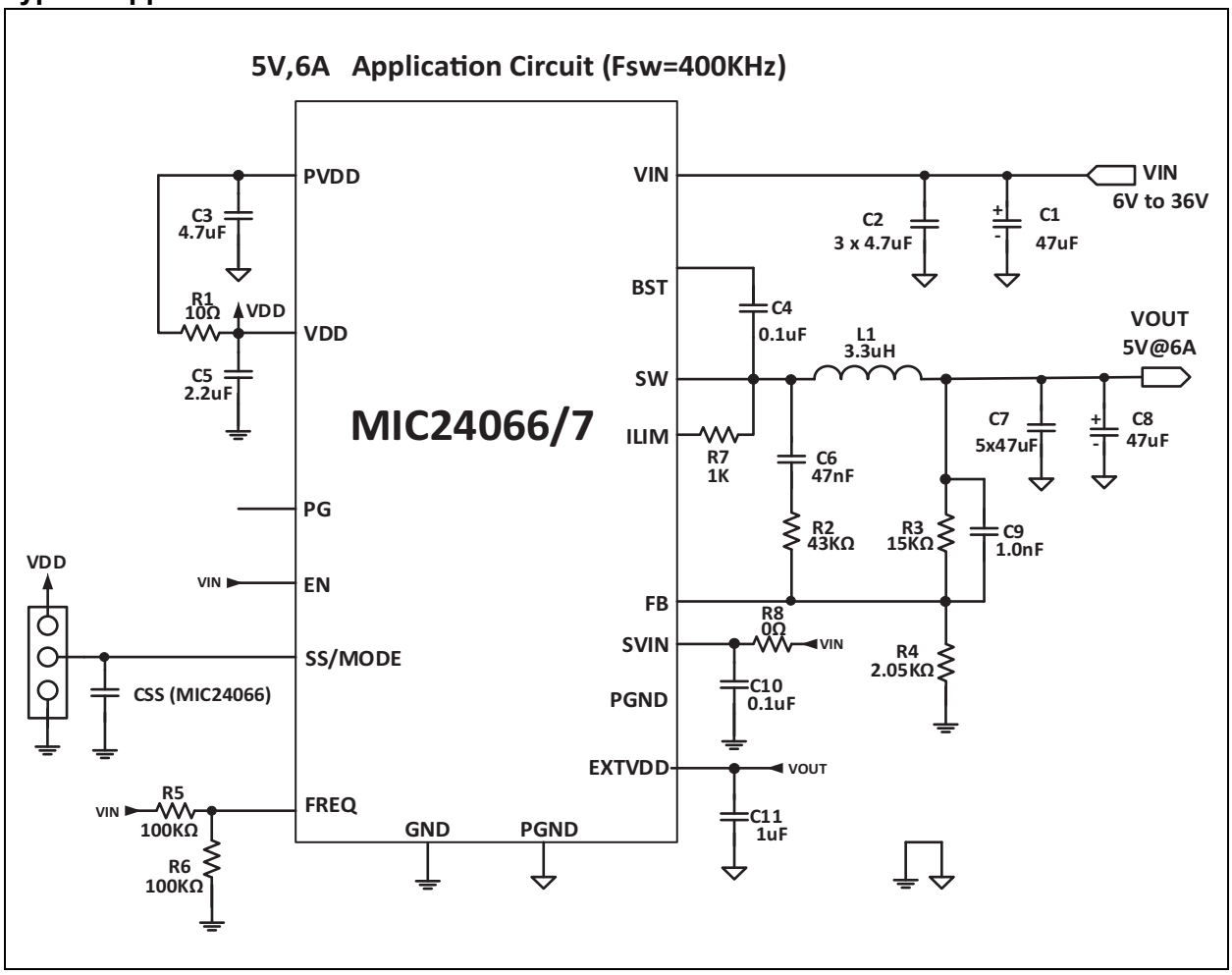
MIC24066/7

36-Pin 5 mm x 6 mm VQFN*

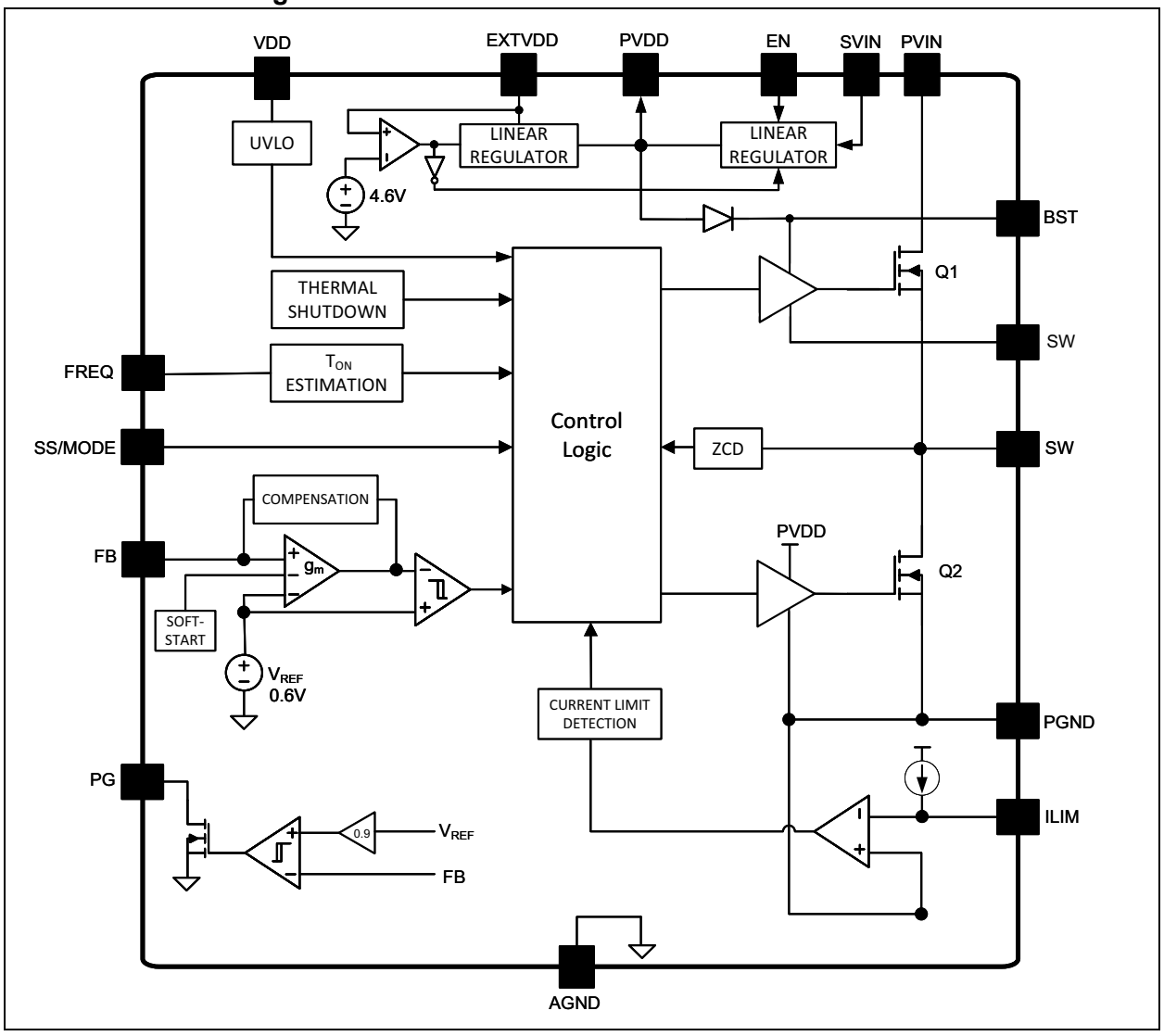


*Includes Exposed Thermal Pads (AGND, VIN & SW); see Table 3-1.

Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†(1)

SV_{IN}, P_{VIN} to PGND ..... -0.3V to +45V
V_{DD} to PGND ..... -0.3V to +6V
PV_{DD} to PGND ..... -0.3V to +6V
FREQ, ILIM, EN to PGND ..... -0.3V to (V_{IN} +0.3V)
SW to PGND ..... -0.3V to (V_{IN} +0.3V)
BST to SW ..... -0.3V to +12V
SS/MODE, FB, PG, to PGND ..... -0.3V to (V_{DD} + 0.3V)
EXTVDD to AGND ..... -0.3V to +14V
PGND to AGND ..... -0.3V to +0.3V
Maximum Junction Temperature (T_J) ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Temperature (T_{LEAD}) ..... +300°C
ESD Rating(2)(HBM) ..... ±1500V
ESD Rating (2)(CDM) ..... ±1500V

Operating Ratings‡

Supply Voltage (SV_{IN}, P_{VIN}) ..... 4.5V to 36V
PV_{DD}, V_{DD} Pin Voltage ..... 4.3V to 5.5V
SS/MODE, PG Pin Voltage ..... 0V to V_{DD}
EXTVDD Pin Voltage ..... 0V to 12V
ILIM, FREQ, SW, EN ..... 0V to V_{IN}
Junction Temperature(3) (T_J) ..... -40°C to +125°C

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Exceeding the absolute maximum rating may damage the device.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

3: The device is not guaranteed to function outside operating range.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: PV_{IN} = SV_{IN} = 12V, V_{OUT} = 1.2V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate 40°C ≤ TJ ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
PVIN, SVIN Voltage Range	V_{IN}	**4.5**	—	**36**	V	
Quiescent Supply Current	I_Q	—	300	**600**	µA	V_{FBS} = +1.5V, MODE = GND
		—	1.4	**1.8**	mA	V_{FBS} = +1.5V, No Switching
Shut Down Current	I_{SD}	—	5	**10**	µA	Power from VIN, V_{EN} = 0V
		—	30	**50**	µA	V_{IN} = V_{DD} = 5.5V, V_{EN} = 0V
PV_{DD} and $EXTV_{DD}$						
PV_{DD} Output Voltage Range	V_{DD}	**4.8**	5.1	**5.4**	V	SV_{IN} = 7V to 36V, IPV_{DD} < = 10 mA
V_{DD} Undervoltage Lockout Upper Threshold	V_{DDUV_R}	3.7	4.2	4.5	V	V_{DD} rising
V_{DD} UVLO Hysteresis	V_{DDUV_HYS}	—	600	—	mV	Hysteresis
V_{DD} Regulation	ΔV_{DD}	—	1	**2.5**	%	V_{IN} = 24V, I_{VDD} from 1 mA to 40 mA (**Note 5**)
V_{DD} Regulator Dropout Voltage	V_{DROP_VDD}	**0.7**	—	1.25	V	SV_{IN} = 5.5V, I_{PVDD} = 25 mA
EXTVDD Switchover Voltage	V_{SO_EXTVDD}	**4.4**	4.6	**4.8**	V	EXTVDD rising
EXTVDD Switchover Voltage Hysteresis	V_{SO_HYS}	—	200	—	mV	Hysteresis
EXTVDD Dropout Voltage	V_{DROP_EXTVDD}	—	250	—	mV	V_{EXTVDD} = 5V, I_{PVDD} = 25 mA
EXTVDD Leakage Current	I_{LK_EXTVDD}	—	0.1	—	µA	V_{EXTVDD} = 14V, V_{EN} = 0V
Soft Start						
Soft Start Period	t_{SS}	—	5	—	ms	Fixed internal SS (MIC24067)
Soft Start Source Current	I_{SS}	**0.8**	1.3	**3**	µA	Programmable SS (MIC24066)
Reference						
Feedback Regulation Voltage	V_{FB}	0.597	0.6	0.603	V	T_J = 25ºC
		0.594	—	**0.606**		-40ºC ≤ T_J ≤ +125ºC
FBS Bias Current	I_{FBS}	—	50	**500**	nA	V_{FBS} = +0.6V
Enable						
Enable Threshold Voltage High	V_{EN_THH}	**1.6**	—	—	V	Enable rising
Enable Threshold Voltage Low	V_{EN_THL}	—	—	**0.6**	V	Enable falling
Enable Hysteresis	V_{EN_HYS}	—	150	—	mV	
Enable Bias Current	I_{EN}	—	6	**30**	µA	V_{EN} = 12V
MODE (MIC24067)						

Note 1: Exceeding the absolute maximum rating may damage the device.

2: Devices are ESD Sensitive. Handling precautions recommended. Human body model: 1.5 kΩ in series with 100 pF.

3: The device is not guaranteed to function outside its operating range.

4: $P_{D(MAX)}$ = ($T_{J(MAX)}$ - T_A) /θ_{JA}, where θ_{JA} depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62", FR-4 PCB with 2 oz finish copper weight per layer is used for the θ_{JA}.

5: Measured in test mode.

6: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 300 ns.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: PV_{IN} = SV_{IN} = 12V, V_{OUT} = 1.2V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate 40°C ≤ TJ ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
MODE Threshold Voltage High	V_{MODE_THH}	**1.6**	—	—		MODE rising
MODE Threshold Voltage Low	V_{MODE_THH}	—	—	**0.6**		MODE falling
MODE Hysteresis	V_{MODE_HYS}	—	150	—		V_{EN} = 12V
On Timer						
Maximum Switching Frequency	f_{SW_max}	**720**	800	**880**	kHz	V_{VIN} = 12V, V_{FREQ} = V_{VIN} R5 = 100k Ω; R6 = Open
Minimum Switching Frequency	f_{SW_MIN}	**230**	270	**300**	kHz	V_{IN} = 12V, V_{FREQ} = 33% × V_{VIN} R5 = 100k Ω; R6 = 50k Ω
Maximum Switching Frequency	f_{SW_max}	—	800	—	kHz	V_{IN} = 12V, V_{OUTS} = 5V
Minimum On-Time	T_{ONMIN}	—	60	—	ns	Measured in application
Minimum Off-Time	T_{OFFMIN}	**100**	200	**300**	ns	V_{FBS} = 0V
Maximum Duty Cycle	D_{MAX}	—	85	—	%	f_{SW} = 400 kHz, R5 = R6 = 100k Ω
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{FBS} = +1V
Current Limit						
Current-Limit Comparator Offset	V_{OFFSET}	**-15**	0	**15**	mV	V_{FB} = 0.59V
I_{LIM} Source Current	I_{CL}	—	115	—	µA	T_J= 25°C
		80	**—**	**180**	µA	T_J= -140°C to 125°C
I_{LIM} Source Current Tempco	TC_{ICL}	—	0.3	—	µA/°C	
Negative Current Limit Comparator Threshold	—	—	48	—	mV	
Internal MOSFET Parameters						
High Side MOSFET On-Resistance	R_{DSON_HS}	—	22	—	mΩ	
Low Side MOSFET On-Resistance	R_{DSON_LS}	—	8.5	—	mΩ	
SW, VIN and BST Leakage						
BST Leakage	$I_{LEAK(BST)}$	—	—	5	µA	V_{IN} = 45V
VIN Leakage	$I_{LEAK(VIN)}$	—	—	5		V_{IN} = 45V
SW Leakage	$I_{LEAK(SW)}$	—	—	5		V_{IN} = 45V
Power Good (PG)						
PG Threshold from Low to High	V_{PG_TH}	**85**	90	**95**	%V_{REF}	V_{FB} rising
PG Threshold Hysteresis	V_{PG_HYS}	—	6	—	%V_{REF}	V_{FB} falling
PG Delay	t_{D_PG}	—	100	—	µs	V_{FB} rising

Note 1: Exceeding the absolute maximum rating may damage the device.

2: Devices are ESD Sensitive. Handling precautions recommended. Human body model: 1.5 kΩ in series with 100 pF.

3: The device is not guaranteed to function outside its operating range.

4: $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62", FR-4 PCB with 2 oz finish copper weight per layer is used for the θ_{JA}.

5: Measured in test mode.

6: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 300 ns.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: PV_{IN} = SV_{IN} = 12V, V_{OUT} = 1.2V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate 40°C ≤ TJ ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
PG Low State Voltage	V_{PG_L}	—	70	**200**	mV	V_{FB} < 90% × V_{NOM}, I_{PG} = 1 mA
PG Leakage Current	$I_{LEAK(PG)}$	—	—	**100**	nA	V_{PG} = 5.5V
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	**—**	160	**—**	°C	T_J rising
Thermal Shutdown Hysteresis	T_{SD_HYS}	**—**	20	**—**	°C	

Note 1: Exceeding the absolute maximum rating may damage the device.

2: Devices are ESD Sensitive. Handling precautions recommended. Human body model: 1.5 kΩ in series with 100 pF.

3: The device is not guaranteed to function outside its operating range.

4: $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62", FR-4 PCB with 2 oz finish copper weight per layer is used for the θ_{JA}.

5: Measured in test mode.

6: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 300 ns.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+125	°C	**Note 1**
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	+150	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Lead Temperature	T_{LEAD}	—	—	+300	°C	Soldering, 10s
Package Thermal Resistance						
Thermal Resistance, 5 mm x 6 mm, 36-Lead VQFN	θ_{JB}	—	10.2	—	°C/W	Junction to Board
	$\theta_{JC(Top)}$	—	31.2	—	°C/W	Junction to Case (Top)
	θ_{JA}	—	33.7	—	°C/W	Junction to Ambient
	Ψ_{JT}	—	11.1	—	°C/W	Junction to Top
	Ψ_{JB}	—	11.8	—	°C/W	Junction to Bot

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C. Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

Power components for different outputs used for following Performance Curves

V_{OUT} Config	C_{INJ}	R_{INJ}	R_{BOT}	R_{TOP}	C_{FF}	L	C_{SNB}	R_{SNB}
1V	43 kΩ	47 nF	12.1 kΩ	8.06 kΩ	2.2 nF	1.15 µH	220 pF	1.2Ω
2.5V	43 kΩ	47 nF	2.05 kΩ	6.49 kΩ	2.2 nF	3.3 µH	220 pF	1.2Ω
3.3V	43 kΩ	47 nF	2.05 kΩ	9.31 kΩ	2.2 nF	3.3 µH	220 pF	1.2Ω
5V	43 kΩ	47 nF	2.05 kΩ	15 kΩ	1 nF	3.3 µH	220 pF	1.2Ω

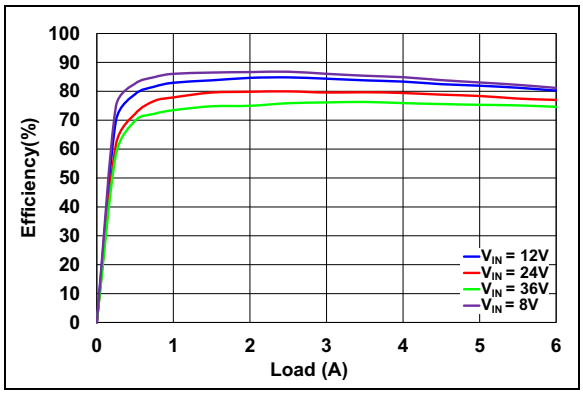


FIGURE 2-1: *Efficiency (V_{OUT} = 1V) vs. Output Current @ 400 kHz (CCM Mode).*

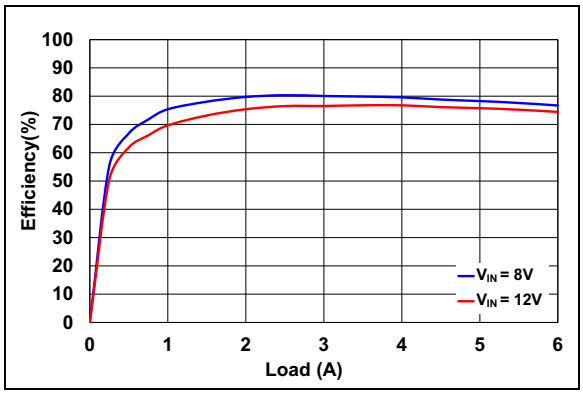


FIGURE 2-3: *Efficiency (V_{OUT} = 1V) vs. Output Current @ 800 kHz (CCM Mode).*

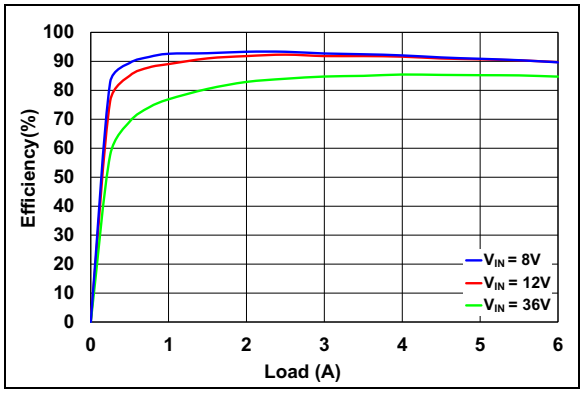


FIGURE 2-2: *Efficiency (V_{OUT} = 2.5V) vs. Output Current @ 400 kHz (CCM Mode).*

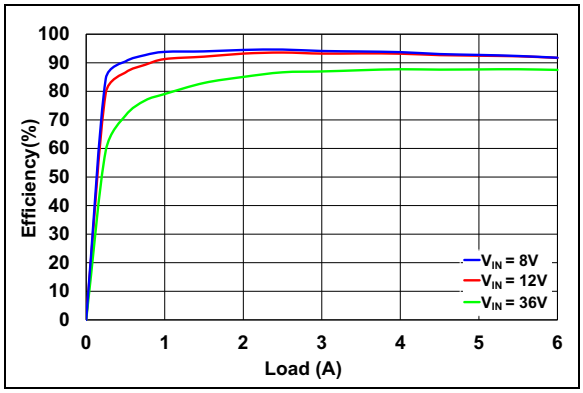


FIGURE 2-4: *Efficiency (V_{OUT} = 3.3V) vs. Output Current @ 400 kHz (CCM Mode).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C.
Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

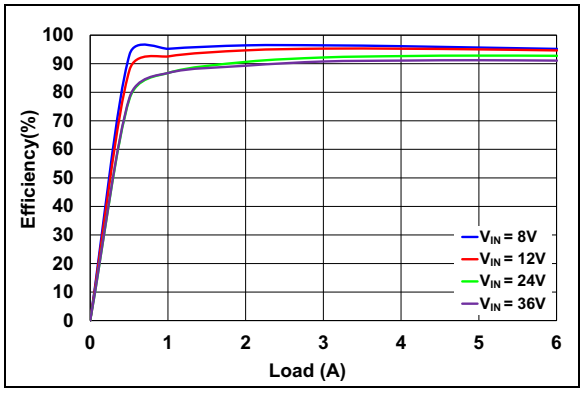


FIGURE 2-5: *Efficiency (V_{OUT} = 5V) vs. Output Current @ 400 kHz (HLL Mode).*

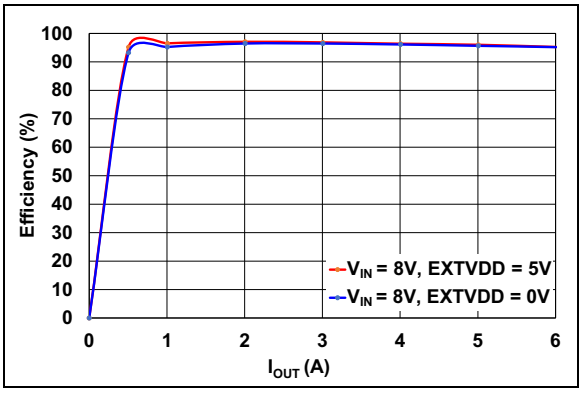


FIGURE 2-8: *MIC24066 Efficiency (V_{IN} = 8V, V_{OUT} = 5V) @ 400 kHz.*

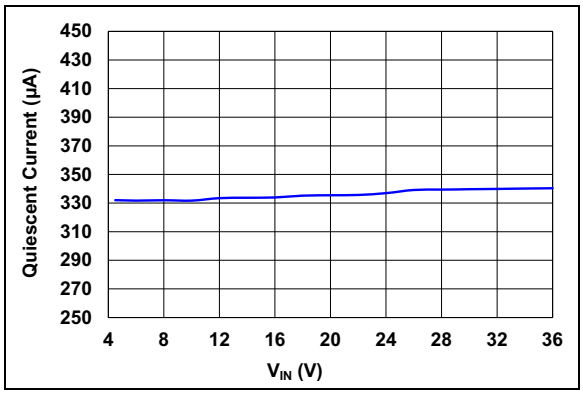


FIGURE 2-6: *V_{IN} Quiescent Current vs. Input Voltage.*

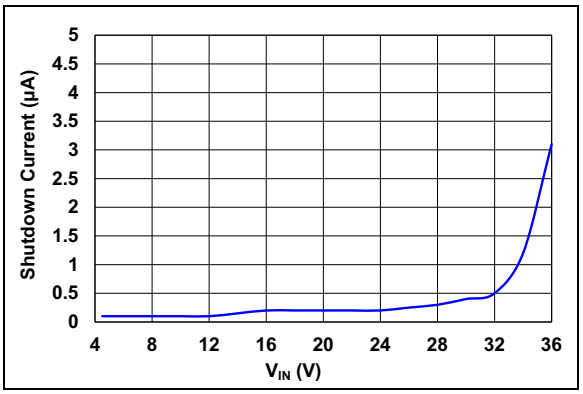


FIGURE 2-9: *Shutdown Current vs. Input Voltage.*

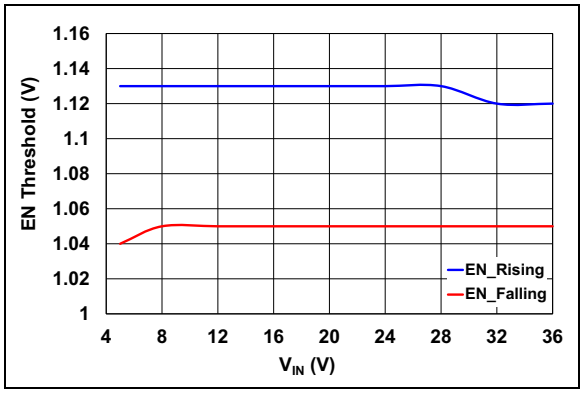


FIGURE 2-7: *Enable Threshold vs. Input Voltage.*

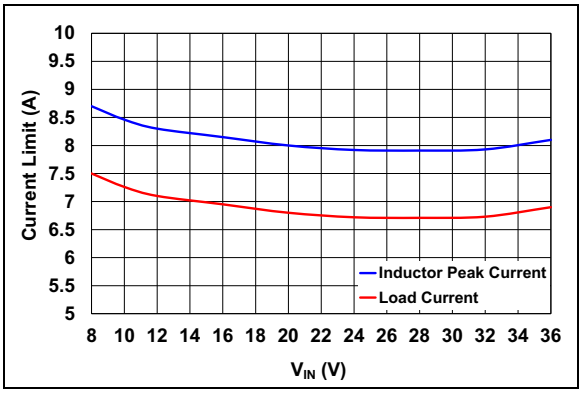


FIGURE 2-10: *Current Limit vs. Input Voltage (V_{OUT} = 5V, RCL = 1 kΩ).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C. Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

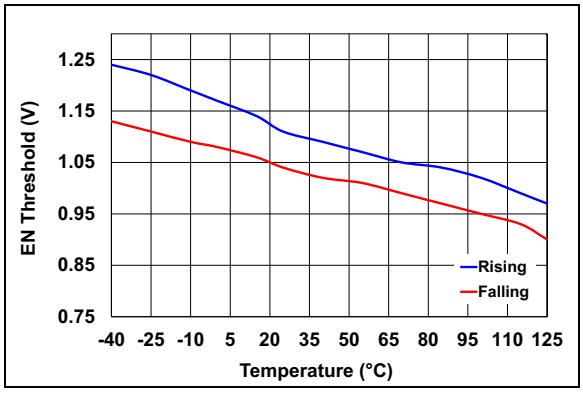


FIGURE 2-11: *Enable Threshold vs. Temperature (V_{IN} = 12V).*

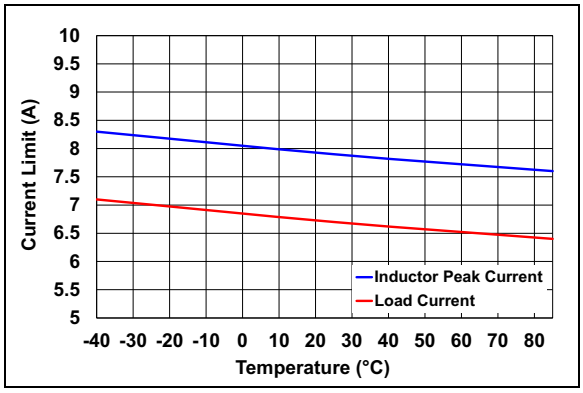


FIGURE 2-14: *Current Limit vs. Temperature (V_{IN} = 12V, V_{OUT} = 5V, RCL = 1 kΩ).*

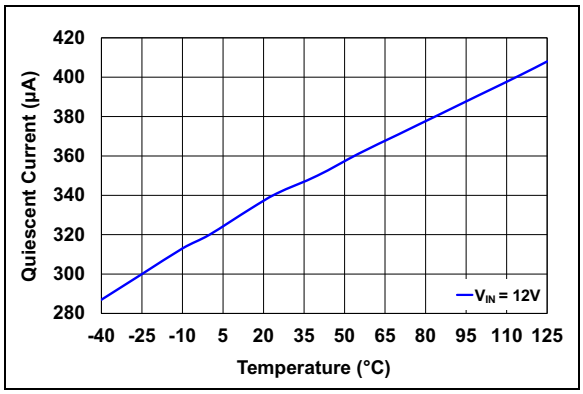


FIGURE 2-12: *V_{IN} Quiescent Current vs.Temperature (V_{IN} = 12V).*

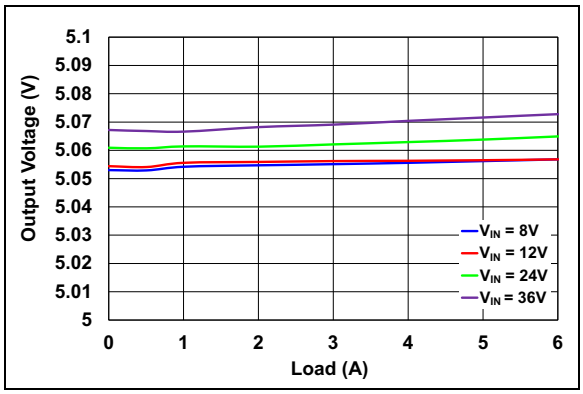


FIGURE 2-15: *Output Voltage (V_{OUT} = 5V) vs. Load (@ 400 kHz, HLL Mode).*

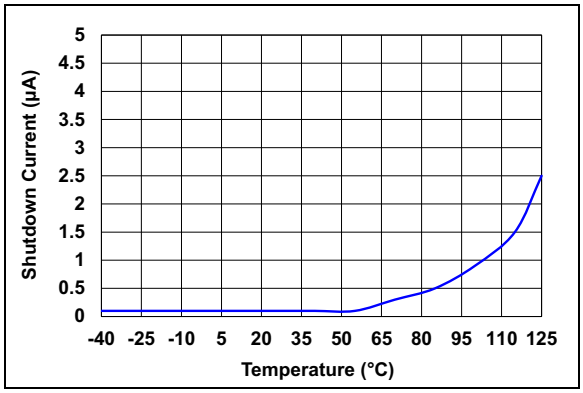


FIGURE 2-13: *Shutdown Current vs. Temperature (V_{IN} = 12V).*

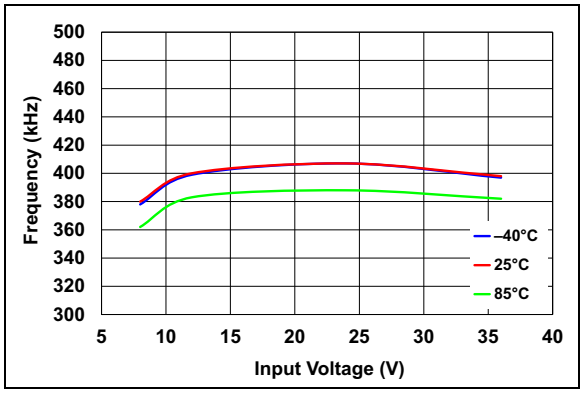


FIGURE 2-16: *Switching Frequency vs. Input Voltage (@NL).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C. Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

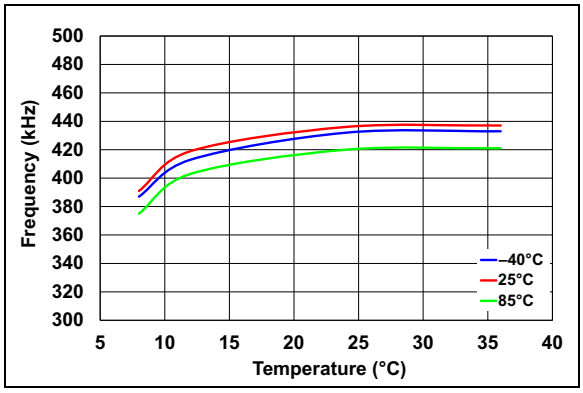


FIGURE 2-17: *Switching Frequency vs. Temperature (@ 6A).*

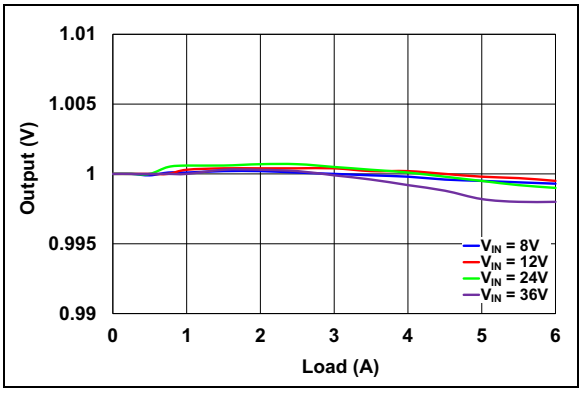


FIGURE 2-20: *Output Voltage (V_{OUT} = 1V) vs. Load (@ 400 kHz, CCM Mode).*

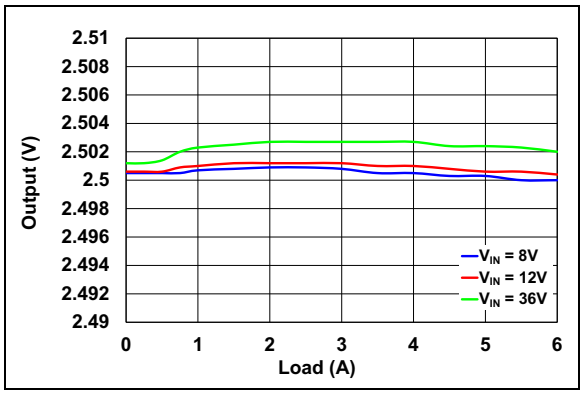


FIGURE 2-18: *Output Voltage (V_{OUT} = 2.5V) vs. Load (@ 400 kHz, CCM Mode).*

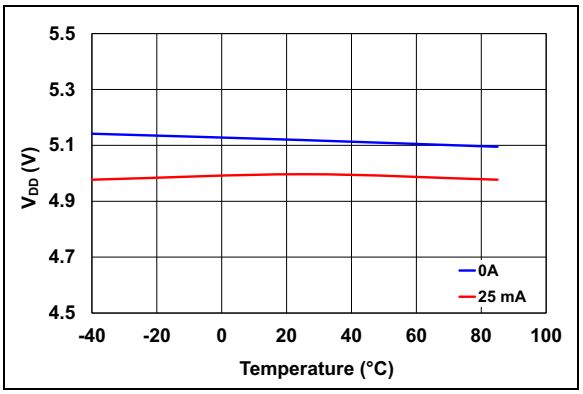


FIGURE 2-21: *V_{DD} vs. Temperature (V_{IN} = 12V).*

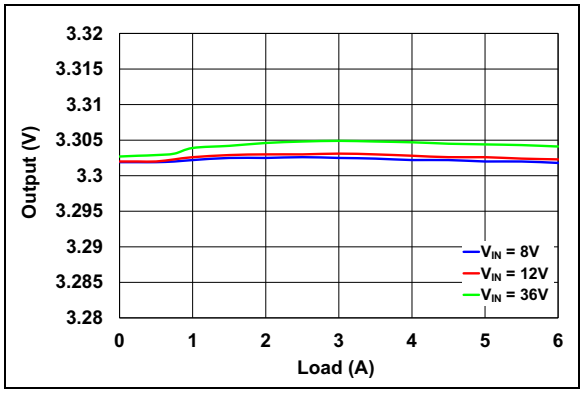


FIGURE 2-19: *Output Voltage (V_{OUT} = 3.3V) vs. Input Voltage (@ 400 kHz, CCM Mode).*

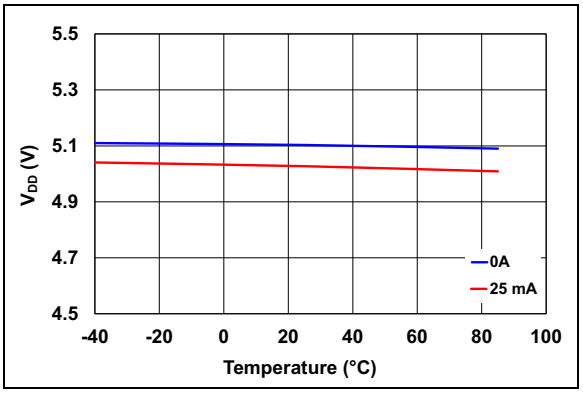


FIGURE 2-22: *EXTVDD vs. Temperature (EXTVDD = 12V).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C. Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

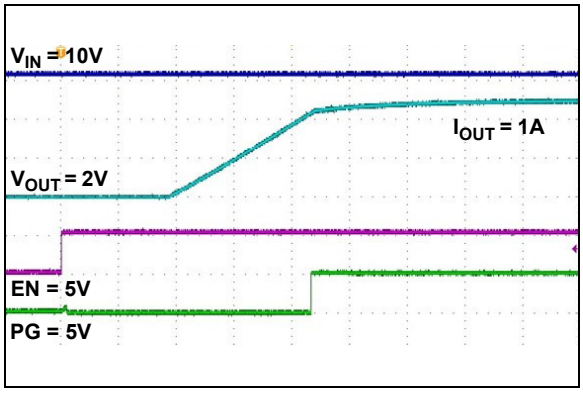


FIGURE 2-23: *Enable Turn-on and Rise Time.*

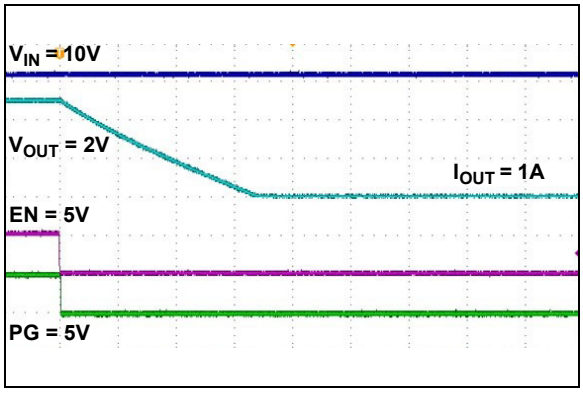


FIGURE 2-26: *Switching Waveforms Phasing (V_{OUT} = 12V, I_{OUT} = 0A).*

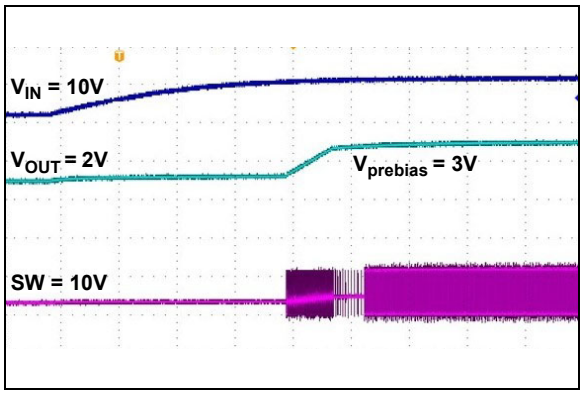


FIGURE 2-24: *V_{IN} Start-Up with Pre-Biased Output.*

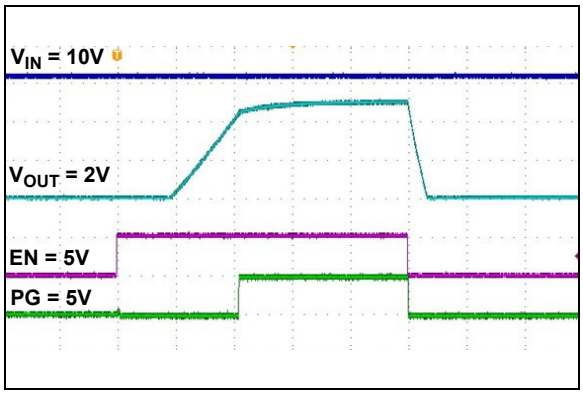


FIGURE 2-27: *Enable Turn-On and Turn-off.*

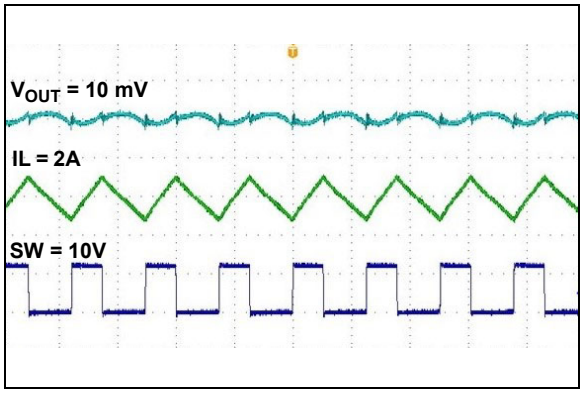


FIGURE 2-25: *Switching Waveform (I_{OUT} = 0A).*

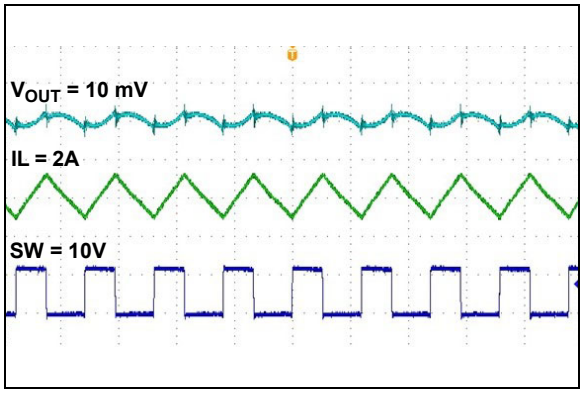


FIGURE 2-28: *Switching Waveforms (I_{OUT} = 6A).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C. Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

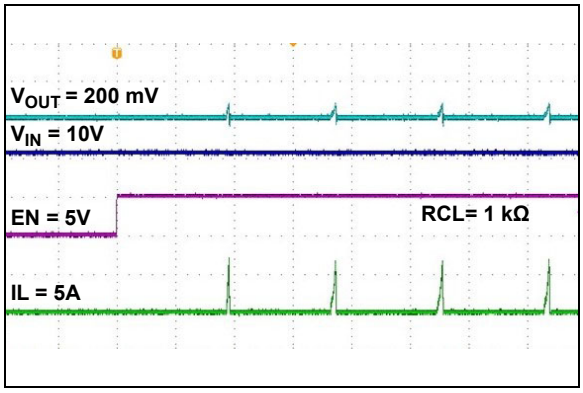


FIGURE 2-29: *Enable Start-Up into Short Circuit.*

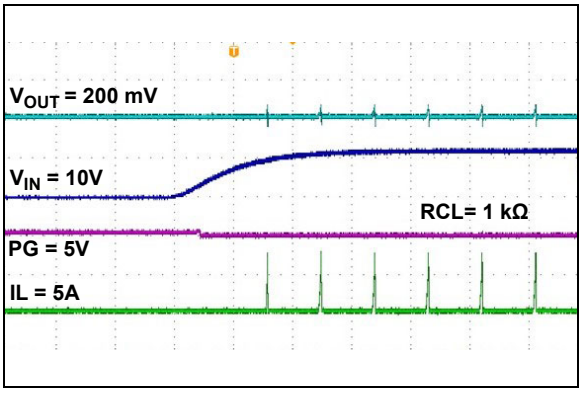


FIGURE 2-32: *V_{IN} Start-Up into Short Circuit.*

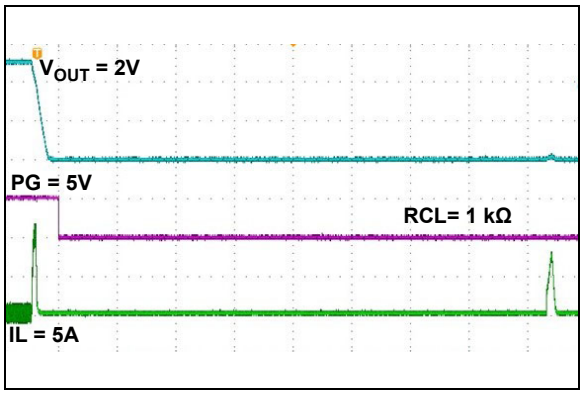


FIGURE 2-30: *Response to Short Circuit.*

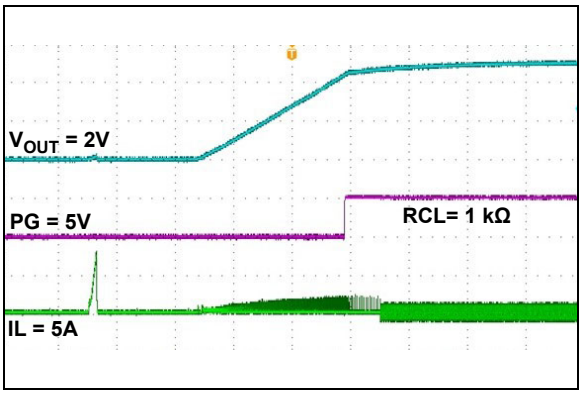


FIGURE 2-33: *Recovery from Short Circuit.*

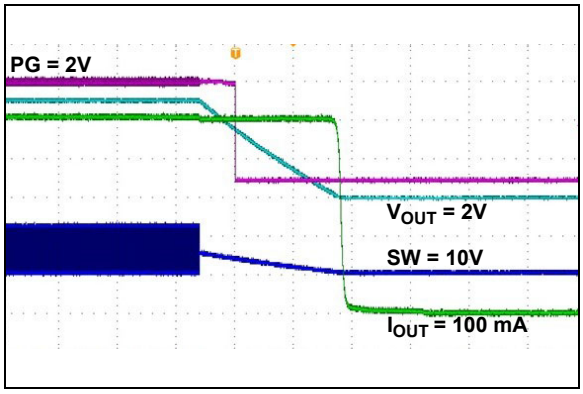


FIGURE 2-31: *Thermal Shutdown Response.*

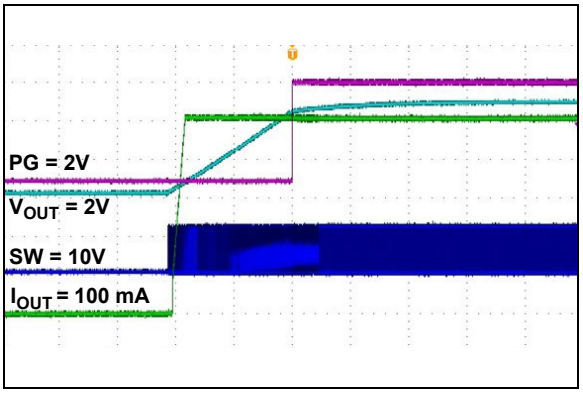


FIGURE 2-34: *Thermal Shutdown Recovery Response.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 5V; f_{SW} = 400 kHz; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C. Measurements were done using Typical Application Circuit schematic unless specific changes are mentioned.

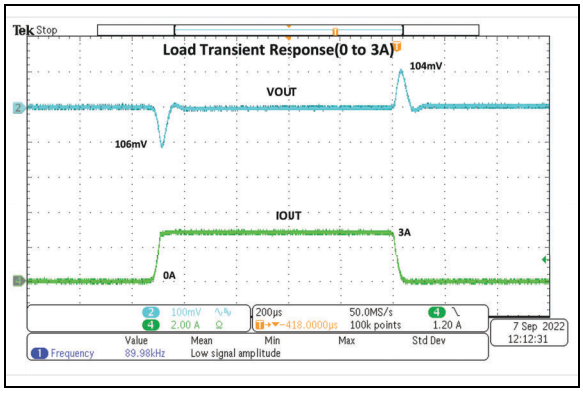


FIGURE 2-35: *Load Transient Response (V_{OUT} = 5V, I_{OUT} = 0A to 3A).*

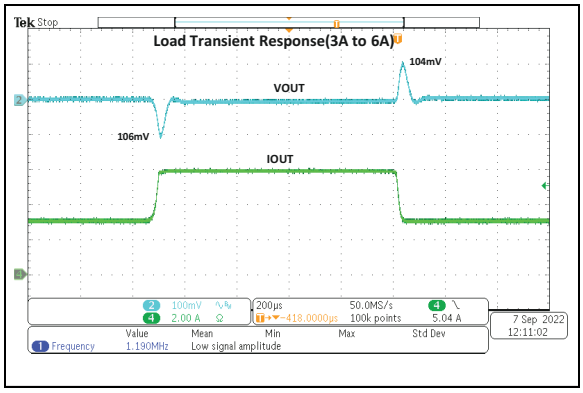


FIGURE 2-36: *Load Transient with Droop (V_{OUT} = 5V, I_{OUT} = 3A to 6A).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1, 14, 23, 28, 36	NC	Not Connected. Leave Pin Unconnected.
2	PG	Open drain Power Good Output: PG is pulled to ground when the output voltage is below 10% of the target voltage. Pull-up PG to VDD through a 10 kΩ resistor to set logic high level when the output voltage is above 90% of the target voltage.
3	ILIM	Current Limit Adjust Input: Connect a resistor from ILIM to the SW node to set current limit. Refer to Section 4.5.2 Current Limit for more details.
4, 25, 32, 33	AGND	Analog ground: Reference node for all the control logic circuit inside the device. Connect AGND to PGND at one point.
5	SW	Switch Node Output: Connect all the SW pins together. Connect one terminal of the Inductor to the SW node.
6	BST	Bootstrap Capacitor connection node: BST pin is the supply voltage for the internal High side MOSFET driver. Connect a 0.1 µF low ESR ceramic capacitor between BST pin and the SW pin.
7, 8, 9, 10, 11, 12, 13	VIN	Power Supply Input to the internal high side MOSFET: Connect all the VIN pins together. Connect low ESR ceramic capacitors between VIN and PGND pins close to the IC to supply switching currents.
14	NC	Not Connected. Pin can be floating or grounded.
15, 16, 17, 18	PGND	Power Ground: PGND is the return path for the low side MOSFET current and for the low side MOSFET driver. Connect all the PGND pins together and connect to the power ground plane.
19, 20, 21, 22	SW	Switch Node Output: Connect all the SW pins together. Connect one terminal of the Inductor to the SW node.
23	NC	Not Connected. Pin can be floating or grounded.
24	PVDD	Internal High Voltage LDO output: This is the supply for the low side MOSFET driver and for the Bootstrap capacitor. Connect a minimum 4.7 µF low ESR ceramic capacitor from PVDD to PGND.
26	EXTVDD	Auxiliary LDO Input: Connect to a supply higher than 4.7V (typical) to bypass the internal high voltage LDO or leave unconnected/connect to ground. Connect a minimum 1 µF low ESR ceramic capacitor between EXTVDD and PGND when EXTVDD is connected to external supply.
27	EN	Enable Logic Input: Connect to VIN or Drive from an external logic signal. When EN = Logic High, the device is enabled; When EN = Logic Low, the device is disabled.
29	FREQ	Frequency Programming Input: Connect to VIN to set the switching frequency to 800 kHz. Connect to mid-point of a resistor divider from VIN to AGND to set the switching frequency. Refer to Section 5.1 Setting the Switching Frequency.
30	SS/MODE	***Soft Start programming Input (MIC24066):*** Connect a capacitor between SS and AGND to program output voltage soft start time. ***Light Load Operating Mode Selection Input (MIC24067):*** Connect to AGND or leave unconnected to set the light load operating mode to HyperLight Load (HLL). Connect to VDD to set mode to Continuous Conduction Mode (CCM) over entire load current range.
31	FB	Feedback Input: Connect to mid-point of a resistor divider from output voltage to AGND to set desired output voltage.
34	VDD	Bias Supply: Bias supply for the internal control logic circuit. Connect to PVDD through 2.2Ω series resistor. Connect a minimum 2.2 µF low ESR ceramic capacitor from VDD to AGND.

TABLE 3-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol	Description
35	SVIN	Supply Voltage Input to the internal LDO: Connect to VIN through low pass RC filter to VIN. Connect to VIN through 2.2Ω series resistor. Connect a minimum 1 µF low ESR ceramic capacitor from SVIN to AGND.
EP	AGND	Exposed Pad: AGND down bonded to this EP. Connect it to AGND plane.
	VIN	Exposed Pad: VIN connected to this EP. Connect to VIN plane.
	SW	Exposed Pad: MOSFET junction is connected to this EP. Connect to SW plane.

3.1 Power Good Output Pin (PG)

Connect PG to VDD through a pull up resistor. PG is low when the FB voltage is 10% below the 0.6V reference voltage.

3.2 Current Limit Pin (ILIM)

Connect a resistor from ILIM to SW to set current limit. Refer to Section 4.5.2 Current Limit for more details.

3.3 Switch Pin (SW)

SW pin 5 is a used to sense low-side MOSFET current by monitoring the SW node voltage for negative current limit function. Connect SW pin 5 to the pins where inductor is connected.

3.4 Bootstrap Capacitor Pin (BST)

BST capacitor acts as supply for the high-side N-MOSFET driver. Connect a minimum of 0.1 µF low ESR ceramic capacitor between BST and SW.

3.5 Input Voltage Pin (VIN)

Supply Input to the MOSFETs. Connect all the VIN pins together and VIN EP. Connect low ESR ceramic capacitors between VIN and PGND pins close to the IC to supply switching currents.

3.6 Power Ground Pin (PGND)

PGND provides return path for the internal low-side N-MOSFET gate driver output and also acts as reference for current limit comparator. Connect PGND to the external low-side N-MOSFET source terminal and to the return terminal of PVDD bypass capacitor.

3.7 Switch Pin (SW)

SW Pins 19-22 are for high current connection of internal MOSFET drain-source junction to the inductor. Connect all SW pins and SW EP together.

3.8 Internal High Voltage LDO Output Pin (PVDD)

Internal high voltage LDO Output of the MIC24066/7. PVDD is the supply for the low-side MOSFET driver and for floating high-side MOSFET driver. Connect a minimum of 4.7 µF low ESR ceramic capacitor from PVDD to PGND.

3.9 EXTVDD

Supply to the internal low voltage LDO. Connect EXTVDD to the output of the Buck converter if it is between 4.7V to 14V to improve system efficiency. Bypass EXTVDD with a minimum of 4.7 µF low ESR ceramic capacitor.

3.10 Enable Input Pin (EN)

EN is a logic input. Connect to logic high to enable the converter and connect to logic low to disable the converter.

3.11 Switching Frequency Programming Input Pin (FREQ)

Switching Frequency Programming Input. Connect to mid-point of the resistor divider formed between VIN and AGND to set switching frequency of the converter. Tie FREQ to VIN to set the switching frequency to 800 kHz. Refer to Section 5.1 Setting the Switching Frequency for more details.

3.12 Soft Start/Light Load Mode Selection Input (SS/MODE)

Soft Start/Light Load Mode Selection Input. For MIC24066 connect a ceramic capacitor from SS to AGND to set the output soft start time. For MIC24067 connect MODE pin to VDD to select Continuous Conduction Mode under light loads or connect to AGND to select HyperLight Load (HLL) Mode of operation under light loads. Refer to Section 5.3 Setting the Soft-Start Time for further details.

3.13 Feedback Input Pin (FB)

FB is input to the transconductance amplifier of the control loop. The control loop regulates the FB voltage to 0.6V. Connect FB node to mid-point of the resistor divider between output and AGND.

3.14 Analog Ground Pin (AGND)

AGND is reference to the analog control circuits inside the controller. Connect AGND to PGND at one point on PCB.

3.15 Bias Voltage Pin (VDD)

Supply for the controller internal analog circuits. Connect VDD to PVDD through a 2.2Ω resistor. Connect a minimum of 4.7 µF low ESR ceramic capacitor from VDD to AGND for decoupling.

3.16 SVIN

Supply Input to the internal high voltage LDO. Connect to the main power source and bypass to PGND with a minimum of 1 µF low ESR ceramic capacitor.

3.17 AGND (EP)

Connect to AGND copper plane to improve thermal performance of the MIC24066/7.

4.0 FUNCTIONAL DESCRIPTION

4.1 Control Architecture

The MIC24066/7 is an adaptive ON-time synchronous step-down DC/DC regulator. It is designed to operate over a wide input voltage range from 4.5V to 36V and provides a regulated output voltage up to 6A of load current. An adaptive ON-time control scheme is employed in order to obtain a constant-switching frequency and to simplify the control compensation. Overcurrent protection is implemented without the use of an external sense resistor. The device includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

The output voltage is sensed by the feedback pin (FB) via the voltage divider R1 and R2 and is compared to a 0.6V reference voltage V_{REF} at the error comparator through a low-gain trans-conductance (g_m) amplifier. If the feedback voltage decreases and the output of the g_m amplifier fall below 0.6V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimation" circuitry:

EQUATION 4-1:

$$T_{ON(EST)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output Voltage

V_{IN} = Power Stage Input Voltage

f_{SW} = Switching Frequency

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier fall below 0.6V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(MIN)}$, which is about 300 ns then the MIC24066/7 control logic will apply the $t_{OFF(MIN)}$ instead. The minimum $t_{OFF(MIN)}$ period is required to maintain enough energy in the boost capacitor (CBST) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300 ns $t_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{T_S - T_{OFF(MIN)}}{T_S} = 1 - \frac{300\ ns}{T_S}$$

Where:

T_S = $1/f_{SW}$

It is not recommended to use MIC24066/7 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the V_{DD} voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 36V to 1.0V.

Figure 4-1 shows the control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

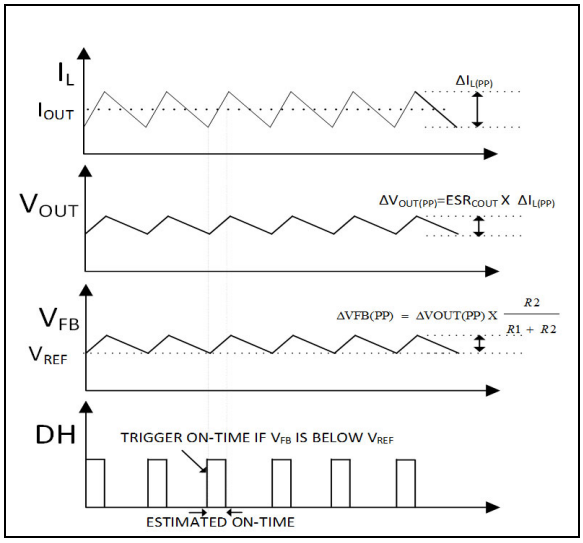


FIGURE 4-1: *Steady State Operation (FB Ripple Shows Injected and ESR Ripple Only, Reactive Impedances Neglected).*

Figure 4-2 shows the operation of the MIC24066/7 during load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge CBST since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in the MIC24066/7 converter. The transient response is shown in Figure 4-3.

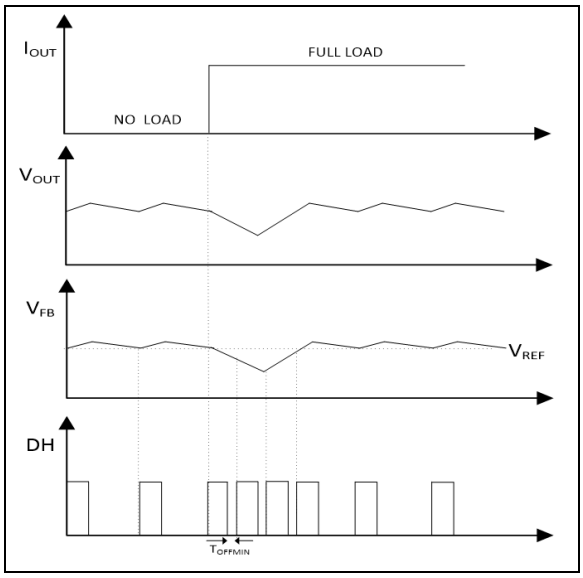


FIGURE 4-2: *MIC24066/7 Load Transient Response.*

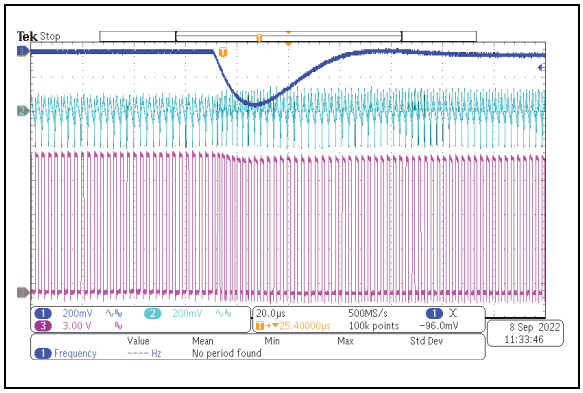


FIGURE 4-3: *MIC24066/7 Load Transient Response.*

Unlike true current-mode control, the MIC24066/7 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. In order to meet the stability requirements, the feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20 mV~100 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation.

4.2 Stability Analysis

The MIC24066/7 uses ripple-based constant on time architecture to generate switching pulses. The FB node requires in-phase ripple which resembles inductor current for regulation. The magnitude of ripple needs to be in the range of 20 mV-70 mV. The ripple can be extracted from ESR of the output capacitor in addition to capacitor ripple. The Figure 4-4 shows the ripple at FB node with respect to reference voltage.

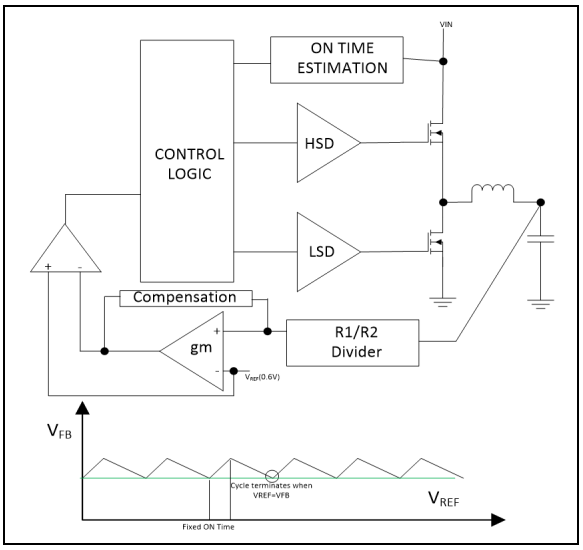


FIGURE 4-4: *MIC24066/7 Ripple at FB node.*

If the ripple voltage at the FB node not in phase with inductor current ripples, double or multiple pulses may occur causing the circuit to become unstable. The output capacitors generally have three components. The capacitive ripple lags the inductor current ripple. ESR ripple is in phase with inductor current. ESL ripple effect is very minimal in low voltage capacitors.

As shown in Figure 4-5, output capacitive ripple lags inductor current and ESR ripple is in phase with inductor current ripple. Figure 4-6 shows the vector relation of effective FB ripple voltage for high ESR capacitors.

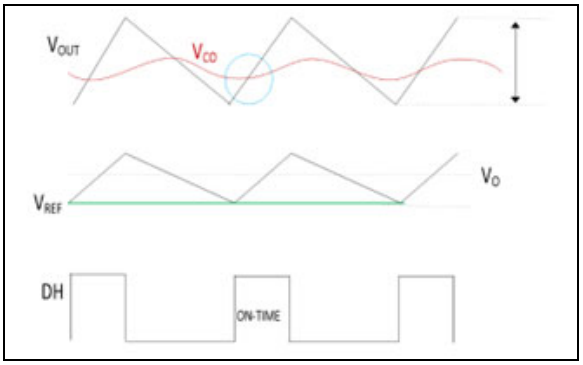


FIGURE 4-5: *Output Capacitive and ESR Ripple.*

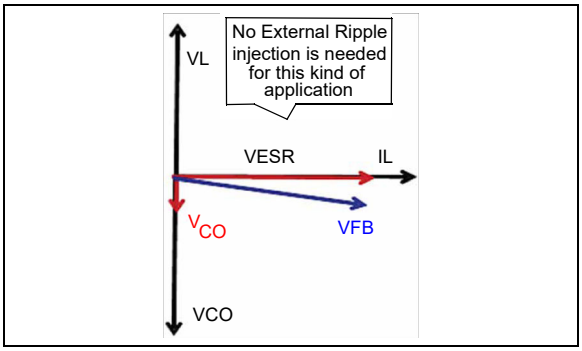


FIGURE 4-6: *Output Capacitive and ESR Ripple Vector Relation.*

External injected ripple is not required when ESR ripple is high as compared to capacitive ripple. The modern loads require output voltage steady state ripple to be less than 1% of regulation voltage. For output voltages in the range of 1V, output steady state ripple voltage requirement is in the order of 10 mV for modern high current ASIC loads. Customers generally use ceramic capacitors or low ESR tantalum capacitors to meet steady state requirements for their loads. In those cases, MIC24066/7 control loop requires external ripple injection to the FB node.

Note that as R_{BIAS} is always present, it draws an additional current form the injection driver when INJ pin is 4.5V for 100 ns. This adds to the device's IQ. However, its contribution to the device's IQ will be low, because this current will be present for 100 ns only. Another thing to note is that the INJ driver must be capable of supplying this additional current.

4.3 Ripple Injection for Low ESR Capacitors

When customers use low ESR electrolytic capacitors or tantalum capacitors, external ripple can be injected by connecting feed forward capacitor (C_{FF}) from output to the FB node as shown in Figure 4-7.

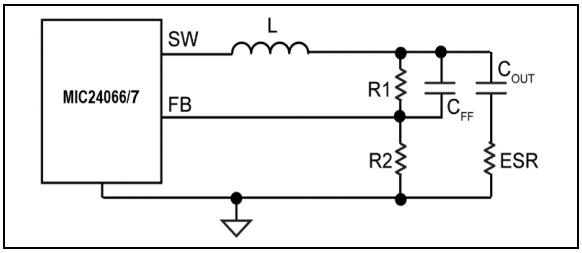


FIGURE 4-7: *Feed Forward Capacitor.*

EQUATION 4-3:

$$\frac{V_{FB}}{V_{OUT}}(s) = \frac{R2}{R1+R2} \times \frac{(1 + s \times C_{FF} \times R1)}{\left(1 + s \times C_{FF} \times \frac{R1 \times R2}{R1+R2}\right)}$$

As shown in Figure 4-8, feed forward capacitor bypasses high frequency ripple to the FB pin and provides phase boost at mid frequency.

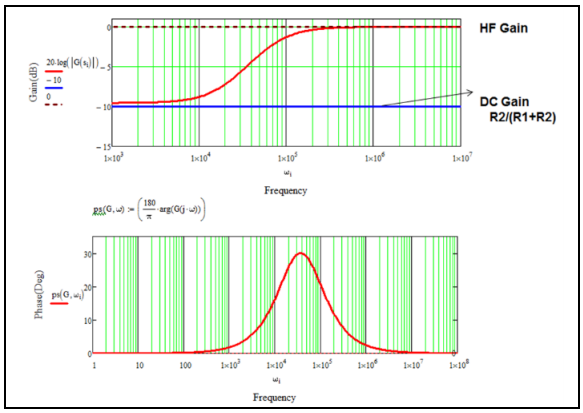


FIGURE 4-8: *Feed Forward Capacitor Gain and Phase Plots.*

4.4 Ripple Injection for Ceramic Capacitors

Customers use ceramic capacitors as output filter for much high performance ASIC. Ceramic capacitors have very low ESR and ESL. The MIC24066/7 need extra ripple injected from switch node. In those applications, external ripple can be injected by connecting series RC network from switch node to FB node as shown in Figure 4-9.

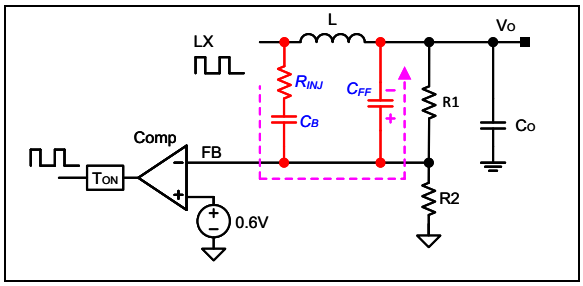


FIGURE 4-9: *MIC24066/7 External Ripple Injection Circuit.*

The purpose of C_B is to block the DC component and forward high frequency from the switch node. It is required to select C_B value very much higher than C_{FF} value. The following equation denotes the amount of ripple injected at FB node.

EQUATION 4-4:

$$\Delta V_{FB(PP)} = V_{IN} \times K_{DIV} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau}$$

$$K_{DIV} = \frac{R1 \,/\!/\, R2}{R_{INJ} + R1 \,/\!/\, R2}$$

Where:

V_{IN}	=	Power stage input voltage
D	=	Duty Cycle
f_{SW}	=	Switching Frequency
τ	=	(R1//R2//R_{INJ}) × C_{FF}

It is assumed that the time constant associated with C_{FF} must be much greater than the switching period:

EQUATION 4-5:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1$$

If the voltage divider resistors R1 and R2 are in the kΩ range, a C_{FF} of 1 nF to 22 nF can easily satisfy the large time constant requirements. Also, an 100 nF injection capacitor C_{INJ} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

1. Select C_{FF} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{FF} is 1 nF to 22 nF if R1 and R2 are in kΩ range.
2. Select R_{INJ} according to the expected feedback voltage ripple using Equation 4-6:

EQUATION 4-6:

$$K_{DIV} = \frac{\Delta V_{FB(PP)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1-D)}$$

Then the value or R_{INJ} is obtained as:

$$R_{INJ} = (R1 \,/\!/\, R2) \times \left(\frac{1}{K_{DIV}} - 1\right)$$

3. Select C_{INJ} as 100 nF, which could be considered as short for a wide range of the frequencies.

4.5 Detailed Device Description

The MIC24066 always operates in CCM and soft start is adjustable with external capacitor. MIC24067 has MODE selector for CCM/DCM and has fix internal sift start.

4.5.1 HYPERLIGHT LOAD (HLL) MODE (MIC24067)

In continuous mode, the inductor current can go negative at light loads. However, at light loads the MIC24067 is able to force the inductor current to operate in discontinuous mode when MODE is set to HLL Mode. In HLL mode, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC24067 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.6V.

The MIC24067 has a zero crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} >0.6V and the inductor current goes slightly negative, then the MIC24067 automatically power down most of the IC circuitry and goes into a low-power mode.

Once the MIC24067 goes into discontinuous mode, both the high-side and low-side MOSFETs are kept in off state. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. Figure 4-10 shows the control loop timing in discontinuous mode.

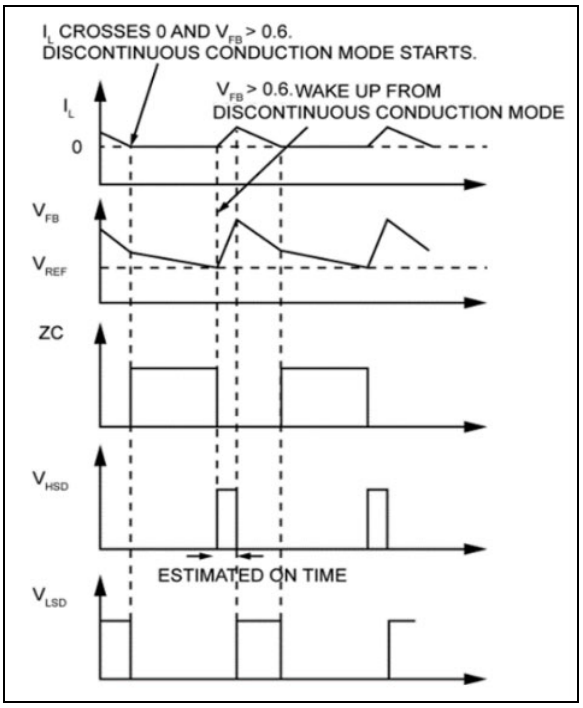


FIGURE 4-10: *MIC24066/7 Control Loop Timing (HLL Mode).*

During discontinuous mode, the bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 300 µA, allowing the MIC24066/7 to achieve high efficiency in light load applications.

4.5.2 CURRENT LIMIT

The MIC24066/7 uses the $R_{DS(ON)}$ of the internal low-side power MOSFET to sense overcurrent conditions. This method will avoid additional cost, use of additional board space and power losses taken by a discrete current sense resistor.

Current limit threshold can be programmed by connecting a resistance from switch node to ILIM pin.

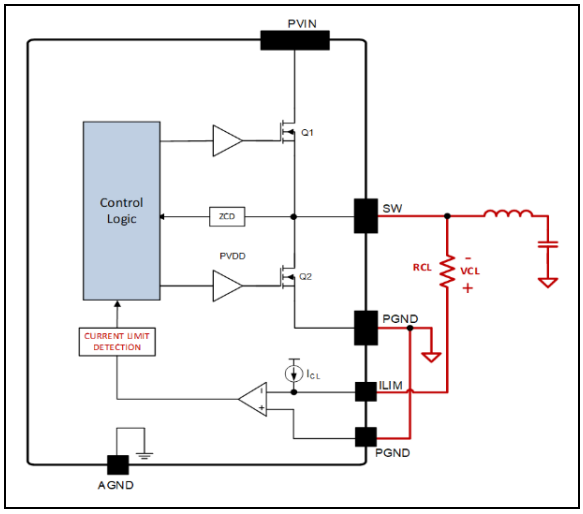


FIGURE 4-11: *MIC24066/7 Current-Limiting Circuit.*

In each switching cycle of the converter, the inductor current is sensed by monitoring the low-side MOSFET voltage during the OFF period of the switching cycle during which the LSFET is ON. There is 150 ns (typ) blanking period after which sense signal is considered for protection. The blanking period improves noise immunity. If the low side MOSFET voltage is greater than VCL threshold, then the MIC24066/7 keeps the low side FET ON until the voltage across the low side MOSFET is below the VCL. HS FET is turned on once the voltage across the low side MOSFET is below the VCL. If the voltage across the low side MOSFET is greater than the VCL for 8 consecutive clock cycles then the part enters into high impedance mode for a time period equal to hiccup timeout. After the hiccup timeout, the controller initiates soft start sequence. The same repeats if the part hits current limit again (even during soft start also). This mode of operation is called "hiccup mode" and its purpose is to protect the downstream load in case of a hard short.

The following Figure 4-12 shows a typical behavior when the device enters current limit and the output voltage recovery when overcurrent condition is cleared.

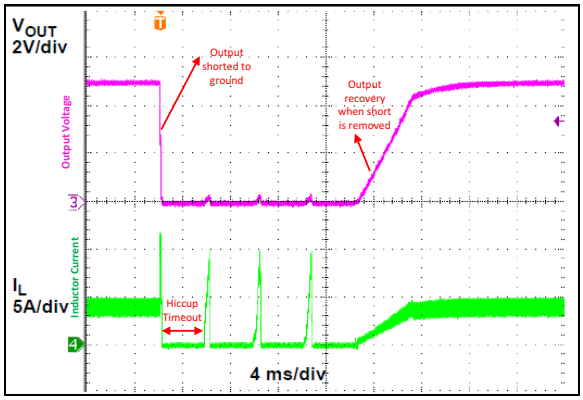


FIGURE 4-12: *MIC24066/7 Current-Limit Threshold Relationship to Output Current.*

The current limit resistor value can be calculated using the formula below:

EQUATION 4-7:

$$RCL = \frac{(I_{LIMIT} + \Delta IL) \times R_{DSON} - V_{OFFSET}}{ICL}$$

Where:

I_{LIMIT}	=	Desired Current Limit (Average Value)
ΔIL	=	Inductor Peak to Peak Ripple Current
R_{DSON}	=	On-Resistance of Low-Side Power MOSFET
V_{OFFSET}	=	Current-limit Comparator Offset (refer to Electrical Characteristics table)
ICL	=	ILIM source current, the typical value is 115 µA in Electrical Characteristics table.

4.5.3 SOFT-START

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC24066 device offer programmable soft start time by placing a capacitor at the SS pin. The MIC24067 implements an internal digital soft-start by making the 0.6V reference voltage V_{REF} ramp from 0 to 100% in about 5 ms. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption.

4.5.4 PVDD REGULATOR AND EXTVDD LDO

MIC24066/7 has integrated high voltage LDO that provides a 5V regulated output for the input voltage up to 36V. When V_{IN} < 5.5V, VDD can be tied to PVIN pins to bypass the internal linear regulator. The internal LDO powers the control circuitry and gate drive current.

The MIC24066/7 also features an auxiliary low voltage LDO which is powered by EXTVDD. When the voltage on the EXTVDD is higher than 4.6V (typ), this auxiliary LDO is enabled and powers all the internal circuitry. At the same time the main high voltage LDO is disabled. This increases the efficiency of the system by reducing the differential voltage across the high voltage LDO and hence reducing the power losses in the LDO. In general the output of the buck converter is used as the power supply for the auxiliary LDO by connecting EXTVDD pin to the output of the buck converter. The maximum voltage that can be applied at the EXTVDD is limited to 14V. The following Figure 4-13 shows the internal 5V LDO and EXTVDD connection in MIC24066/7.

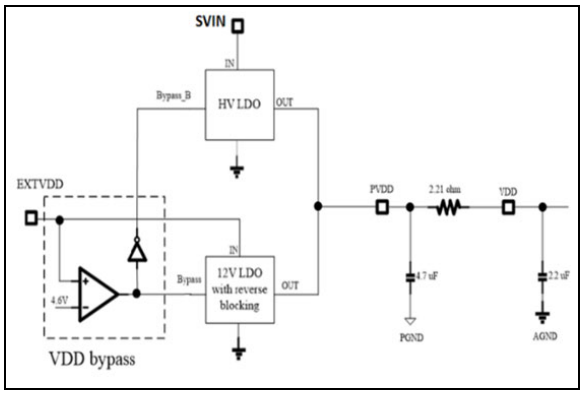


FIGURE 4-13: *MIC24066/7 EXTVDD.*

Considering the EXTVDD is powered from V_{OUT} of buck regulator. The V_{OUT} is noisy if there is a fast changing load. When $V_{OUT} > 5V + V_{DROPOUT}$, the noise could be suppressed by loop of 12V LDO. But when $V_{OUT} = 5V$, the 12V LDO works in dropout mode, so there is no loop gain. The LDO acts just like a resistor. It is not recommended to connect EXTVDD to VOUT, if VOUT < EXTVDD rising threshold.

4.5.5 POWER GOOD (PG)

The Power Good (PG) pin is an open drain output which indicates logic high when the output is nominally > 92% of its steady state voltage. A pull-up resistor of more than 10 kΩ should be connected from PG to VDD.

4.5.6 EN FUNCTION

The MIC24066/7 has EN pin which is used either to enable/disable switching. When EN pin threshold is higher than 1.6V, MIC24066/7 starts functioning. The internal regulator will power up and starts switching. The following Figure 4-14 shows the EN pin sequencing.

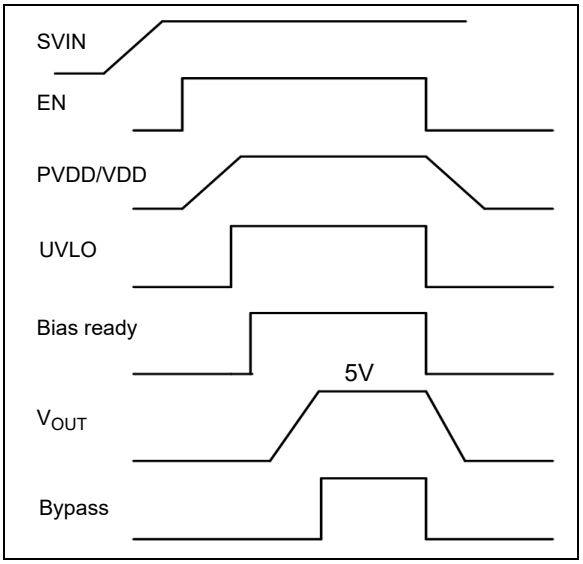


FIGURE 4-14: *EN Pin Sequencing.*

When EN pin threshold is below 0.6V, MIC24066/7 put in to shutdown mode. The MIC24066/7 stops switching and all internal control circuitry switched OFF to reduce quiescent current. The EN pin along with PG pin can be used for sequencing multiple MIC24066/7. It is recommended to power up VIN before EN signal.

4.5.7 NEGATIVE CURRENT LIMIT

The MIC24066/7 implements negative current limit by sensing the SW voltage when the low-side FET is ON. If the SW node voltage exceeds 48 mV typical, the device turns off the low-side FET for 500 ns. Negative current limit value is shown in Equation 4-8.

EQUATION 4-8:

$$I_{NLIM} = \frac{48\ mV}{R_{DSON}}$$

Where:

I_{NLIM} = Negative Current Limit

R_{DSON} = On-Resistance of Low-Side Power MOSFET

4.5.8 AUXILIARY BOOTSTRAP LDO (EXTVDD)

The MIC24066/7 features an auxiliary bootstrap LDO which improves the system efficiency by supplying the internal circuit bias power and gate drivers from the converter output voltage. This LDO is enabled when the voltage on the EXTVDD pin is above 4.6V (typical) and at the same time the main LDO which operates from VIN is disabled to reduce power consumption.

5.0 APPLICATION INFORMATION

5.1 Setting the Switching Frequency

The MIC24066/7 is an adjustable-frequency, synchronous buck controller featuring a unique adaptive on-time control architecture. The switching frequency can be adjusted between 270 kHz and 800 kHz by changing the resistor divider network between VIN and AGND pins consisting of R1 and R2 as shown in Figure 5-1:

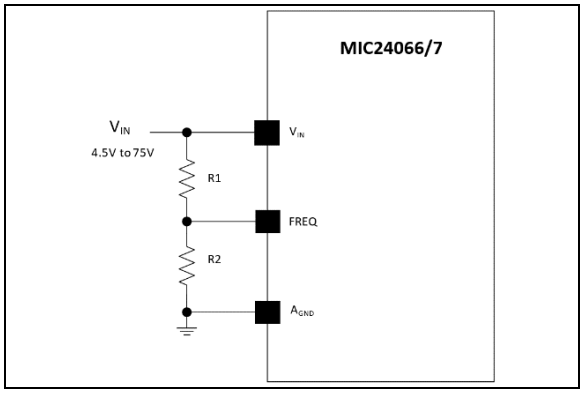


FIGURE 5-1: *Switching Frequency Adjustment.*

Equation 5-1 shows the estimated switching frequency:

EQUATION 5-1:

$$f_{SW} = f_O \times \frac{R_2}{R_2 + R_1}$$

f_O is the switching frequency when R_1 is 100 kΩ and R_2 being open; f_O is typically 800 kHz. For more precise setting, it is recommended to use Figure 5-2:

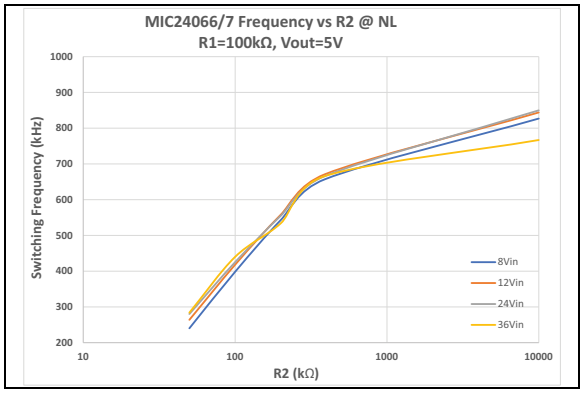


FIGURE 5-2: *Switching Frequency vs. R_2.*

5.2 Output Voltage Setting

The output voltage can be adjusted using a resistor divider from output to AGND whose mid-point is connected to FB pin as shown the Figure 5-3.

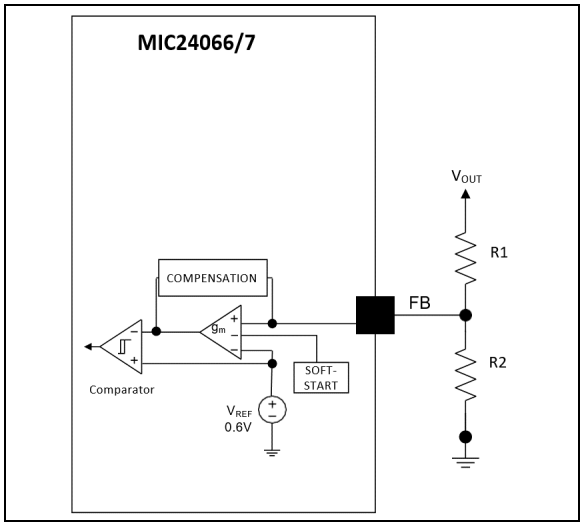


FIGURE 5-3: *Output Voltage Adjustment.*

The output voltage can be calculated using Equation 5-2:

EQUATION 5-2:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where:

V_{REF} = 0.6V

The maximum output voltage that can be programmed using the MIC24066/7 is limited to 30V, if not limited by the maximum duty cycle (see Equation 4-2).

A typical value of R1 is less than 30 kΩ. If R_1 is too large, it may allow noise to be introduced into the voltage feedback loop and also increases the offset between the set output voltage and actual output voltage because of the error amplifier bias current. If R_1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_1 is selected, R_2 can be calculated using Equation 5-3.

EQUATION 5-3:

$$R_2 = \frac{R_1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

5.3 Setting the Soft-Start Time

The output Soft-Start time can be set by connecting a capacitor from SS to AGND from 2 ms to 100 ms as shown in Figure 5-4:

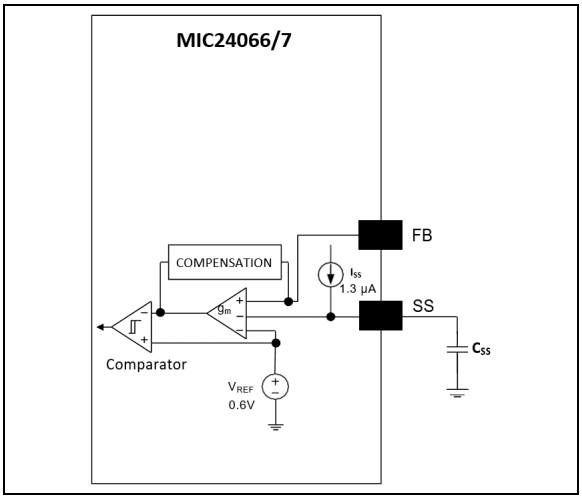


FIGURE 5-4: *Setting the Soft Start Time.*

The value of the capacitor can be calculated using Equation 5-4:

EQUATION 5-4:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}$$

Where:

C_{SS} = Capacitor from SS pin to A_{GND}
I_{SS} = Internal Soft Start Current (1.3 µA typical)
t_{SS} = Output Soft Start Time
V_{REF} = 0.6V

5.4 Inductor Selection

Inductance value, saturation and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current.

The lower the inductance value, the higher the peak-to-peak ripple current through the inductor, which increases the core losses in the inductor. Higher inductor ripple current also requires more output capacitance to smooth out the ripple current. The greater the inductance value, the lower the peak-to-peak ripple current, which results in a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 30% of the maximum output current.

The inductance value is calculated by Equation 5-5:

EQUATION 5-5:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times 0.3 \times f_{FL}}$$

Where:

V_{IN} = Input Voltage
f_{SW} = Switching Frequency
I_{FL} = Full Load Current
V_{OUT} = Output Voltage

For a selected Inductor, the peak-to-peak inductor ripple current ripple can be calculated using Equation 5-6:

EQUATION 5-6:

$$\Delta IL_{PP} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The peak inductor current is equal to the load current plus one half of the peak-to-peak inductor current ripple which is shown in Equation 5-7:

EQUATION 5-7:

$$IL_{PK} = \left(I_{LOAD} + \frac{\Delta IL_{PP}}{2}\right)$$

The RMS and saturation current ratings of the selected inductor should be at least equal to the RMS current and saturation current calculated in Equation 5-8 and Equation 5-9.

EQUATION 5-8:

$$IL_{RMS} = \sqrt{(I_{LOAD(MAX)})^2 + \frac{(\Delta IL_{PP})^2}{12}}$$

Where:

$I_{LOAD(MAX)}$ = Maximum Load Current

EQUATION 5-9:

$$IL_{SAT} = \frac{(R_{CL} \times V_{IN}) + 15\ mV}{R_{DSON}}$$

Where:

R_{CL} = Current Limit Resistor
I_{CL} = Current Limit Source Current (115 µA typical)
R_{DSON} = On Resistance of Low Side MOSFET

Maximizing the efficiency requires the proper selection of core material and minimizing the winding resistance.

Use of ferrite materials is recommended in the higher switching frequency applications. Lower cost iron powder cores may be used but the increase in core loss reduces the efficiency of the power supply.

This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetic's vendor.

The amount of copper loss in the inductor is calculated by Equation 5-10:

EQUATION 5-10:

$$P_{INDUCTOR(CU)} = (IL_{RMS})^2 \times R_{DCR}$$

5.5 Output Capacitor Selection

The main parameters for selecting the output capacitor are capacitance value, voltage rating and RMS current rating. The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Recommended capacitor types are ceramic, tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR can be calculated using Equation 5-11.

EQUATION 5-11:

$$ESR \leq \frac{\Delta V_{OUT\_PP}}{\Delta IL_{PP}}$$

Where:

ΔV_{OUT_PP}	=	Peak-to-Peak Output Voltage Ripple
ΔIL_{PP}	=	Peak-to-Peak Inductor Current Ripple

The required output capacitance to meet steady state output ripple can be calculated using Equation 5-16.

EQUATION 5-12:

$$C_{OUT} = \frac{\Delta IL_{PP}}{8 \times f_{SW} \times \Delta V_{OUT\_PP}}$$

Where:

C_{OUT}	=	Output Capacitance
f_{SW}	=	Switching Frequency

As described in Section 4.1 Control Architecture, the MIC24066/7 requires at least 20 mV peak-to-peak ripple at the FB pin to ensure that the g_m amplifier and the comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection circuit should be used to provide the enough feedback-voltage ripple. Refer to Section 4.4 Ripple Injection for Ceramic Capacitors for details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic, ceramic or OS-CON. The output capacitor RMS current is calculated in Equation 5-13.

EQUATION 5-13:

$$I_{COUT(RMS)} = \frac{\Delta IL_{PP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is shown in Equation 5-14.

EQUATION 5-14:

$$P_{COUT} = (I_{COUT(RMS)})^2 \times ESR_{COUT}$$

5.6 Input Capacitor Selection

The input capacitor reduces peak current drawn from the power supply and reduces noise and voltage ripple on the input. The input voltage ripple depends on the input capacitance and ESR. The input capacitance and ESR values can be calculated using Equation 5-15.

EQUATION 5-15:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN\_C}}$$

$$ESR_{C\_IN} = \frac{\Delta V_{IN\_ESR}}{IL_{PK}}$$

Where:

I_{LOAD}	=	Load Current
I_{LPK}	=	Peak Inductor Current
ΔV_{IN_C}	=	Input Ripple due to Input Capacitance
ΔV_{IN_ESR}	=	Input Ripple due to Input Capacitor ESR
η	=	Power Conversion Efficiency

The input capacitor should be rated for ripple current rating and voltage rating. The RMS value of input capacitor current is determined at the maximum output current. The RMS current rating of the input capacitor should be greater than or equal to the input capacitor RMS current calculated using the Equation 5-16.

EQUATION 5-16:

$$I_{C\_IN(RMS)} = I_{LOAD(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is calculated using Equation 5-17.

EQUATION 5-17:

$$P_{CIN} = (I_{IN(RMS)})^2 \times ESR_{CIN}$$

6.0 PCB LAYOUT GUIDELINES

Note: To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power and signal return paths. Use star ground technique between AGND and PGND, and minimize trace length for high-current paths.

Follow these guidelines to ensure proper operation of the MIC24066/7 buck regulator.

6.1 Integrated Circuit

- The 2.2 µF ceramic capacitor, which is connected to the VDD pin, must be located right at the IC. The VDD pin is very noise sensitive, so placement of the capacitor is critical. Use wide traces to connect to the VDD, PVDD and PGND pins.
- Connect a 2.2 µF ceramic capacitor to the EXTVDD pin, which must be located right at the IC.
- Connect the Analog Ground pin (AGND) directly to the ground planes. Do not route the AGND pin to the PGND pad on the top layer.
- Place the IC close to the point of load (POL).
- Use thick traces and minimize trace length for the input and output power lines.
- Keep the signal and power grounds separate and connected at only one location.

6.2 Input Capacitor

- Use parallel input capacitors to minimize effective ESR and ESL of the input capacitor.
- Place input capacitors next to the high-side power MOSFETs for each phase channel.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Connect the V_{IN} supply to VIN pin through a 1.2Ω resistor and connect a 1 µF ceramic capacitor from VIN pin to PGND pin. Keep both the VIN pin and GND connections short.
- Place several vias to the ground plane close to the input capacitors ground terminal.
- Use either X7R or X5R dielectric input ceramic capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any additional other type of capacitor can be placed in parallel with the input capacitor.
- In "Hot-Plug" applications, use electrolytic bypass capacitor to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3 Inductor

- Keep the inductor connection to the switch node (SW1, SW2) short.
- Do not route any signal traces underneath or close to the inductor.
- Keep the switch node (SW1, SW2) away from the feedback (FBS) pin.
- Connect the CSPx and CSNx pins directly to the drain and source of the low-side power MOSFET respectively and route the CSP and CSN traces together for each phase channel to accurately sense the voltage across the low-side MOSFET to achieve accurate current sensing.
- To minimize noise, place a ground plane under the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. There should be sufficient vias on the power traces to conduct high current between the inductor and the IC and output load. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough heatsink and air flow to keep the power components within their temperature limits. Place the input and output capacitors on the same side of the board as the IC.

6.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

6.5 V_{OUT} Remote Sense

- The remote sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, MOSFETs and other high dv/dt or di/dt sources.

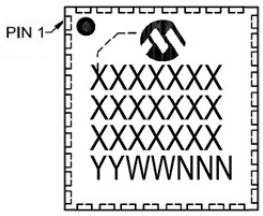
6.6 RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

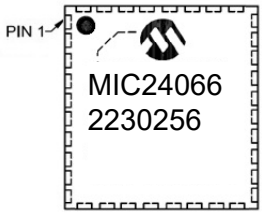
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

36-Lead VQFN



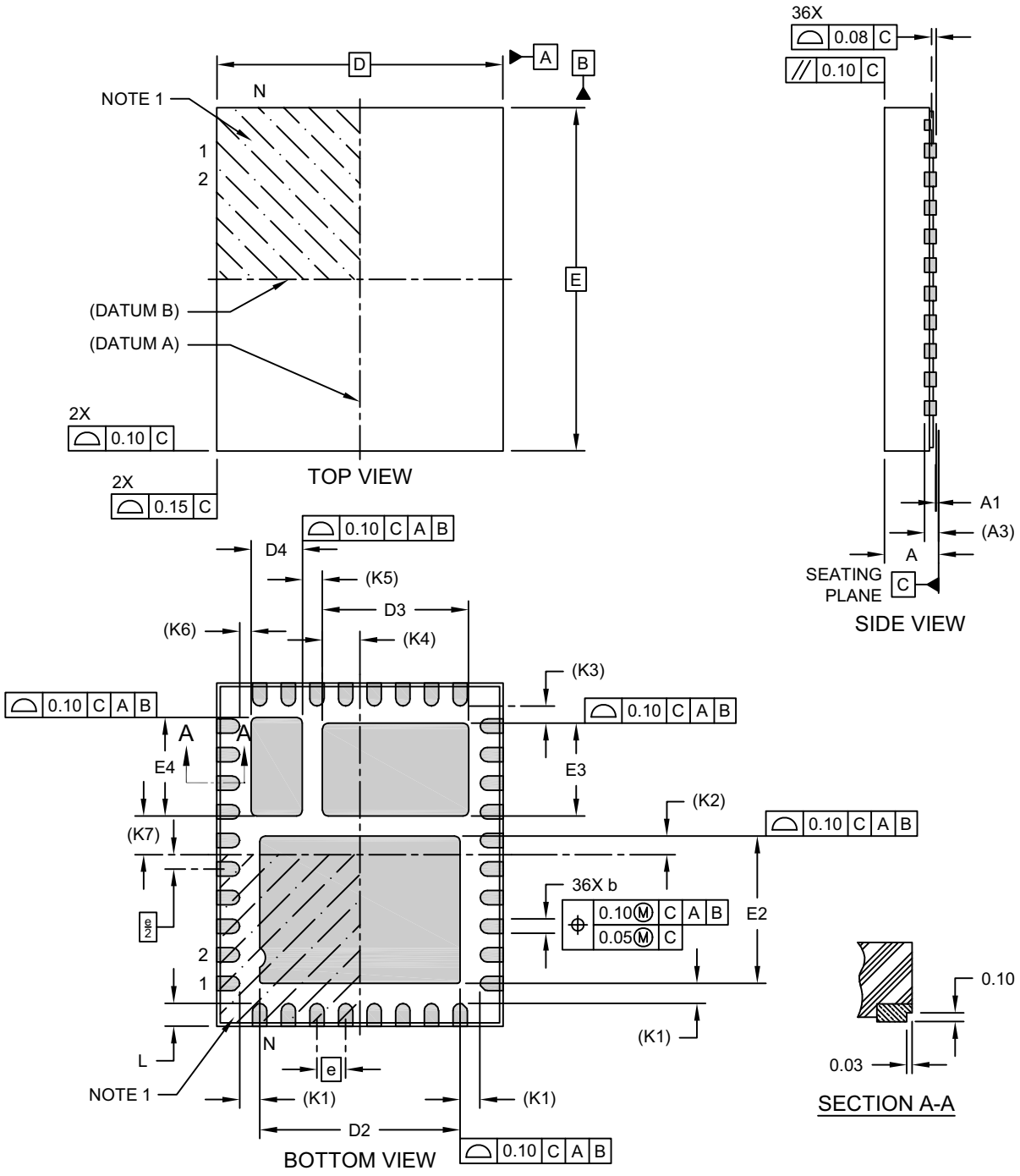
Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲,▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo. Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

36-Lead Very Thin Plastic Quad Flat, No Lead Package (QNA) - 5x6x0.9 mm Body [VQFN] With Mutiple Exposed Pads

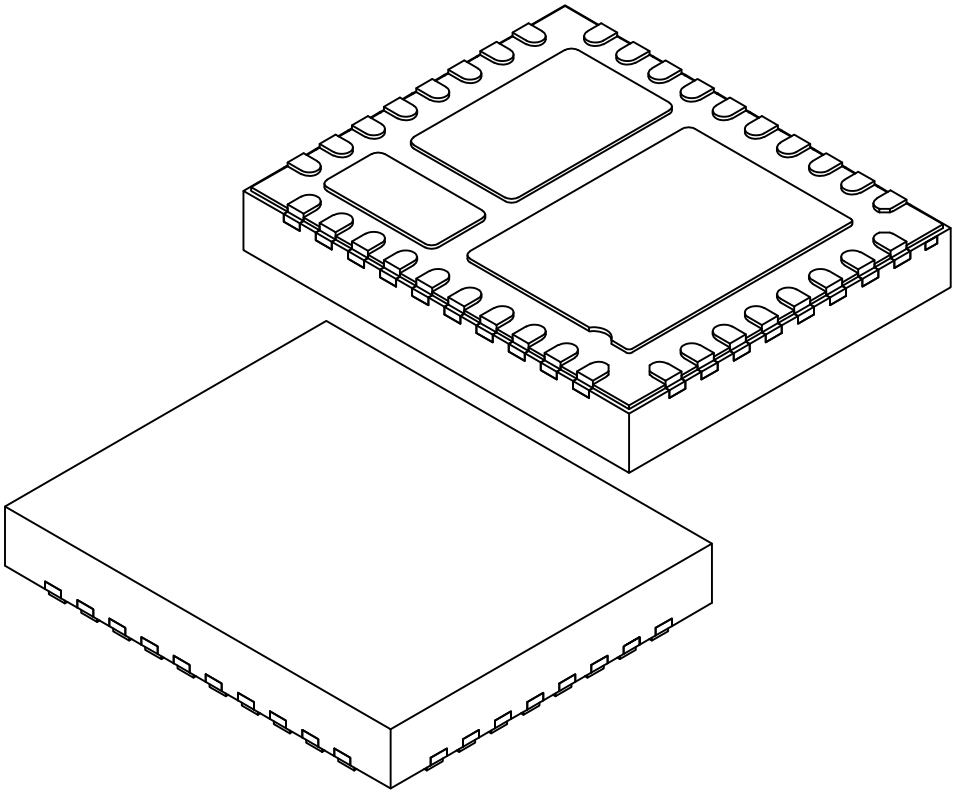
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1290 Rev A Sheet 1 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (QNA) - 5x6x0.9 mm Body [VQFN] With Mutiple Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		36	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	0.90
Standoff	A1	0.00	–	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.40	3.50	3.60
Exposed Pad Length	D3	2.455	2.555	2.655
Exposed Pad Length	D4	0.795	0.895	0.995
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	2.475	2.575	2.675
Exposed Pad Width	E3	1.525	1.625	1.725
Exposed Pad Width	E4	1.625	1.725	1.825
Terminal to Exposed Pad	K1		0.35 REF	
Center to Exposed Pad	K2		0.325 REF	
Terminal to Exposed Pad	K3		0.30 REF	
Center to Exposed Pad	K4		0.655 REF	
Pad to Pad	K5		0.123 REF	
Terminal to Exposed Pad	K6		0.20 REF	
Center to Exposed Pad	K7		0.675 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

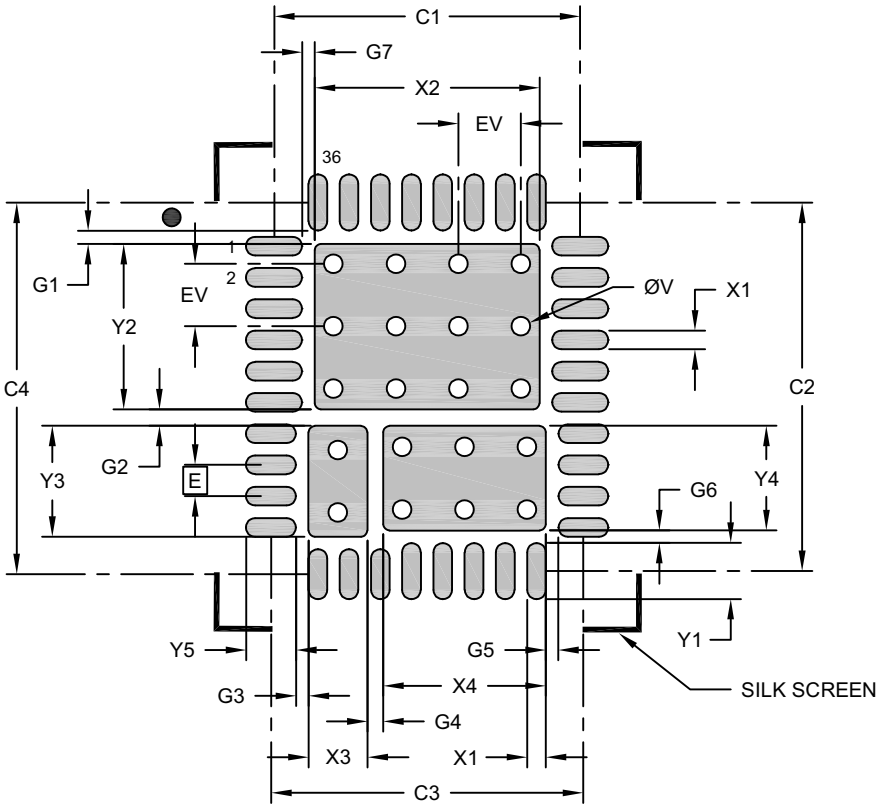
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1290 Rev A Sheet 2 of 2

36-Lead Very Thin Plastic Quad Flat, No Lead Package (QNA) - 5x6x0.9 mm Body [VQFN] With Mutiple Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		5.90	
Contact Pad Spacing	C3		5.00	
Contact Pad Spacing	C4		5.95	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.90
Contact Pad Length (Xnn)	Y5			0.80
Center Pad Width	X2			3.60
Center Pad Length	Y2			2.65
Center Pad Width	X3			0.95
Center Pad Length	Y3			1.78

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Center Pad Width	X4			2.61
Center Pad Length	Y4			1.68
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	
–	G1	0.21		
–	G2	0.26		
–	G3	0.20		
–	G4	0.25		
–	G5	0.20		
–	G6	0.20		
–	G7	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3290 Rev A

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X(1)	-X	/XXX
Device	Tape and Reel Option	Junction Temperature Range	Package

Devices:	MIC24066:	36V, 6A High Performance Switching Buck Regulator with Programmable Soft Start Time
	MIC24067:	36V, 6A High Performance Switching Buck Regulator with Programmable HLL/CCM Operation
Tape and Reel Option:	T	= 3300/Reel (for VQFN)
Junction Temperature Range:	E	= –40°C to +125°C, Extended Temperature Range
Package:	QNA	= 36-Lead 5 mm x 6 mm VQFN, Wettable Flank, Exposed Pad

Examples:

a) MIC24066T-E/QNA: 36V, 6A High Performance Switching Buck Regulator with Programmable Soft Start Time, 3300/Reel, -40°C to +125°C Extended Junction Temperature Range, 36-Lead 5 mm x 6 mm VQFN, Wettable Flank, Exposed Pad

b) MIC24067T-E/QNA: 36V, 6A High Performance Switching Buck Regulator with Programmable HLL/CCM Operation, 3300/Reel, -40°C to +125°C Extended Junction Temperature Range, 36-Lead 5 mm x 6 mm VQFN, Wettable Flank, Exposed Pad

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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