PGA411-Q1 Resolver Sensor Interface

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Resolver to Digital Converter (RDC)
- Exciter Preamplifier and Power Amplifier
- Exciter-Boost Power Supply With Spread Spectrum
- Analog Front-End
- Automatic Offset Calibration
- Type-II PI Controller Tracking Loop
- Parallel, Encoder, or SPI Data Output
- Analog Data Output
- SafeTI™ Semiconductor Component
  - Designed for Functional Safety Applications
  - Developed According to the Requirements of ISO 26262
- Automatic and Manual Phase Correction
- Sensor-Input Fault Detection
- Diagnostics Interrupt Output
- Internal and External Oscillator
- Analog and Logic Built-In Self-Test for Fault Detection
- 64-Pin HTQFP PowerPAD™ IC Package

2 Applications

- Motor Control
- HEV/EV Motor Inverters
- Electrical Power Steering
- Integrated Start-Stop Generators
- Servo Drives
- AC Drives
- Industrial Robots
- CNC Machinery
- Elevators/Lifts
- Injection Molding Machinery

3 Description

The PGA411-Q1 device is a resolver to digital converter, with an integrated exciter-amplifier and boost-regulator power supply, that is capable of both exciting and reading the sine and cosine angle from a resolver sensor. The integration of the exciter amplifier and boost supply with protection in the PGA411-Q1 device enables cost reductions of the bill of materials (BOM) and space reductions on the printed circuit board (PCB) because of the elimination of most external and passive components.

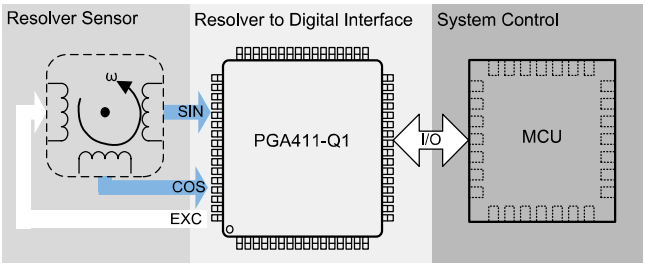
The PGA411-Q1 device also has an internal clock for generating a sine wave used for sensor excitation. The architecture of the analog front-end (AFE) allows the user to output 10 bits or 12 bits of resolution for the angle position and velocity. Because of high integration, the PGA411-Q1 device has diagnostics and protection on each internal block inside the device. The integrated diagnostics monitor can signal a fault condition through a dedicated pin which can be used as a MCU interrupt. These features allow flexibility in both resolver sensor choice and platform scalability. Additionally, the PGA411-Q1 was designed according to the requirements of ISO 26262 for functional safety applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PGA411-Q1	HTQFP (64)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified System Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2016) to Revision D — **Page**

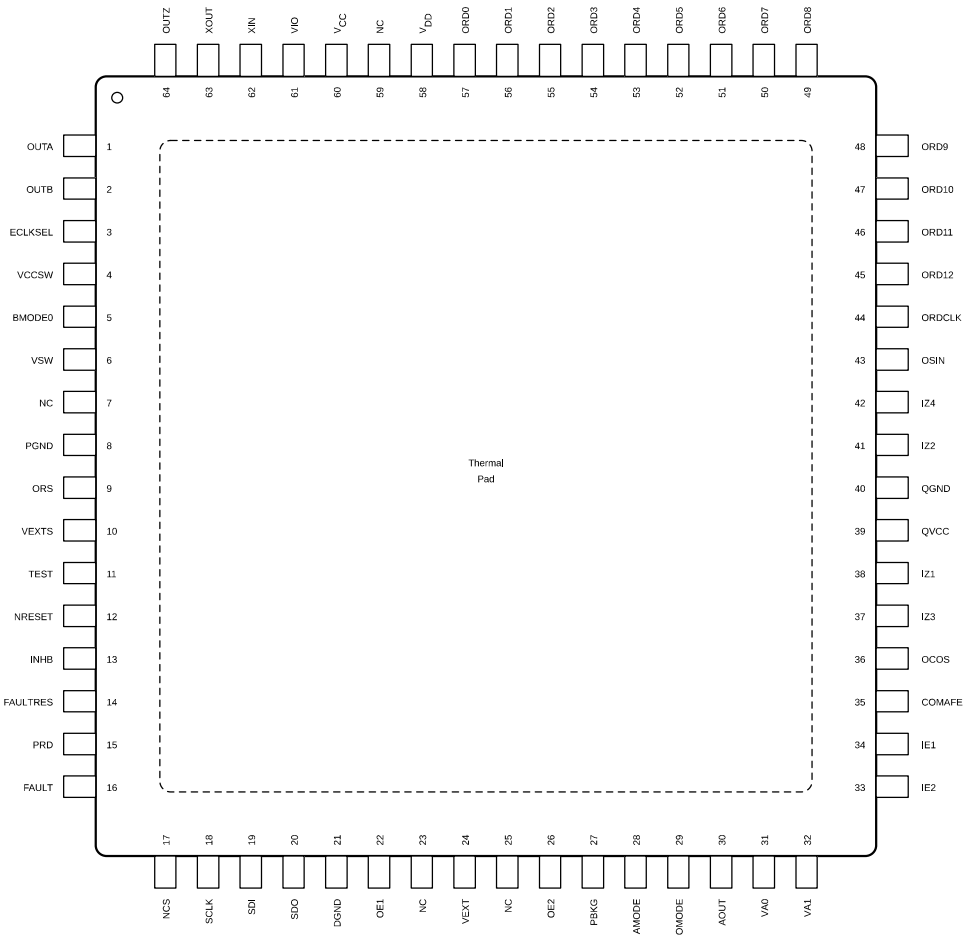
- Added the resistor to ground production statement in the *Analog Output* section and *Pin Functions* table and added the resistor to the *PGA411-Q1 Typical Application Diagram* image ... 40
- Changed the factory setting from 003Fh (00111111b) to 00CEh (11001110b) for the DEV_CLCRC register in the *User EEPROM Space SPI Mapping* table and in the *DEV_CLCRC Register* section ... 78
- Added a note to the *Power Supply Recommendations* section about the input supply when connected to V_{CC} and QVCC pins ... 94

Changes from Revision B (December 2015) to Revision C — **Page**

- Changed the device status from *Product Preview* to *Production Data* ... 1

5 Pin Configuration and Functions

PAP Package
64-Pin HTQFP With Exposed Thermal Pad
Top View



NC - No internal connection

Pin Functions

PIN		TYPE(1)	LOGIC INPUT OR OUTPUT	DESCRIPTION
NAME	NO.			
AMODE	28	I	Input	Accelerated mode select
AOUT	30	O	—	ORD (angle and velocity) analog output. Use for testing only, in production connect to ground.
BMODE0	5	I	Input	Resolution select, input low is 10-bit mode, input high is 12-bit mode
COMAFE	35	O	—	Common-mode output for the analog front-end (AFE)
DGND	21	P	—	Digital ground
ECLKSEL	3	I	Input	Clock select input
FAULT	16	O	Output	Fault-detection signal output (open drain structure)
FAULTRES	14	I	Input	Fault reset input (faults are reset when this pin is LOW)
IE1	34	I	—	Positive input to the AFE from the resolver exciter coil
IE2	33	I	—	Negative input to the AFE from the resolver exciter coil
INHB	13	I	Input	Inhibit function and output data hold

(1) I = input; O = output; I/O = input and output; P = power

Pin Functions (continued)

PIN		TYPE(1)	LOGIC INPUT OR OUTPUT	DESCRIPTION
NAME	NO.			
IZ1	38	I	—	Positive input to the AFE from the resolver cosine coil
IZ2	41	I	—	Positive input to the AFE from the resolver sine coil
IZ3	37	I	—	Negative input to the AFE from the resolver cosine coil
IZ4	42	I	—	Negative input to the AFE from the resolver sine coil
NC	7	I	—	Not connected (connect to ground)
	23			
	25			
	59			
NCS	17	I	Input	Chip select for the serial peripheral interface (SPI)
NRESET	12	I	Input	Reset input
OCOS	36	O	—	Resolver cosine output
OE1	22	O	—	Exciter-amplifier positive output
OE2	26	O	—	Exciter-amplifier negative output
OMODE	29	I	Input	Data output format select
ORD0	57	O	Output	Data output, 0 for parallel angle and velocity. Encoder output U
ORD1	56	O	Output	Data output, 1 for parallel angle and velocity. Encoder output V
ORD10	47	O	Output	Data output, 10 for parallel angle and velocity
ORD11	46	O	Output	Data output, 11 for parallel angle and velocity
ORD12	45	O	Output	Optional pin (data output, 12 for parallel angle and velocity - unused)
ORDCLK	44	O	Output	ORD Clock
ORD2	55	O	Output	Data output select 2 for parallel angle and velocity. Encoder output W
ORD3	54	O	Output	Data output select 3 for parallel angle and velocity. Encoder output U1
ORD4	53	O	Output	Data output select 4 for parallel angle and velocity. Encoder output V1
ORD5	52	O	Output	Data output select 5 for parallel angle and velocity. Encoder output W1
ORD6	51	O	Output	Data output select 6 for parallel angle and velocity. Encoder output A
ORD7	50	O	Output	Data output select 7 for parallel angle and velocity. Encoder output B
ORD8	49	O	Output	Data output select 8 for parallel angle and velocity. Encoder output Z
ORD9	48	O	Output	Data output select 9 for parallel angle and velocity
ORS	9	O	—	Exciter pre-amplifier output
OSIN	43	O	—	Resolver sine output
OUTA	1	O	Output	Incremental encoder, output A
OUTB	2	O	Output	Incremental encoder, output B
OUTZ	64	O	Output	Incremental encoder, output Z
PBKG	27	P	—	Ground
PGND	8	P	—	Power ground
PRD	15	O	Output	Data parity output
QGND	40	P	—	Power supply ground (quiet, used for AFE)
QVCC	39	P	—	Power supply input (quiet, used for AFE)
SCLK	18	I	Input	SPI clock
SDI	19	I	Input	SPI data input
SDO	20	O	Output	SPI data output
TEST	11	I/O	—	Test input and output (I/O). Texas Instruments reserved pin. Connect this pin to ground.
VA0	31	I	Input	Data output select 0 for angle and velocity
VA1	32	I	Input	Data output select 1 for angle and velocity
V_{CC}	60	P	—	Power supply input

Pin Functions (continued)

PIN NAME	PIN NO.	TYPE(1)	LOGIC INPUT OR OUTPUT	DESCRIPTION
VCCSW	4	P	—	Boost DC-DC inverter-supply input
V_{DD}	58	P	—	Output for the regulated digital power supply
VEXT	24	P	—	Exciter-amplifier supply input
VEXTS	10	I	—	Sense input for the boost supply and diagnostics.
VIO	61	P	—	Logic I/O voltage-level supply input
VSW	6	O	—	Boost DC-DC inverter FET drain
XIN	62	I	—	Crystal input
XOUT	63	O	—	Crystal output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VEXTS, OE1, OE2	–0.3	40	V
	VCCSW, VSW, VEXT, IZ1, IZ2, IZ3, IZ4	–0.3	20	
	V_{DD}, XIN, XOUT	–0.3	2	
	PGND, DGND, GND	–0.3	0.3	
	All Other pins	–0.3	5.5	
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 16, 17, 32, 33, 48, 49, and 64)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

				MIN	NOM	MAX	UNIT
V_{CC} / QVCC	Supply input voltage			4.75	5	5.25	V
V_{EXT}	Exciter supply input	VEXT	4-V_{RMS} mode	11	12	13	V
			7-V_{RMS} mode	14	15	16	
V_{CCSW}	Boost regulator input	VCCSW		4.75		8.5	V
V_{IO}	I/O supply input	VIO	V_{VIO} = 3.3 V	2.97	3.3	3.63	V
			V_{VIO} = 5 V	4.5	5	5.25	
V_{IZ}	Differential amplitude input	IZ1, IZ2, IZ3, IZ4)	(V_{IZ1} - V_{IZ3}); (V_{IZ2} - V_{IZ4}		2	3	V_{PP}
T_A	Operating fee-air temperature			–40		125	°C
T_J	Operating junction temperature			–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		PGA411-Q1 PAP (HTQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	10.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Exciter Output, Amplifier, and Power Supply Characteristics

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITER SIGNAL OUTPUT (PREAMPLIFIER)						
A_{EXC}	Exciter preamplifier gain	SPI programmable	1.15		1.9	V/V
f_{EXC}	Exciter output frequency range	SELFEXT = 0x00; System clock used; f_{OSC} = 20 MHz	9	10	11	kHz
		SELFEXT = 0x07; System clock used; f_{OSC} = 20 MHz	18	20	22	
V_{ORS}	Signal output voltage	ORS signal with respect to COMAFE voltage; GAIN = 1.5; C_{ORS} = 0.47 nF; I_{ORS} = ± 10 µA		1.5	2	V_{Peak}
V_{COMAFE}	Common-mode voltage output	COMAFE pin; C_{COMAFE} = 10 nF	2.25	2.5	2.75	V
EXCITER POWER SUPPLY						
V_{EXCPS}	Exciter power-supply output voltage	MODEVEXT = 0x00; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 4.75 V; nBOOST_FF = 1	8	10	12	V
		MODEVEXT = 0x01; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 4.75 V; nBOOST_FF = 1	9	11	13	
		MODEVEXT = 0x02; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 5 V; nBOOST_FF = 1	10	12	14	
		MODEVEXT = 0x03; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 5 V; nBOOST_FF = 1	11	13	15	
		MODEVEXT = 0x04; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 5 V; nBOOST_FF = 1	12	14	16	
		MODEVEXT = 0x05; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 6 V; nBOOST_FF = 1	13	15	17	
		MODEVEXT = 0x06; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 6 V; nBOOST_FF = 1	14	16	18	
		MODEVEXT = 0x07; I_{EXTPS} = 150 mA; V_{CCSW} ≥ 7 V; nBOOST_FF = 1	15	17	19	
f_{EXTPS}	Exciter power-supply switching frequency	With 10% spread spectrum		414		kHz
L_{EXCPS}	Exciter power-supply inductor range			56		µH
C_{EXCPS}	Exciter power-supply capacitor range			10		µF
EXCITER AMPLIFIER						

Exciter Output, Amplifier, and Power Supply Characteristics (continued)

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{EXCO}	Exciter-amplifier differential output voltage	4-V_{RMS} mode; EXTOUT_GL = 0x00	7.12	8.38		V_{PP}
		4-V_{RMS} mode; EXTOUT_GL = 0x01	7.44	8.75		
		4-V_{RMS} mode; EXTOUT_GL = 0x02	7.74	9.11		
		4-V_{RMS} mode; EXTOUT_GL = 0x03	8.05	9.47		
		4-V_{RMS} mode; EXTOUT_GL = 0x04	8.36	9.84		
		4-V_{RMS} mode; EXTOUT_GL = 0x05	8.67	10.2		
		4-V_{RMS} mode; EXTOUT_GL = 0x06	8.98	10.57		
		4-V_{RMS} mode; EXTOUT_GL = 0x07	9.29	10.93		
		4-V_{RMS} mode; EXTOUT_GL = 0x08	9.61	11.3		
		4-V_{RMS} mode; EXTOUT_GL = 0x09	9.91	11.66		
		4-V_{RMS} mode; EXTOUT_GL = 0x0A	10.23	12.03		
		4-V_{RMS} mode; EXTOUT_GL = 0x0B	10.53	12.39		
		4-V_{RMS} mode; EXTOUT_GL = 0x0C	10.84	12.75		
		4-V_{RMS} mode; EXTOUT_GL = 0x0D	11.15	13.12		
		4-V_{RMS} mode; EXTOUT_GL = 0x0E	11.46	13.48		
		4-V_{RMS} mode; EXTOUT_GL = 0x0F	11.77	13.85		
		7-V_{RMS} mode; EXTOUT_GL = 0x00	12.49	14.69		
		7-V_{RMS} mode; EXTOUT_GL = 0x01	13.03	15.33		
		7-V_{RMS} mode; EXTOUT_GL = 0x02	13.57	15.97		
		7-V_{RMS} mode; EXTOUT_GL = 0x03	14.12	16.61		
		7-V_{RMS} mode; EXTOUT_GL = 0x04	14.65	17.24		
		7-V_{RMS} mode; EXTOUT_GL = 0x05	15.20	17.88		
		7-V_{RMS} mode; EXTOUT_GL = 0x06	15.74	18.52		
		7-V_{RMS} mode; EXTOUT_GL = 0x07	16.29	19.16		
		7-V_{RMS} mode; EXTOUT_GL = 0x08	16.83	19.8		
		7-V_{RMS} mode; EXTOUT_GL = 0x09	17.37	20.44		
		7-V_{RMS} mode; EXTOUT_GL = 0x0A	17.92	21.08		
		7-V_{RMS} mode; EXTOUT_GL = 0x0B	18.46	21.72		
		7-V_{RMS} mode; EXTOUT_GL = 0x0C	19	22.35		
		7-V_{RMS} mode; EXTOUT_GL = 0x0D	19.54	22.99		
		7-V_{RMS} mode; EXTOUT_GL = 0x0E	20.09	23.63		
		7-V_{RMS} mode; EXTOUT_GL = 0x0F	20.63	24.27		
V_{REXC}	Exciter-amplifier reference voltage	SPI programmable using EXTOUT bits	0.5		2	V
I_{QEXC}	Exciter-amplifier quiescent current		1		15	mA
I_{EXCO}	Exciter amplifier output current range	(OE1-OE2) = 20 V_{PP}			145	mA
I_{EXCREV}	Exciter amplifier output reverse current	Reverse current to VEXT, OE1 or OE2 shorted to battery (battery must be greater than 180% of VEXT)			15	mA

6.6 Analog Front-End Characteristics

Over operating free-air temperature range, V_{IN} = 4.5 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITER SIGNAL MONITOR (IE1, IE2)						
V_{IECM}	Input voltage range		0.5		4.5	V
f_{IEIN}	Input frequency range		8		24	kHz
R_{EIN}	Input resistance		30	40	50	kΩ
SIN AND COS INPUT GAIN AMPLIFIER (IZ1, IZ3), (IZ2, IZ4), (OSIN, OCOS)						
$S_{GAIN}(C_{GAIN})$	SIN and COS Amplifier Gain	COMAFE = 2.5 V; GAINCOS = GAINSIN = 0x00	0.735	0.75	0.765	V/V
		COMAFE = 2.5 V; GAINCOS = GAINSIN = 0x01	0.98	1	1.02	
		COMAFE = 2.5 V; GAINCOS = GAINSIN = 0x02	2.205	2.25	2.295	
		COMAFE = 2.5 V; GAINCOS = GAINSIN = 0x03	3.43	3.5	3.57	
V_{IZx}	Differential IZx input voltage range (pk-pk)	S_{GAIN} = 0.75; C_{GAIN} = 0.75 COMAFE=2.5 V			3	V
I_{IZx}	IZx input current range	At V_{IZX} = 1 V and 4 V	–150		150	µA

Analog Front-End Characteristics (continued)

Over operating free-air temperature range, V_{IN} = 4.5 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{IZx}	IZx input resistance (internal)		15	20	25	kΩ
$CMRR_{SIN(COS)}$	Commond-mode rejection ratio			45		dB
PSRRsin(cos)	Supply rejection ratio			60		dB
$V_{OS}(V_{OC})$	Output voltage range	OSIN pin; OCOS pin; I_{OUT} = 10 µA	0.5		4.5	V
V_{COMAFE}	Common-mode voltage output	COMAFE pin; I_{OUT} = 10 µA	2.375	2.5	2.625	V

6.7 Digital Tracking Loop Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
O_{MODE1}	Output data resolution 1	BMODE0=L; BMODE1=L		10		bit
O_{MODE2}	Output data resolution 2	BMODE0=H; BMODE1=L		12		bit
TR1	Maximum tracking rate 1	10-bit mode		200 000		rpm
TR2	Maximum tracking rate 2	12-bit mode		72 000		rpm
ACL1	Maximum angular acceleration 1	10-bit mode		200 000		rad / s^2
ACL2	Maximum angular acceleration 2	12-bit mode		50 000		rad / s^2
ACC1	Maximum angular accuracy 1 (1)	10-bit mode		±10.56		arc min
ACC2	Maximum angular accuracy 2 (1)	12-bit mode		±2.64		arc min
INL1	Integral linearity 1	10-bit mode; OHYS = 1	–2		2	LSB
INL2	Integral linearity 2	12-bit mode; OHYS = 1	–8		8	LSB
DNL1	Differential linearity 1	10-bit mode; OHYS = 1	–1		1	LSB
DNL2	Differential linearity 2	12-bit mode; OHYS = 1	–2		3	LSB
t_{DLT1}	Settling time 1 (2)	AMODE=H; 180-degree step input; 10-bit mode	0.1	1.5	3.5	ms
		AMODE=H; 180-degree step input; 12-bit mode	0.1	3	7	
t_{DLT2}	Settling time 2 (2)	AMODE=L; 180-degree step input; 10-bit mode	11	15	18	ms
		AMODE=L; 180-degree step input; 12-bit mode	45	60	65	
t_{RESP}	Phase delay response	f_{IN} = 10 000 rpm	–0.4		0.4	deg
Ph_{ADJ}	Exciter to SIN and COS phase adjustment range	Manual mode; f_{EXC}= 10 kHz	–44.5		44.5	deg
		Manual mode; f_{EXC}= 20 kHz	–89.2		89.2	
		Auto mode	–89.2		89.2	
Ph_{ADJ_STEP}	Exciter to SIN and COS phase adjustment range step size	Manual mode; f_{EXC}= 10 kHz		1.44		deg
		Manual mode; f_{EXC}= 20 kHz		2.88		
		Auto mode; f_{EXC}= 10 kHz		0.36		
		Auto mode; f_{EXC}= 20 kHz		0.72		

(1) Refers to a differential angle change.
(2) Digital Tracking Loop Settings: Dki = 0x4; Dkp = 0x4; Mkp = 0x2 (Mkp used only when AMODE = H)

6.8 Diagnostics Monitor Characteristics

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC_{OV}	V_{CC} overvoltage threshold	SPI flag; Exciter disabled	5.4	5.75	5.92	V
VCC_{UV}	V_{CC} undervoltage threshold	NPOR asserted	4.28	4.41	4.54	V
$t_{VCCOVUV}$	V_{CC} overvoltage and undervoltage deglitch time		4.2	5.2	6.2	µs
V_{DD} REGULATOR						
V_{VDD}	Digital functional voltage range	V_{DD} pin	1.623		1.984	V
VDD_{OV}	V_{DD} overvoltage threshold	SPI flag; Exciter disabled	2	2.2	2.4	V
VDD_{UV}	V_{DD} undervoltage threshold	SPI flag; NPOR asserted	1.23	1.35	1.53	V
$t_{VDDOVUV}$	V_{DD} overvoltage and undervoltage deglitch time		4.2	5.2	6.2	µs
I_{VDDLIM}	V_{DD} current limit	V_{CC} = 4.75 to 5.25 V; SPI flag; Maximum current draw from V_{DD} for external consumption is 10 mA	10	100	250	mA

Diagnostics Monitor Characteristics (continued)

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{VDDOC}	V_{DD} overcurrent deglitch time		4.2	5.2	6.2	µs
EXCITER POWER SUPPLY						
OV_{EXCPS}	Exciter power-supply overvoltage threshold	SPI flag	110	115	122	% V_{EXCPS}
UV_{EXCPS}	Exciter power-supply undervoltage threshold		75	82.5	85	% V_{EXCPS}
COV_{EXCPS}	Critical overvoltage threshold	Power supply disabled			180	% V_{EXCPS}
CUV_{EXCPS}	Critical undervoltage threshold	Power supply disabled	15			% V_{EXCPS}
t_{EXCPS}	Exciter power-supply fault deglitch time		9.2	10.2	11.2	us
EXCITER AMPLIFIER						
SOV_{EXC}	Single-ended overvoltage	Exciter disabled	110	115	120	%V_{EXC}
OV_{EXC}	Differential overvoltage threshold	4 Vrms mode; Exciter disabled; SPI flag	6.8	8	9.2	V
		7 Vrms mode; Exciter disabled; SPI flag	11.9	14	16.1	
UV_{EXC}	Differential undervoltage threshold	4 Vrms mode; Exciter disabled; SPI flag	2.55	3	3.45	V
		7 Vrms mode; Exciter disabled; SPI flag	5.1	6	6.9	
$I_{EXCOLIM(OE1-OE2)}$	Exciter amplifier output current-limit high level (from OE1 into OE2)	EXTILIMTH_H1_2 = 0x0	100	150	190	mA
		EXTILIMTH_H1_2 = 0x1	110	165	210	
		EXTILIMTH_H1_2 = 0x2	120	180	230	
		EXTILIMTH_H1_2 = 0x3	130	200	250	
		EXTILIMTH_H1_2 = 0x4	150	225	281	
		EXTILIMTH_H1_2 = 0x5	170	260	320	
		EXTILIMTH_H1_2 = 0x6	200	300	370	
		EXTILIMTH_H1_2 = 0x7	230	360	440	
$I_{EXCOLIM(OE2-OE1)}$	Exciter amplifier output current-limit low level (from OE2 into OE1)	EXTILIMTH_L1_2 = 0x0	90	140	181	mA
		EXTILIMTH_L1_2 = 0x1	100	150	200	
		EXTILIMTH_L1_2 = 0x2	110	165	220	
		EXTILIMTH_L1_2 = 0x3	120	180	231	
		EXTILIMTH_L1_2 = 0x4	140	200	260	
		EXTILIMTH_L1_2 = 0x5	160	230	550	
		EXTILIMTH_L1_2 = 0x6	180	550	830	
		EXTILIMTH_L1_2 = 0x7	210	550	830	
t_{EXCOV}	Exciter-amplifier overvoltage deglitch time	SPI programmable using EXTOVT bits	1.2		15.2	µs
t_{EXCUV}	Exciter-amplifier undervoltage deglitch time	EXTUV_CFG=10; SPI programmable using EXTUVT bits	1.2		15.2	µs
		EXTUV_CFG=0x; SPI programmable using EXTUVT bits	55		405	µs
$t_{EXCOLIM}$	Exciter-amplifier output current-limit deglitch time		4.2	5.2	6.2	µs
ANALOG FRONT-END						
OV_{IZX}	Input overvoltage threshold	IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZH = 0x0	72	75	78	%V_{CC}
		IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZH = 0x1	77	80	83	
		IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZH = 0x2	82	85	88	
		IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZH = 0x3	87	90	93	
UV_{IZX}	Input undervoltage threshold	IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZL = 0x0	22	25	28	%V_{CC}
		IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZL = 0x1	17	20	23	
		IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZL = 0x2	12	15	18	
		IZ1, IZ2, IZ3, IZ4 pins; Reported by SPI flags; OVIZL = 0x3	7	10	13	
t_{OVUV_IZX}	Input overvoltage and undervoltage deglitch time	SPI programmable using IZTHL bits(Independent)	1.2		15.2	µs
V_{SHRTP}	Positive input short-circuit voltage	OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x0	50.4	52.5	54.6	%V_{CC}
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x1	52.8	55	57.2	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x2	55.2	57.5	59.8	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x3	57.6	60	62.4	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x4	60	62.5	65	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x5	62.4	65	67.6	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x6	64.8	67.5	70.2	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTH = 0x7	67.2	70	72.8	

Diagnostics Monitor Characteristics (continued)

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SHRTN}	Negative input short-circuit voltage	OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x0	45.6	47.5	49.4	$\%V_{CC}$
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x1	43.2	45	46.8	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x2	40.8	42.5	44.2	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x3	38.4	40	41.6	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x4	36	37.5	39	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x5	33.6	35	36.4	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x6	31.2	32.5	33.8	
		OSIN, OCOS pins; Reported by SPI flags; OSHORTL = 0x7	28.8	30	31.2	
V_{OPNP}	Positive input open-circuit voltage	OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x0	72	75	78	$\%V_{CC}$
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x1	74.4	77.5	80.6	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x2	76.8	80	83.2	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x3	79.2	82.5	85.8	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x4	81.6	85	88.4	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x5	84	87.5	91	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x6	86.4	90	93.6	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHH = 0x7	88.8	92.5	96.2	
V_{OPNN}	Negative input open-circuit voltage	OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x0	22.5	25	27.5	$\%V_{CC}$
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x1	20.3	22.5	24.8	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x2	18	20	22	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x3	15.8	17.5	19.3	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x4	13.5	15	16.5	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x5	11.3	12.5	13.8	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x6	9	10	11	
		OSIN, OCOS pins; Reported by SPI flags; OOPENTHL = 0x7	6.8	7.5	8.3	
t_{SHRT}	Input short deglitch time	SPI programmable using TSHORT bits (Each setting has ±10-µs tolerance)	35		140	µs
t_{OPN}	Input open deglitch time	SPI programmable using TOPEN bits (Each setting has ±10-µs tolerance)	35		140	µs
D_{ERRP_IEX}	Exciter signal-monitor positive duty error	(IE1 - IE2) signal; Reported by SPI flag	80			$\%f_{EXC}$
D_{ERRN_IEX}	Exciter signal-monitor negative duty error	(IE1 - IE2) signal; Reported by SPI flag			20	$\%f_{EXC}$
t_{ERR_IEX}	Exciter signal-monitor duty-error deglitch	SPI programmable using TEXTMON bits (Each setting has ±10-µs tolerance)	35		140	µs
VM_{SENH}	Input integrity check high threshold	IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x0	2.44	2.6	2.73	V
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x1	2.59	2.75	2.88	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x2	2.73	2.9	3.04	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x3	2.87	3.05	3.19	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x4	3.01	3.2	3.35	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x5	3.15	3.35	3.5	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x6	3.29	3.5	3.66	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENH = 0x7	3.42	3.65	3.81	

Diagnostics Monitor Characteristics (continued)

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VM_{SENL}	Input integrity check low threshold	IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x0	2.27	2.4	2.52	V
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x1	2.12	2.25	2.37	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x2	1.98	2.1	2.21	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x3	1.84	1.95	2.06	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x4	1.7	1.8	1.9	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x5	1.55	1.65	1.75	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x6	1.41	1.50	1.6	
		IZ1, IZ2, IZ3, IZ4 pins; V_{CC} = 5 V; This threshold is a percentage of V_{CC}; Reported by SPI flags; DVMSENHL = 0x7	1.26	1.35	1.44	
t_{SENHL}	Input integrity check deglitch time		4.2	5.2	6.2	µs
DIGITAL TRACKING LOOP						
V_{LERRH}	Tracking-loop error signal high threshold	Reported by SPI flag; SPI programmable	0.1		0.8	V
V_{LERRL}	Tracking-loop error signal low threshold	Reported by SPI flag; SPI programmable	–0.8		-0.1	V
t_{LERR}	Tracking-loop error window	SPI programmable using TRDHL bits; AMODE = H	2		8	ms
		SPI programmable using TRDHL bits; AMODE = L	90		180	ms
THERMAL PROTECTION						
TSD_{EXC_WR}	Exciter thermal warning	SPI flag	125		155	°C
TSD_{EXC_SD}	Exciter thermal shutdown	Exciter disabled ; SPI flag	155	175	200	°C
TSD_{VDD_WR}	V_{DD} regulator thermal warning	SPI flag	125		155	°C
TSD_{VDD_SD}	V_{DD} regulator thermal shutdown	NPOR asserted	155	175	200	°C

6.9 V_{DD} Regulator Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDD}	V_{DD} output voltage		1.69	1.8	1.91	V
I_{VDD}	V_{DD} output current range				10	mA
$Lr1_{VDD}$	Line regulation	I_{VDD} = 0 to 10 mA; Exciter power-supply enabled	90		110	$\%V_{VDD}$
$Lr2_{VDD}$	Load regulation	I_{VDD} = 0 to 10 mA; V_{CC} = 4.5 to 5.5 V	90		110	$\%V_{VDD}$
C_{VDD}	V_{DD} external capacity	V_{DD} pin		100		nF

6.10 Digital I/O Characteristics

V_{CC} = 4.75 to 5.25 V; V_{VIO} = 3.3 to 5 V T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC OUTPUT						
V_{OH}	Output-level high logic	I_{LOAD} = 3 mA	90			$\%V_{VIO}$
V_{OL}	Output-level low logic	I_{LOAD} = - 3 mA			10	$\%V_{VIO}$
T_{ODLY_H}	Transition low-to-high delay time	C_{LOAD} = 50 pF(1)			40	ns
T_{ODLY_L}	Transition high-to-low delay time	C_{LOAD} = 50 pF(1)			40	ns
R_{OPD}	Internal pulldown resistance	V_{PIN} = 5 V	40	100	160	kΩ
LOGIC OUTPUT (OPEN DRAIN)						
V_{OLOD}	Output-level low logic	R_{EXT_PU} = 4.7 kΩ			400	mv
$T_{ODLY\_H\_OD}$	Transition low-to-high delay time	R_{EXT_PU} = 4.7 kΩ; C_{LOAD} = 50 pF(1)			200	µs
$T_{ODLY\_L\_OD}$	Transition high-to-low delay time	R_{EXT_PU} = 4.7 kΩ; C_{LOAD} = 50 pF(1)			1	µs
R_{PUOD}	Internal pullup resistance	FAULT pin; V_{PIN} = 0 V	40	100	160	kΩ
LOGIC INPUT						
V_{IH}	High logic-level input threshold		70			$\%V_{VIO}$
V_{IL}	Low logic-level input threshold				30	$\%V_{VIO}$

(1) Parameter specified by design.

Digital I/O Characteristics (continued)

V_{CC} = 4.75 to 5.25 V; V_{VIO} = 3.3 to 5 V T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{IDLY_H}	Transition low-to-high delay time(1)				40	ns
T_{IDLY_L}	Transition high-to-low delay time(1)				40	ns
R_{PD}	Internal pulldown resistance	V_{PIN} = 5 V	40	100	160	kΩ
R_{PU}	Internal pullup resistance	NCS pin; V_{PIN}= 0 V	40	100	160	kΩ

6.11 Oscillator Characteristics

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSC_E}	External oscillator frequency	20-MHz XTAL; ECLKSEL = H(1)		20		MHz
f_{OSC_I}	Internal oscillator frequency		18.4	20	21.6	MHz
E_{OSC}	System-clock out-of-range threshold	NPOR asserted	–30%		40%	
t_{POR}	Device start-up time	From VDD_UV = L(1)			1.5	ms

(1) Parameter specified by design

6.12 Output Data Interface Characteristics

Over operating free-air temperature range, V_{IN} = 4.5 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PARALLEL DIGITAL OUTPUT (ORD[11:0])						
$RATE_{ORD\_DATA}$	Parallel-data output rate			10		MHz
t_{ORD_DATA}	Parallel-data output update time			100		ns
EMULATED ENCODER OUTPUT (OUTA, OUTB, OUTZ, OUTU, OUTV, OUTW, OUTU1, OUTV1, OUTW1)						
ABZ_{10BIT_RES}	OUTA and OUTB resolution in 10-bit mode			256		pulses/rotation
ABZ_{12BIT_REZ}	OUTA and OUTB resolution in 12-bit mode			1024		pulses/rotation
ABZ_{OUTZ}	OUTZ resolution (10-bit mode or 12-bit mode)			1		pulses/rotation
ABZ_{RPM}	Maximum rotation supported by emulated encoder mode				200 000	RPM
t_{ABZ}	Rise and fall times of emulated encoder outputs			160	200	us
ANALOG OUTPUT MONITOR						
RES_{MON_DAC}	Analog output DAC resolution			10		Bit
V_{MON_DAC}	Analog output-voltage range		0.5		4.5	V

6.13 SPI Interface Timing Requirements

V_{CC} = 4.75 to 5.25 V, T_A = –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
f_{SPI}	SPI clock (SCLK) frequency	V_{VIO} = 3.3 V; C_{SDO} = 50 pF; SPI clock tolerance = ± 10%			8	MHz
t_{whigh}	High time: SCLK logic high time duration		55			ns
t_{wlow}	Low time: SCLK logic low time duration		55			ns
t_{su_cs}	NCS setup time: Time delay between falling edge of NCS and rising edge of SCLK		55			ns
t_{h_cs}	Hold time: Time between the falling edge of SCLK and rising edge of NCS		55			ns
t_{pd_soen}	Delay time: Time delay from falling edge of NCS to data valid at SDO				55	ns
t_{pd_sodis}	Delay time: Time delay from rising edge of NCS to SDO transition to tri-state				55	ns
t_{su_si}	SDI setup time: Setup time of SDI before the falling edge of SCLK		15			ns
t_{h_si}	Hold time: Time between the falling edge of SCLK to SDI valid		15			ns
t_{pd_so}	Propagation delay from rising edge of SCLK to SDO	C_{SDO} = 50 pF			45	ns
t_{w_cs}	SPI transfer inactive time (time between two transfers) during which NCS must remain high		200			ns

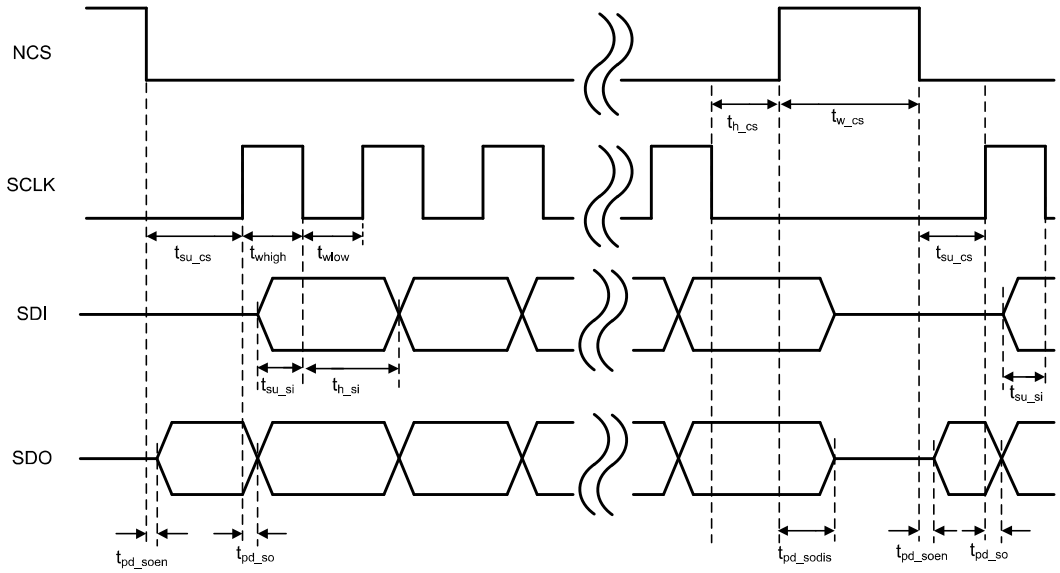


Figure 1. SPI Timing Diagram

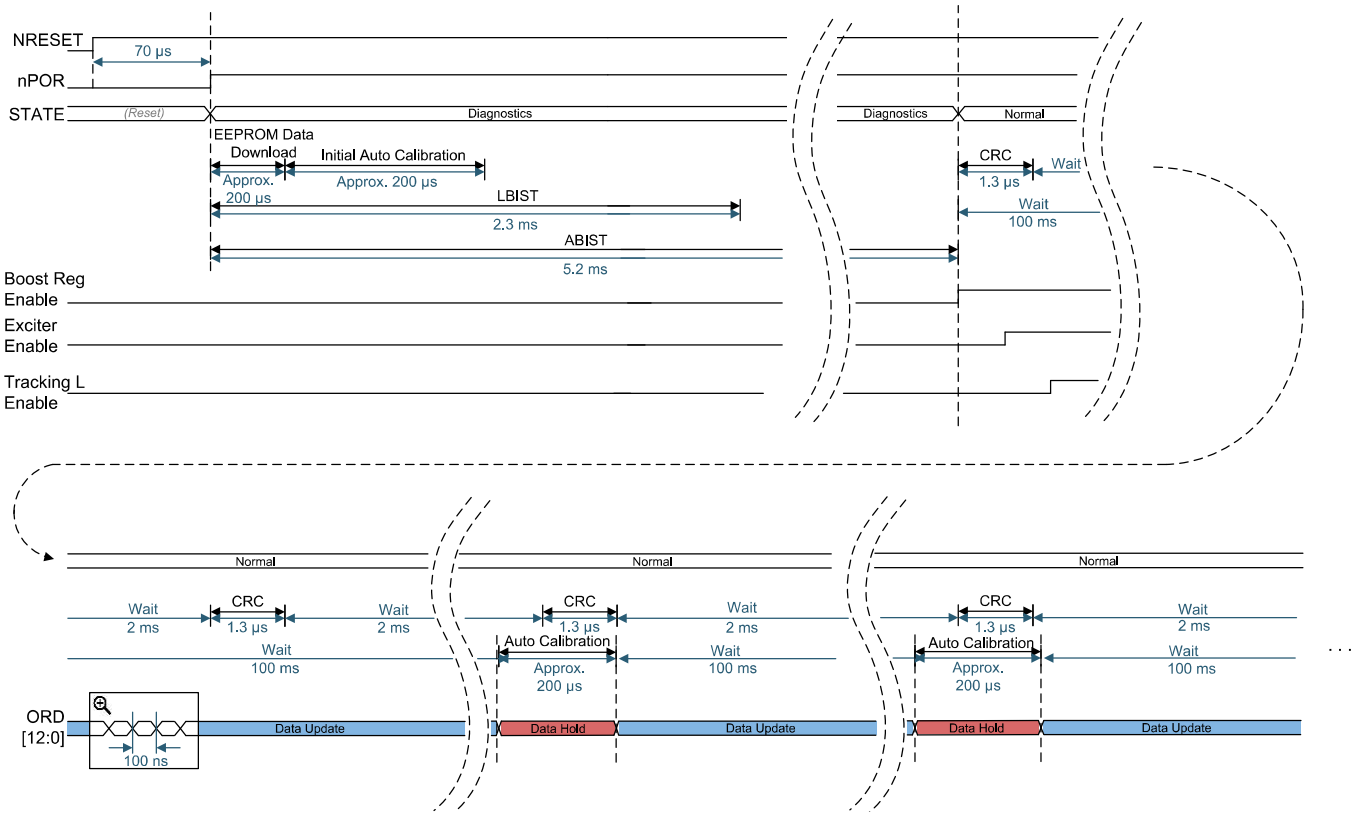
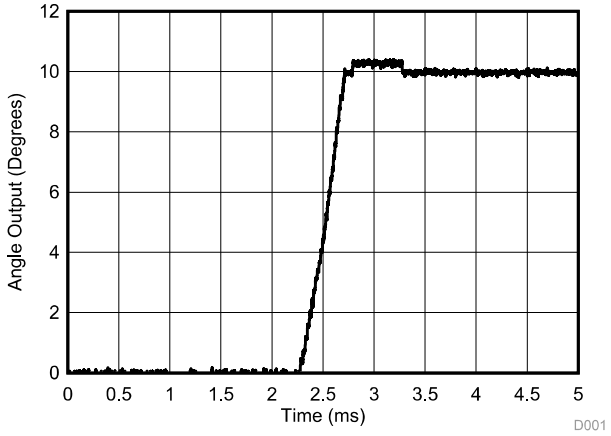


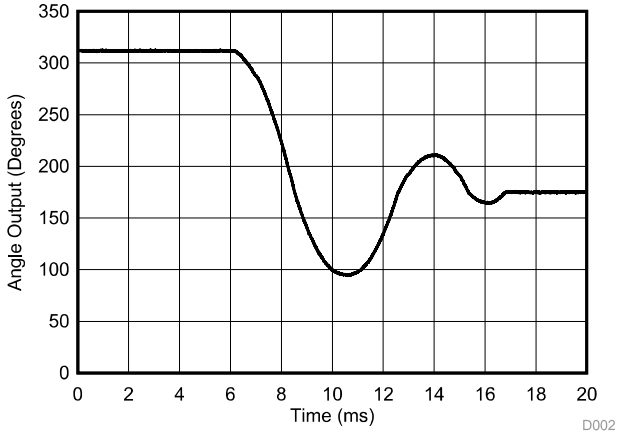
Figure 2. Power-Up Timing Diagram

6.14 Typical Characteristics



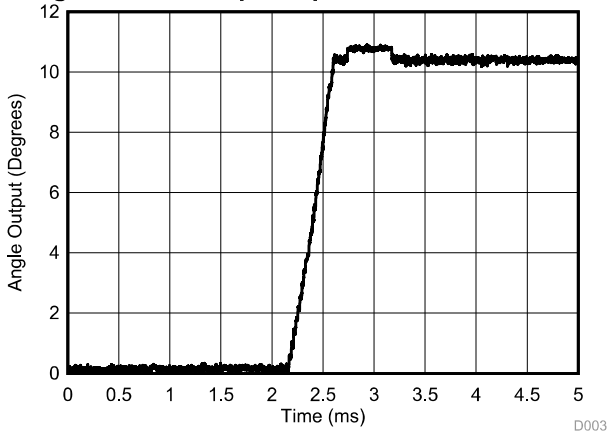
AMODE = 0

Figure 3. 10° Step Response in 10-Bit Mode



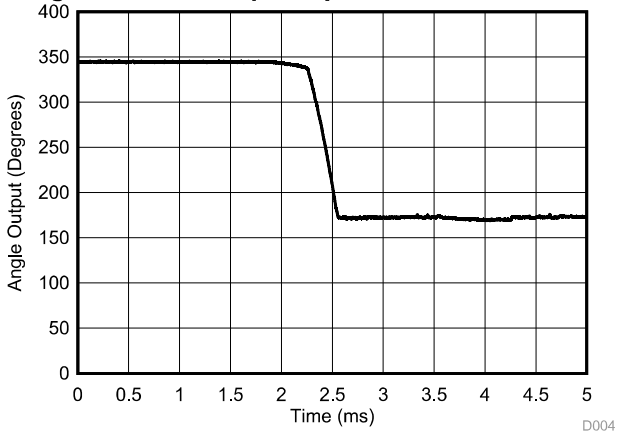
AMODE = 0

Figure 4. 180° Step Response in 10-Bit Mode



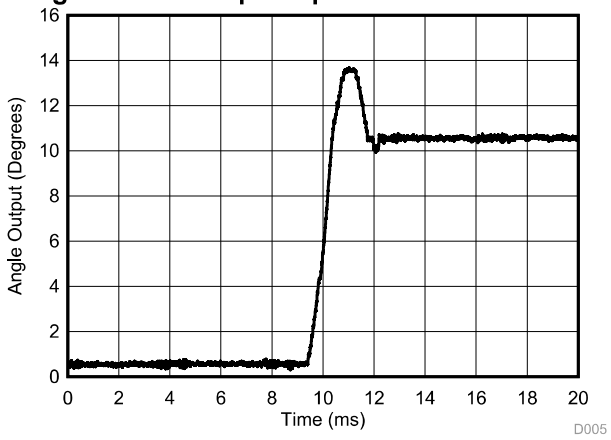
AMODE = 1

Figure 5. 10° Step Response in 10-Bit Mode



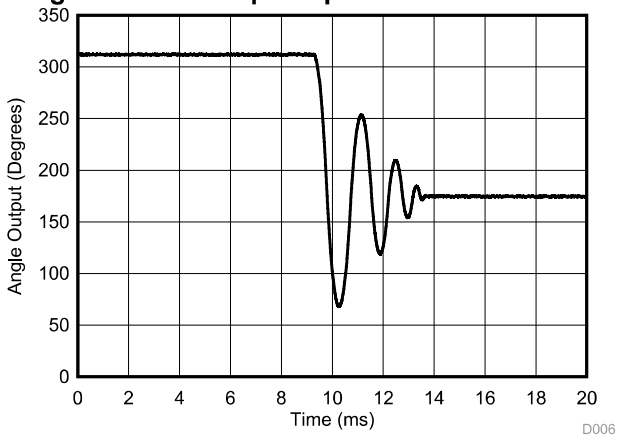
AMODE = 1

Figure 6. 180° Step Response in 10-Bit Mode



AMODE = 0

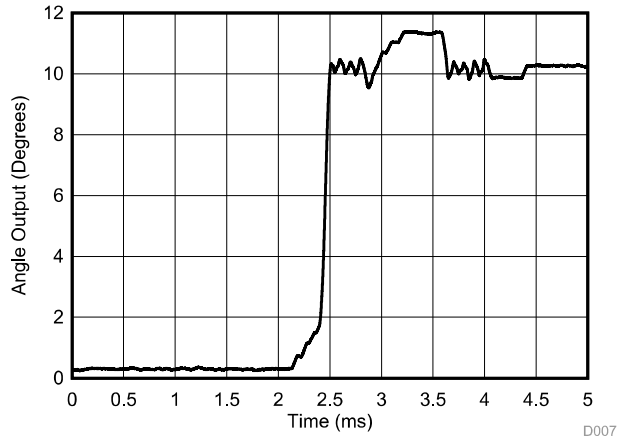
Figure 7. 10° Step Response in 12-Bit Mode



AMODE = 0

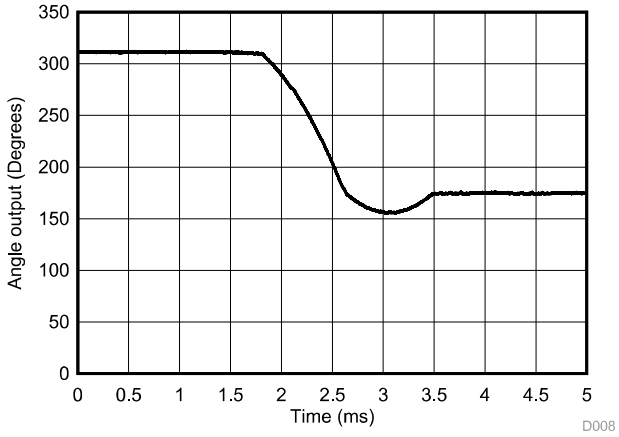
Figure 8. 180° Step Response in 12-Bit Mode

Typical Characteristics (continued)



AMODE = 1

Figure 9. 10° Step Response in 12-Bit Mode



AMODE = 1

Figure 10. 180° Step Response in 12-Bit Mode

7 Detailed Description

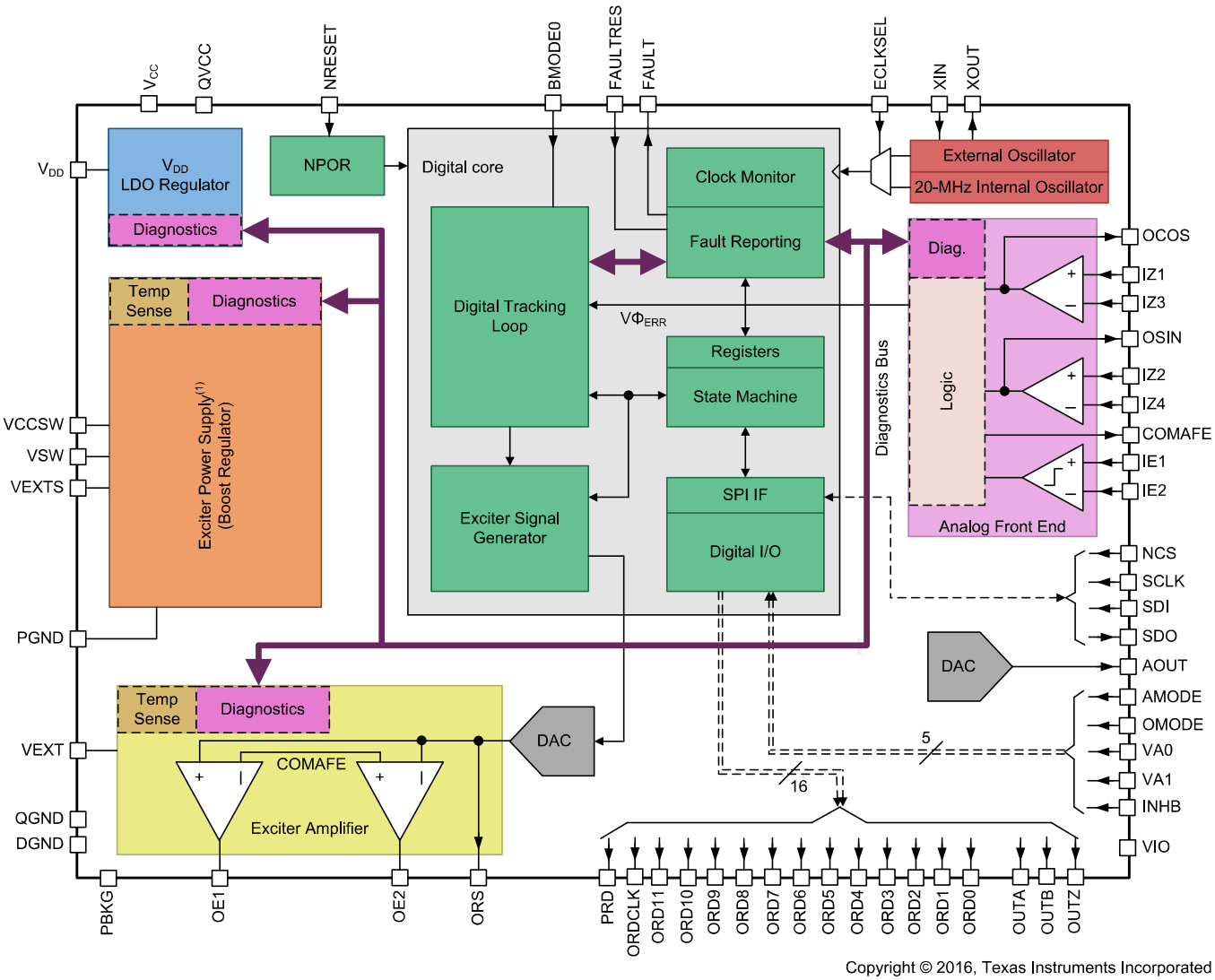
7.1 Overview

The PGA411-Q1 device is a resolver sensor interface device with an integrated exciter amplifier and boost power supply. The PGA411-Q1 device is capable of running with either 10-bit or 12-bit resolution. The internal boost power supply for the exciter can be used from 10 V to 17 V which enables the exciter output to be adjustable between 4-V_{RMS} or 7-V_{RMS} mode. The integrated exciter amplifier enables up to 145 mA of excitation current with an exciter frequency from 10 kHz to 20 kHz.

The analog front-end (AFE) along with the digital tracking loop performs the resolver-to-digital-converter functionality. The AFE uses the cosine and sine signals and amplifies them by differential input amplifiers with programmable gain. The tracking loop is based on a Type-II Pi-controller architecture which enables the device to support up to 200 000 RPM in 10-bit mode.

Each block inside the device has dedicated diagnostics for fault coverage. All of the fault conditions are reported out through the SPI registers with a dedicated FAULT pin that can be used to interrupt a microcontroller unit (MCU) when a fault is detected in the system. The PGA411-Q1 device has programmable features that allow system flexibility when working with a wide range of resolver sensors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Exciter Amplifier Power Supply

The exciter power supply implemented in PGA411-Q1 device is supplied by the VCCSW pin for the internal driver logic and error correction and the VSW pin as a switch pin for creating a higher voltage rail. Both of these pins can be supplied by the same power supply when connected to the main device supply, V_{CC}, or these can be connected to a separate power source. A stabilization loop feedback pin, VEXTS, is implemented and should be connected to the output of the exciter power supply. Figure 11 shows the block diagram of the exciter power supply (boost regulator).

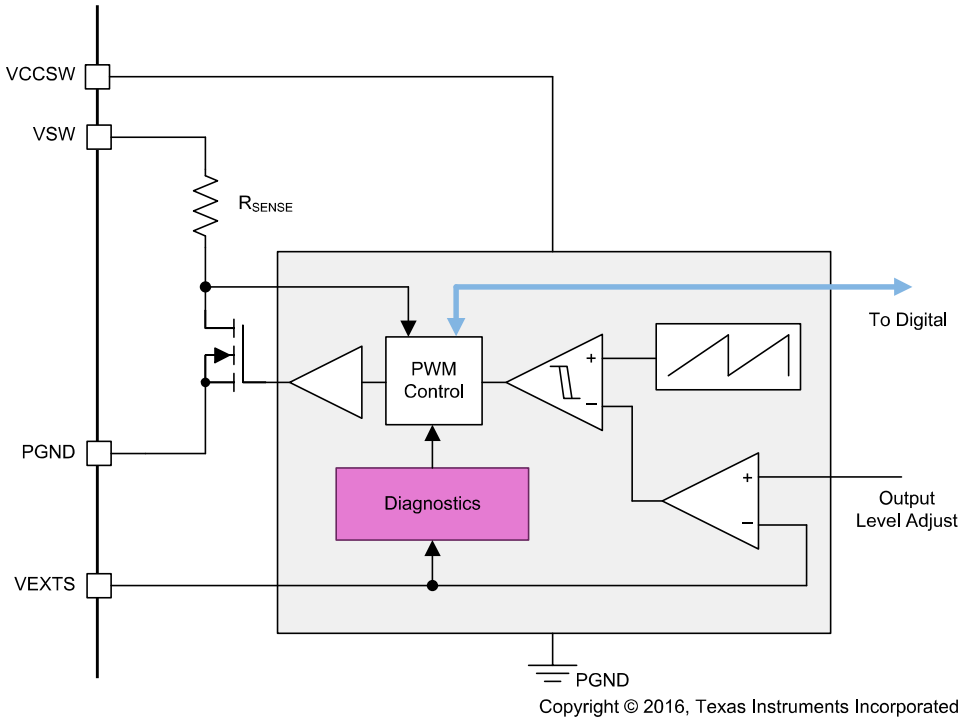


Figure 11. Exciter Power-Supply Block Diagram

The switching frequency for the exciter power supply is 414 kHz (±10% spread spectrum) while the output voltage selection occurs by setting the MODEVEXT bits in the DEV_CONFIG1 register. Regardless of the exciter output mode (4 V_{RMS} or 7 V_{RMS}), the exciter power supply can be adjusted for an output voltage from 10 V to 17 V. If the application requires a typical boost current above 100 mA, the nBoost_FF bit in DEV_OVUV4 should be set. This bit affects the boost regulator feedback control.

The VCCSW input voltage that is needed depends on the output voltage setting and current requirements of the resolver sensor being used. If the sensor requires high current and high voltage, then VCCSW may need to be higher than the typical PGA411-Q1 supply voltage of 5 V.

The exciter power-supply diagnostics are split between the diagnostics monitor and internal exciter power-supply diagnostics.

The diagnostics monitor inside the exciter power supply tracks the following:

- The output overvoltage fault reported by the FBSTOV flag in the DEV_STAT4 register. During this fault the device proceeds to the FAULT state. The typical value for setting the FBSTOV fault is 115% of the nominal selected output voltage.
- The power supply temperature. See the *Thermal Protection* section for more information.

The internal exciter power-supply diagnostics include the following:

Critical overvoltage – Disables the exciter power supply. The typical threshold value for this fault is when the output voltage is more than 175% of the nominal selected output voltage.

Feature Description (continued)

Critical undervoltage – Disables the exciter power supply. The typical threshold value for this fault is when the output voltage is less than 50% of the nominal selected output voltage.

Output current-limit lower threshold at 600 mA – Immediately turns off the switch (low-side FET) for the remaining time of the current switch cycle. After the current cycle expires, the switch continues normal operation.

Output current-limit upper threshold at 2000 mA – Immediately turns off the switch (low-side FET) for three consecutive switch cycles before resuming normal operation. If the condition persists and is still present after three retries the switch is disabled for 2 ms before resuming normal operation.

Both current limits are masked for seven switching cycles when the exciter power supply is initially enabled.

All diagnostics are passed through a 5-µs deglitch.

7.3.2 Exciter Signal Generation

The PGA411-Q1 exciter signal path is optimized for driving highly inductive loads such as the exciter coil of the resolver sensor. The signal path is designed for 4-V_{RMS} or 7-V_{RMS} operation selected by the EXTMODE bits in the DEV_PHASE_CFG register. These bits are also the main enable control for the full exciter signal generation path. When the EXTMODE bit is set to 00 or 11, the exciter signal path is disabled causing the PGA411-Q1 device to signal a FAULT condition. The exciter preamplifier offers the ability to adjust the exciter output signal to compensate for the variations of the transfer ratio for the resolver sensor. Furthermore, the exciter output pins OE1 and OE2 are protected against undervoltage, overvoltage, mutual short, short to battery, short to GND, and overcurrent. Other diagnostics include exciter signal monitoring in the AFE and overtemperature protection. See the *Detailed Design Procedure* section for more information on the calculation of the output voltage for the exciter signal path.

Figure 12 shows the exciter-signal generation circuit which consists of three major blocks.

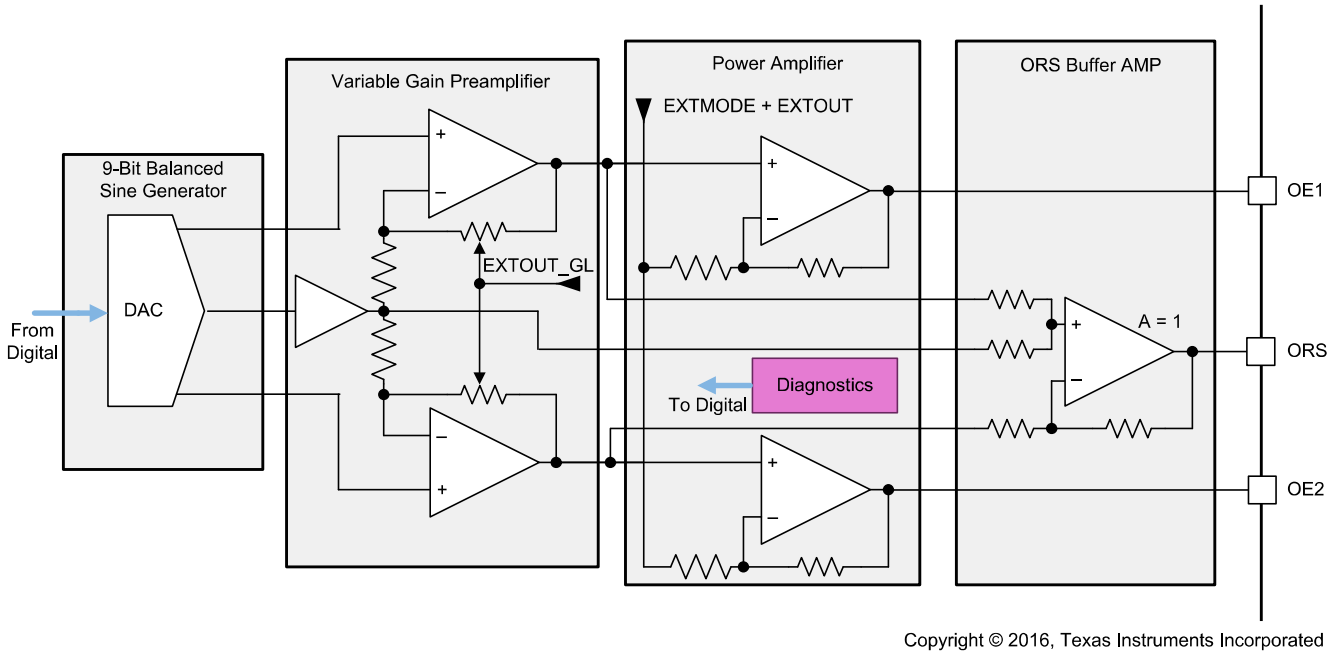


Figure 12. Exciter Signal Generation Circuit

7.3.2.1 Exciter Signal Generator

The exciter signal is generated by reading a digital sine wave stored in the device memory and then passed through a 9-bit differentially balanced DAC for generating a differential analog-exciter signal. The exciter frequency signal is from 10 kHz to 20 kHz and selected by the SELFEXT bits in the DEV_CONFIG1 register. See the *Clock Generation* section for more information on the exciter clocking.

Feature Description (continued)

7.3.2.2 Exciter Signal Preamplifier

The differentially balanced preamplifier conditions the exciter signal to the appropriate level for further output amplification. In the preamplifier block, the amplification level of the exciter signal can be adjusted while the common mode voltage is defined by the voltage at the COMAFE pin (typically 2.5 V). The preamplifier gain is selectable though the EXTOUT_GL bits in the DEV_OVUV1 register and affects both the preamplifier ORS output and the power amplifier outputs as shown in Figure 13.

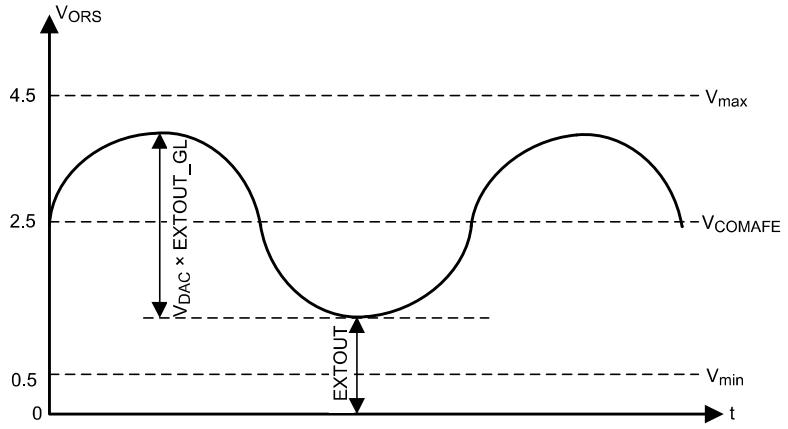


Figure 13. Exciter Preamplifier Gain

For signal monitoring or different exciter topologies, the output signal from the exciter preamplifier is available at the ORS pin of the PGA411-Q1 device. The output voltage is referenced to the voltage on the COMAFE pin. An external power amplifier such as the ALM2402-Q1 can be connected to the ORS pin to drive very high current sensors.

The ORS output of the exciter preamplifier is controlled by the XEXT_AMP bit in the DEV_OVUV2 register. When this bit is set to 1, external amplifier mode is selected which enables the ORS output and disables the internal output-power amplifier. However the default state of this bit is 0 which means that the ORS output is disabled and the internal output-power amplifier is enabled.

7.3.2.3 Exciter Output Power Amplifier

The internal output-power amplifier consists of two identical class-AB amplifier units that are independently input inverted to form a bridge-tied load (BTL) output topology. The exciter coil of the resolver sensor is connected at the output of the power amplifier (essentially between the OE1 and OE2 pins).

Power to the exciter power amplifier is supplied by the VEXT and PGND pins. The applied voltage should not, in any case, exceed the maximum rating of these pins.

To avoid output saturation (clipping), the power amplifier can be common-mode offset adjusted by the EXTOUT bits in the DEV_PHASE_CFG register between the limits of 0.5 V to 2 V expressed as foot-room voltage or the lowest output-voltage swing at OE1 or OE2. Figure 14 shows the common-mode offset (foot-room adjustment).

Feature Description (continued)

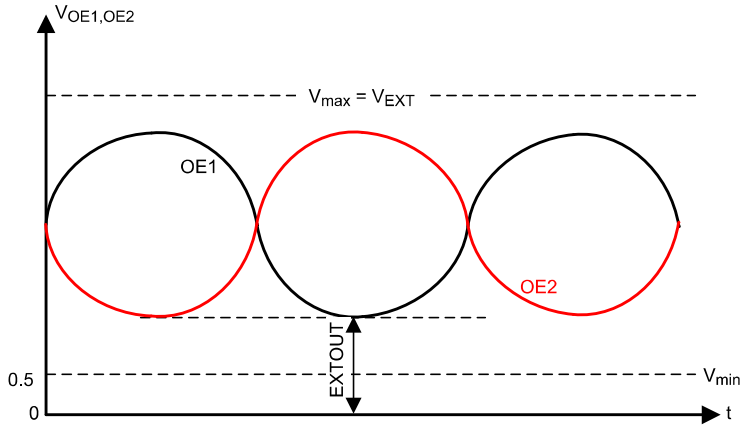


Figure 14. Exciter Power Amplifier Common Mode Offset Adjustment

See the *Diagnostics Monitor* section for diagnostics monitoring of the exciter power amplifier.

7.3.3 Analog Front-End

The AFE in the PGA411-Q1 device together with the tracking loop, performs the resolver-to-digital converter (RDC) functionality. The AFE block connects to the SIN and COS coils of the resolver sensor where the SIN (IZ2 and IZ4) and the COS (IZ1 and IZ3) signals are amplified by differential input amplifiers with variable gain. The amount of gain is determined independently by the SINGAIN and COSGAIN bits in the DEV_AFE_CFG register. The selected gain can be between 0.75 to 3.5. For best accuracy performance, TI recommends that the IZx differential voltage (V_{PP}) is between 600 mV_{PP} and 1.5 V_{PP} as measured at the OSIN and OCOS pins. The gain settings GAINSIN and GAINCOS SPI settings can be adjusted to optimize this signal. For example if the input to the IZx pins is between 800 mV_{PP} and 2 V_{PP}, setting GAINSIN = GAINCOS = .75 gain would give you the optimum V_{PP} of between 600 mV_{PP} and 1.5 V_{PP} on the OSIN and OCOS pins. The single ended voltage requirements on the IEx and IZx pins is between 0.5 V to 4.5 V.

The IE1 and IE2 inputs are used as a feedback from the exciter signal path for monitoring and diagnostics of the exciter signal. This exciter monitor circuit is also used by the phase-offset correction circuit for detecting and synchronizing the exciter signal together with the SIN and COS signals in the tracking loop.

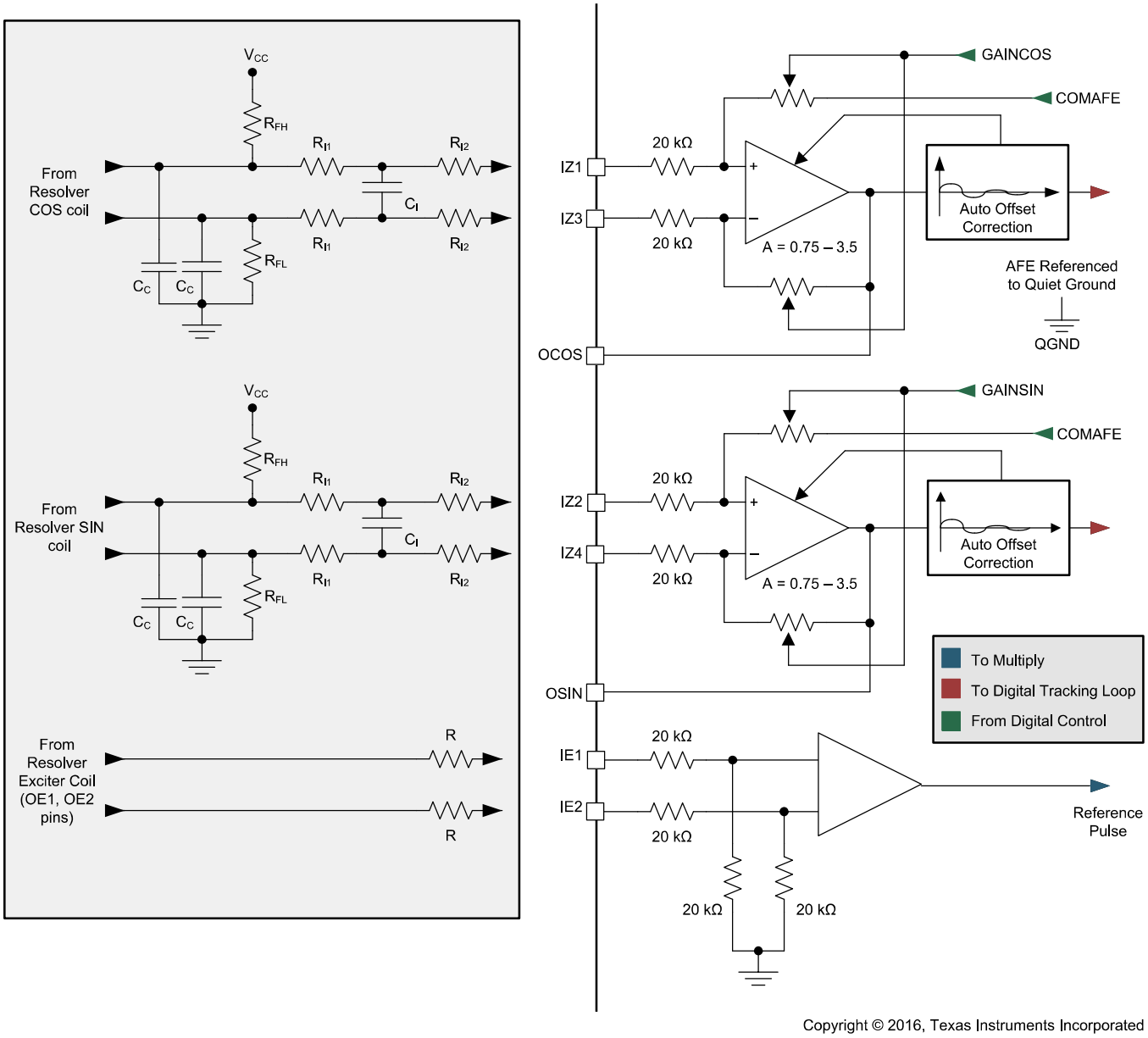
For additional amplification or attenuation and filtering of the input signal, an external circuit can be implemented as shown in Figure 15. See the *Detailed Design Procedure* section for selecting the external component values.

NOTE

The AFE is referenced to the quiet ground pin (QGND) and powered by the quiet voltage supply pin (QVCC). The supply for the QVCC pin must go high at the same time as V_{CC} for normal operation of the device. TI recommends tying QVCC to V_{CC} with additional local capacitance to filter further noise from being introduced.

For external signal monitoring, the PGA411-Q1 device outputs the amplified SIN and COS signals at the dedicated OSIN and OCOS pins. These output pins are referenced to the COMAFE pin.

Feature Description (continued)



R_{IX}	Gain setting resistors
C_I	Input capacitor
R_{FH} and R_{FL}	Open fault resistors
C_C	Common-mode capacitors

Figure 15. PGA411-Q1 Analog Front-End

Feature Description (continued)

7.3.4 Tracking Loop

A portion of the AFE, the analog multiply and subtract circuit, shown in Figure 16, together with the digital tracking loop shown in Figure 17 form a negative feedback loop that extracts the angle value that is measured by the PGA411-Q1 device. While in analog form, the input SIN and COS signals are multiplied with feedback SIN and COS from the digital tracking loop. When the multiplied signals are subtracted, a control deviation voltage signal, $V\Phi_{ERR}$, is generated. By using a comparator this signal is converted into digital form, ε_{PULSE}, and fed into the digital tracking loop.

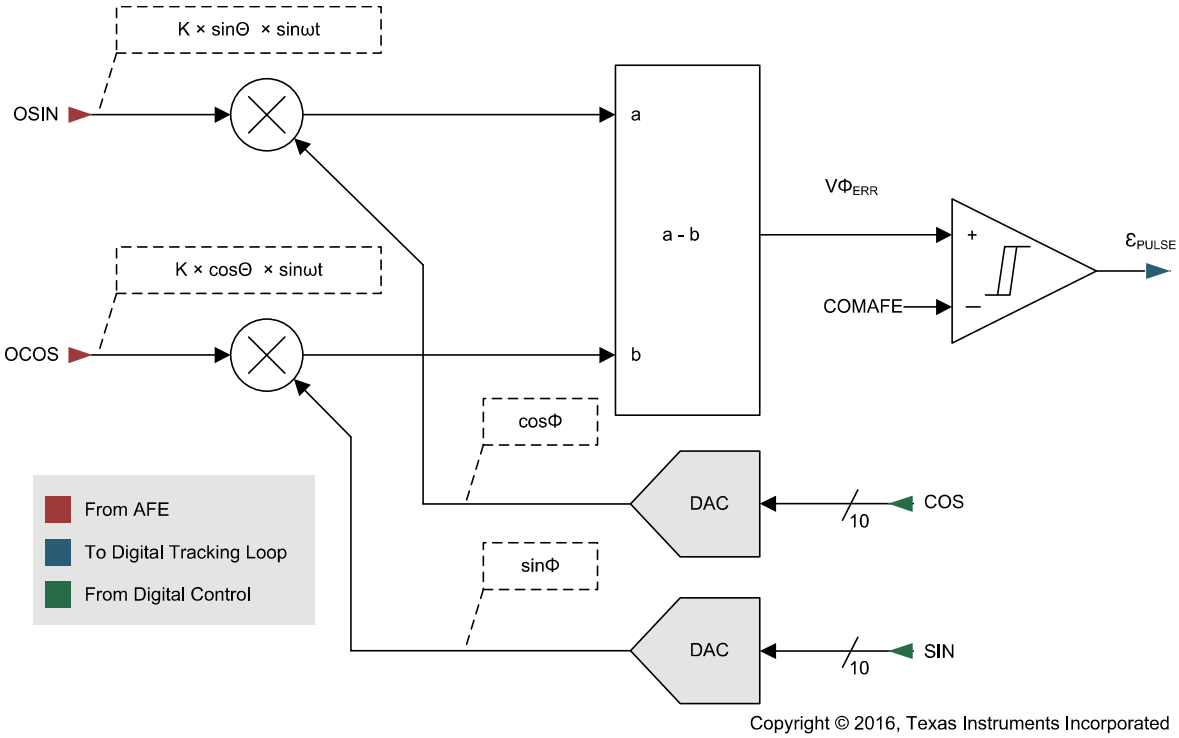


Figure 16. Analog Multiply and Subtract

Feature Description (continued)

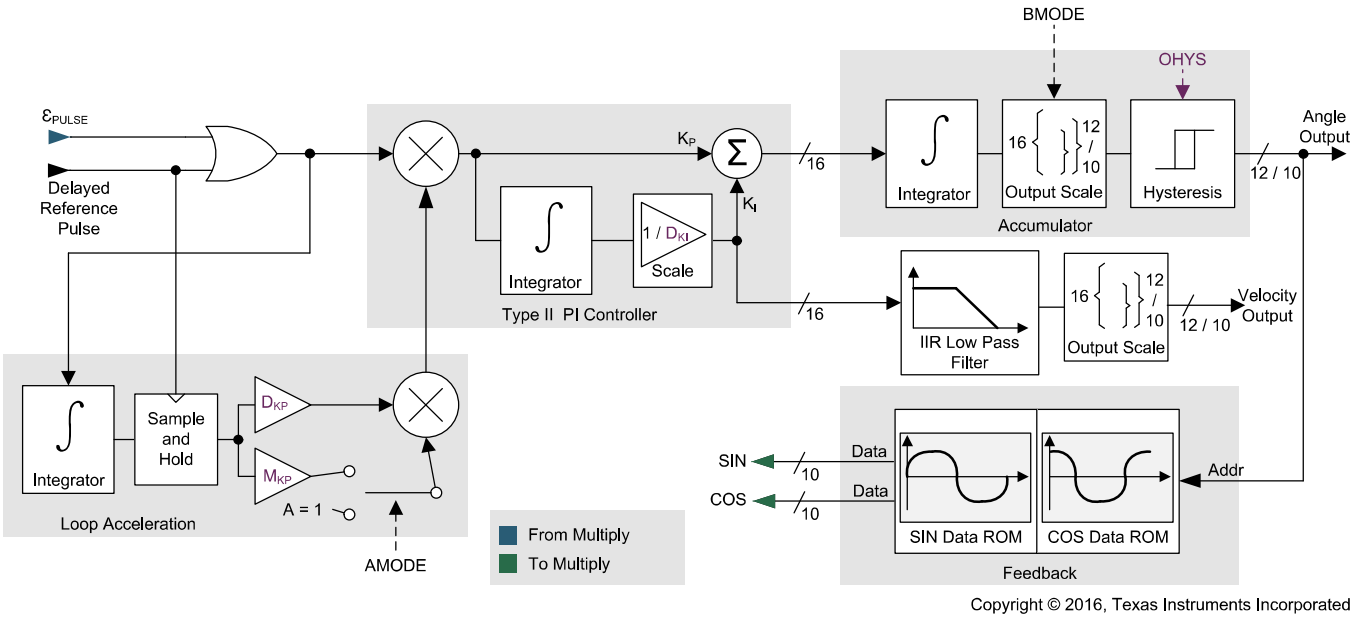


Figure 17. Digital Tracking Loop

The loop acceleration block helps the tracking loop improve the dynamic performance as a result of high angular acceleration effects. The PGA411-Q1 device implements a configurable loop acceleration block as well as an external enable control through the AMODE pin. When the AMODE pin is low, the tracking loop operates in normal mode and is still able to configure the loop-acceleration parameter, D_{KP}. By changing the value of the D_{KP} parameter in the DEV_TLOOP_CFG register, the tracking loop data is multiplied by the D_{KP} parameter at all times, thus defining the loop acceleration and settling time at any point of operation. When the AMODE pin is high the tracking loop data is multiplied by both the D_{KP} and M_{KP} parameters (set in the DEV_TLOOP_CFG register) until stable loop operation is achieved. Then the angle is updated to the new value and the loop returns to the normal mode of operation using only the D_{KP} multiplier.

The advantage of this accelerated mode of tracking is the ability for the tracking loop to disable the M_{KP} multiplier when the loop is stable and continue the operation by using the D_{KP} parameter until the next change in acceleration occurs or, for any reason, the loop becomes unstable. Thus, when using the accelerated mode the loop settling time is significantly reduced. Figure 18 shows the effects of loop acceleration.

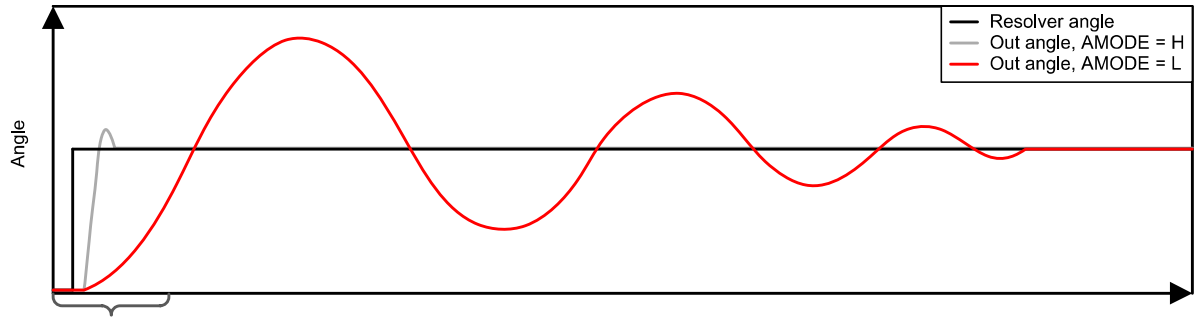


Figure 18. Effects Of Acceleration Mode

The Type II PI Controller extrapolates the synchronous ε_{PULSE} signal into a proportional term and integrated term for further analysis of where the angle data and velocity data are extracted. The PI Controller also tunes the tracking loop to the optimum value for stability. If the PI controller parameters are not selected correctly or the input tracking rate is too high, the PI controller becomes unstable. In this case the output data is unstable with or without oscillation and must be disregarded. Furthermore, instability inside the tracking loop causes the analog

Feature Description (continued)

$V\Phi_{ERR}$ deviation signal to exceed a certain stability limit. As a diagnostic measure for the instability of the tracking loop, a FLOOPE fault flag is implemented which monitors the $V\Phi_{ERR}$ deviation signal and, if outside the specified limits, signifies an unstable loop operation. See the *Fault Reporting* section for more information on loop-instability signaling. Setting the D_{KI} parameter in the DEV_TLOOP_CFG register adjusts the integration time constant in the PI Controller. Setting the integration time constant parameter at a higher value provides a more stable data output with less ripple; however, the tracking loop is at risk of saturation at higher rotational speeds which might be observed as an incorrect value at the velocity output.

The output data is formatted for proper output inside the accumulator. The output resolution of the PGA411-Q1 device is also selected through the BMODE0 pin. When the BMODE0 pin is low (DGND) the device operates in 10-bit mode. The output data range is between 0 and 1023 and extracted from the ORD9 to ORD0 pins when parallel output mode is selected. If the BMODE0 pin is high (VIO) the device operates in 12-bit mode and the output data range is 0 to 4095 extracted from the ORD11 to ORD0 pins when parallel output mode is selected. Prior to the output of the velocity information the data is passed through a first-order IIR low-pass filter with a cutoff frequency. Use Equation 1 to calculate the cutoff frequency.

$$f\ (-3\ \text{dB}) = \frac{0.000078 \times f_{clk}}{2}\ (\text{Hz}) \quad (1)$$

where

- f_{clk} is the device clock frequency (typically 20 MHz)

See the *Output Data Interface* section for more information on the format of the output data.

7.3.4.1 Resolver-to-Digital Converter Theory of Operation

The theory of the operation of a resolver to digital converter is summarized as the input SIN and COS modulated signals that carry the resolver angle information, Θ. Use Equation 2 and Equation 3 to calculate the value of the SIN and COS modulated signals.

$$V_{OSIN} = K \times \sin\Theta \times \sin\omega t \quad (2)$$

$$V_{OCOS} = K \times \cos\Theta \times \sin\omega t \quad (3)$$

At the output of the digital tracking loop an angle output, φ, is provided while the fedback (which includes the SIN and COS ROM value tables and the 10-bit DACs) provide sinφ and cosφ signals back into the analog multiply block. After the multiplication of these, use Equation 4 and Equation 5 to calculate the value of the outputs, a and b.

$$a = K \times (\cos\Theta \times \sin\varphi) \times \sin\omega t \quad (4)$$

$$b = K \times (\sin\Theta \times \cos\varphi) \times \sin\omega t \quad (5)$$

After the subtraction of b and a, use Equation 6 to calculate the value of the $V\varphi_{ERR}$ signal.

$$V\varphi_{ERR} = b - a = K \times (\sin\Theta \times \cos\varphi - \cos\Theta \times \sin\varphi) \times \sin\omega t \quad (6)$$

Further down the signal path, inside the digital tracking loop, the $V\varphi_{ERR}$ signal is demodulated, which yields the following:

$$K \times (\sin\Theta \times \cos\varphi - \cos\Theta \times \sin\varphi) = K \times \sin(\Theta - \varphi) = K \times (\Theta - \varphi), \text{ for small } (\Theta - \varphi) \text{ values.} \quad (7)$$

The expression, $K \times (\Theta - \varphi)$, is the angle error between the resolver angle, Θ, at the input and the RDC angle-output value, φ. The RDC tracking loop can stabalize at any given time, which means $K \times (\Theta - \varphi) \rightarrow 0$ as well as $V\varphi_{ERR} \rightarrow 0$. When the RDC loop is stabilized and the resolver sensor angle is tracked, the RDC output angle value, φ, is equal to the true resolver angle, Θ, as shown in Equation 8.

$$K \times (\Theta - \varphi) = 0 \geq \Theta = \varphi \quad (8)$$

For Diagnostic purposes the $V\varphi_{ERR}$ signal inside the PGA411-Q1 tracking loop is monitored to detect the loss of tracking in the tracking loop. See the *Diagnostics Monitor* section for more information.

Feature Description (continued)

7.3.5 Automatic Offset Correction

Because of the measurement topology of the resolver to digital converter, properly conditioning the input SIN and COS signals is very important. Therefore the PGA411-Q1 device implements an automatic offset correction which corrects the internal AFE offset drift, removing the offset drift the amplification process. Removing the drive occurs by measuring the offset drift voltage and applying the same amount of offset to the negative input of the AFE amplifiers and ε_{PULSE} comparator. The calibration begins with shorting the inputs together and passing the signal through a comparator that feeds into a digital logic circuit. Based on the output of the comparator, the digital logic goes through the offset correction values in the direction determined by the state of the comparator. When the comparator monitoring the offset voltage changes states, the direction of the calibration sweep changes, meaning at the point of minimal offset the comparators begins to toggle output states. This toggling signifies correct offset calibration. The automatic offset procedure is then complete. Figure 19 shows the block diagram for the AFE amplifier-calibration circuit.

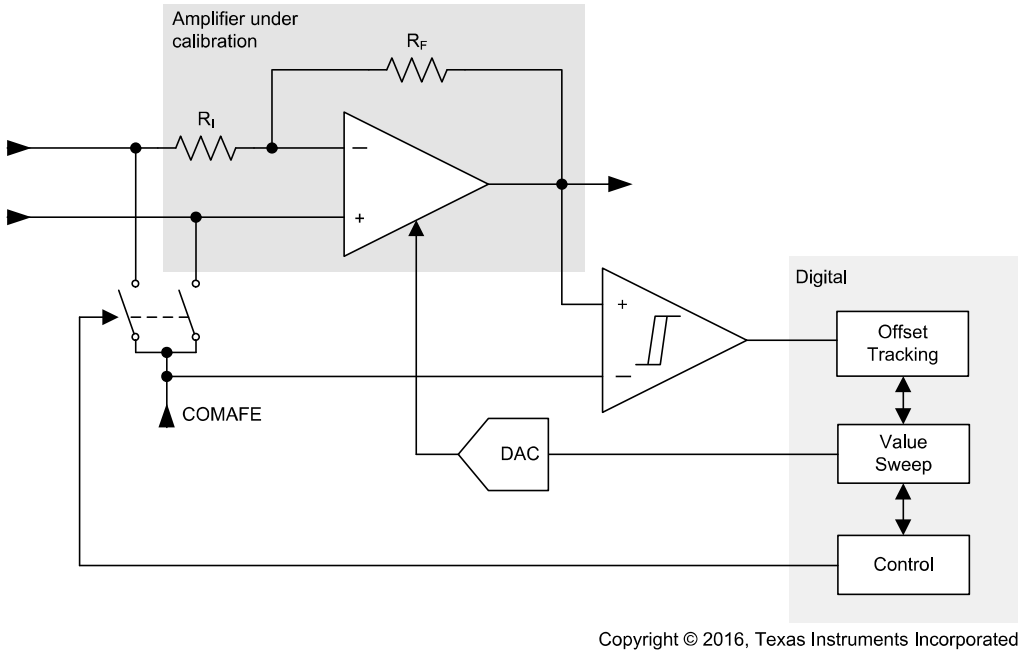


Figure 19. Amplifier Automatic Offset Calibration

In the same way as the AFE amplifier offset drift, the SIN and COS DAC amplifiers and the offset drift of the ε_{PULSE} comparator are calibrated for offset as soon as the AFE offset calibration is complete.

The offset correction occurs on every device power up when the device enters DIAGNOSTICS state and every 100 ms while the device is operating in the NORMAL state. The adjustment procedure lasts between 200 µs and 400 µs. The fault flag, FAFECAL in the DEV_STAT7 register indicates when the calibration encounters an error. See Figure 20 for more information on the automatic offset correction procedure.

Feature Description (continued)

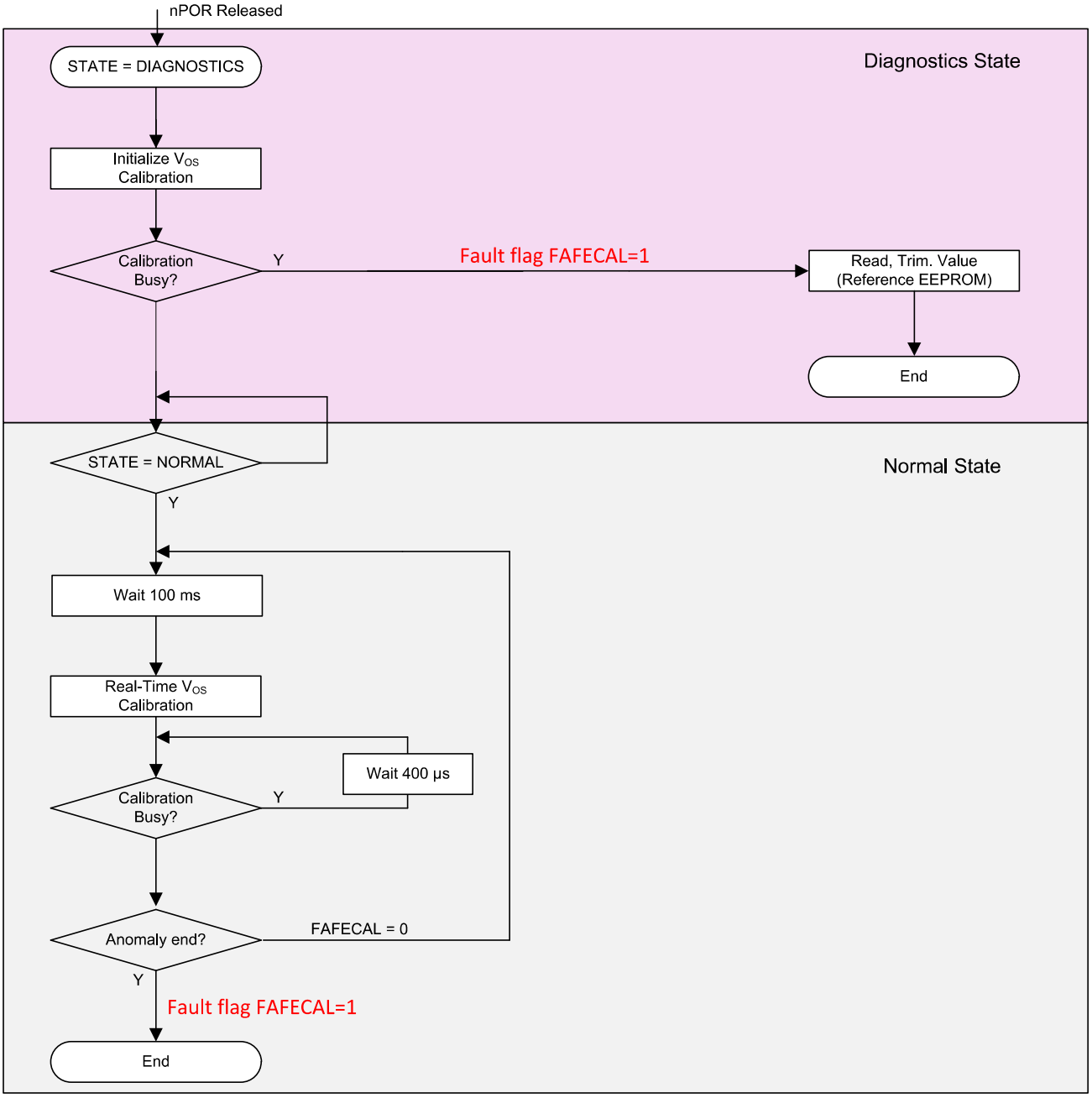


Figure 20. Automatic Input-Offset Correction Function Flow

NOTE

During the time period for automatic offset correction, the output of the PGA411-Q1 device is held at the last good value before the procedure began.

7.3.6 Phase Offset Correction

For the $V\varphi_{ERR}$ signal inside the tracking loop to demodulate correctly, an exciter reference pulse generated by the AFE exciter-signal monitor (the IE1 and IE2 pins) is used. This reference pulse must be in phase with the $V\varphi_{ERR}$ phase which, in turn is determined by the phase of the SIN and COS input signals.

Feature Description (continued)

The combination of the resolver coil impedance and the filter capacitance on the SIN (IZ2/IZ4) and COS (IZ1/IZ3) inputs can cause a phase delay between the reference pulse and SIN or COS input signals. If this phase shift is too large, it can lead to tracking loop instability and wrong angle data of the resolver to digital converter. The PGA411-Q1 implements a phase offset correction circuit to correct the position of the reference pulse while eliminating the phase mismatch.

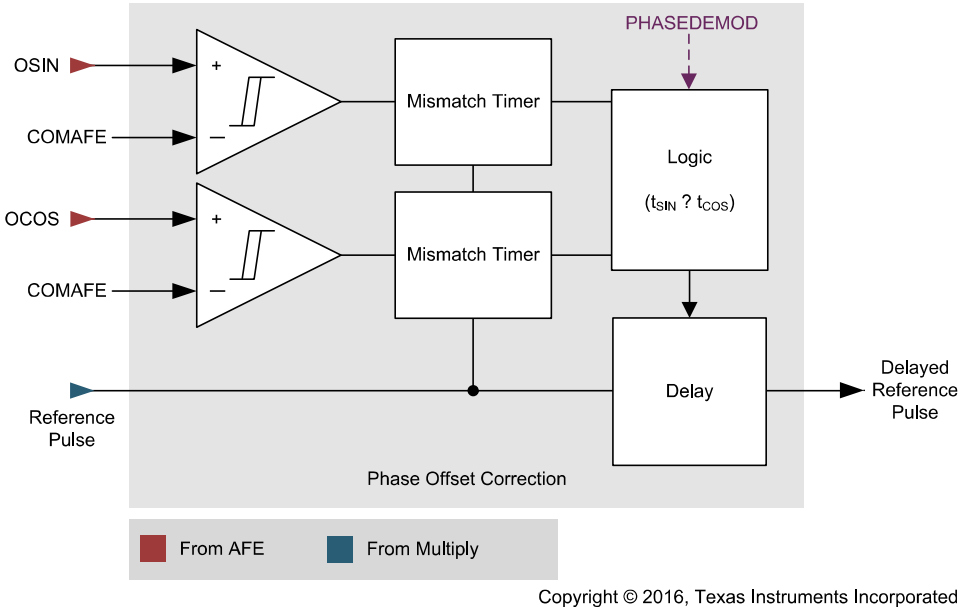


Figure 21. PGA411-Q1 Phase Offset Correction

The phase-offset correction circuit has two modes of operation: auto-mode phase delay and manual-mode phase delay. Table 1 lists the PDEN and APEN bit values (DEV_PHASE_CFG) for selecting each of these modes.

Table 1. Phase Delay Settings

PDEN	APEN	FUNCTION
0	0	No phase delay to the reference pulse
0	1	Auto-mode phase delay
1	0	Manual-mode phase delay
1	1	

7.3.6.1 Manual Mode

Phase delay to the reference pulse can be applied by setting the PHASEDEMOD bits in the DEV_PHASE_CFG register. The value of this setting is expressed in time (microseconds). The delay can be adjusted from –12.4 µs to +12.4 µs with a step size of 0.4 µs.

Use Equation 9 to calculate the phase delay in angular value.

$$\text{Phase Delay (degrees)} = 360 \times \text{Phase Delay (s)} \times \text{Exciter Frequency (Hz)} \quad (9)$$

Using Equation 9, the calculated adjustment range of manual phase is between –44.5 to +44.5 degrees with a step of 1.44 degrees for 10-kHz excitation frequency, or –89.2 to +89.2 degrees with a step of 2.88 degrees for a 20-kHz excitation frequency.

7.3.6.2 Auto Mode

In auto mode the phase delay of the SIN and COS input signals is measured with mismatch timers that are synchronized to the reference pulse. The higher measured value is then applied as a delay to the input reference pulse.

The auto-phase adjustment range can be between –89.2 to +89.2 degrees regardless of the excitation frequency as long as the frequency is from 10 kHz to 20 kHz. The adjustment step size is 100 ns which yields an angular step of 0.36 degrees at 10-kHz excitation frequency all the way to a step size of 0.72 degrees at a 20-kHz excitation frequency.

7.3.6.3 Diagnostics Monitor

The PGA411-Q1 diagnostics monitor tracks multiple signals that are being accepted from the resolver sensor (SIN and COS coils) and signals that are fed into the resolver sensor (exciter coil). In the case where any of these signals are deviated out of the assigned thresholds the diagnostic monitor reports fault signals to designated flags in the SPI registers. In conjunction with the fault reporting and the digital state machine, the PGA411-Q1 device reports these faults through the FAULT pin or disables a particular block accordingly to protect the system from a the given fault.

NOTE

Exciter diagnostics are disabled for the first 10ms after the exciter has been enabled.

7.3.6.3.1 Analog Front-End (AFE) Diagnostics

The AFE diagnostic monitor tracks signals that are fed into the PGA411-Q1 device from the resolver sensor SIN and COS coils. This tracking occurs by monitoring the IZx (where x = 1 through 4) signals and the OSIN output used to monitor the SIN-coil (IZ2 through IZ4) faults as well as OCOS output used to monitor the COS-coil (IZ1 through IZ3) faults. Additionally, as mentioned in the *Tracking Loop* section, the $V\varphi_{ERR}$ signal is monitored to ensure the tracking loop is stable and tracking.

Most AFE fault monitors include a high and a low threshold level setting because of the fact that the input signals are symmetrical and swing around a common-mode voltage (defined by COMAFE) therefore two threshold levels are defined for some faults while two overvoltage faults are defined for some signals that monitor the high-signal peak limit and the low-signal peak limit.

The AFE system faults monitored include the following:

- Input-short to GND or input-short to battery
- Input mutual short
- Input open
- Tracking loop stability
- Signal integrity check
- Exciter output open

Figure 22 shows the diagnostics implementation circuit for four of the listed faults.

NOTE

AFE diagnostics require a supply voltage of at least 5 V to be provided on the VEXT pin.

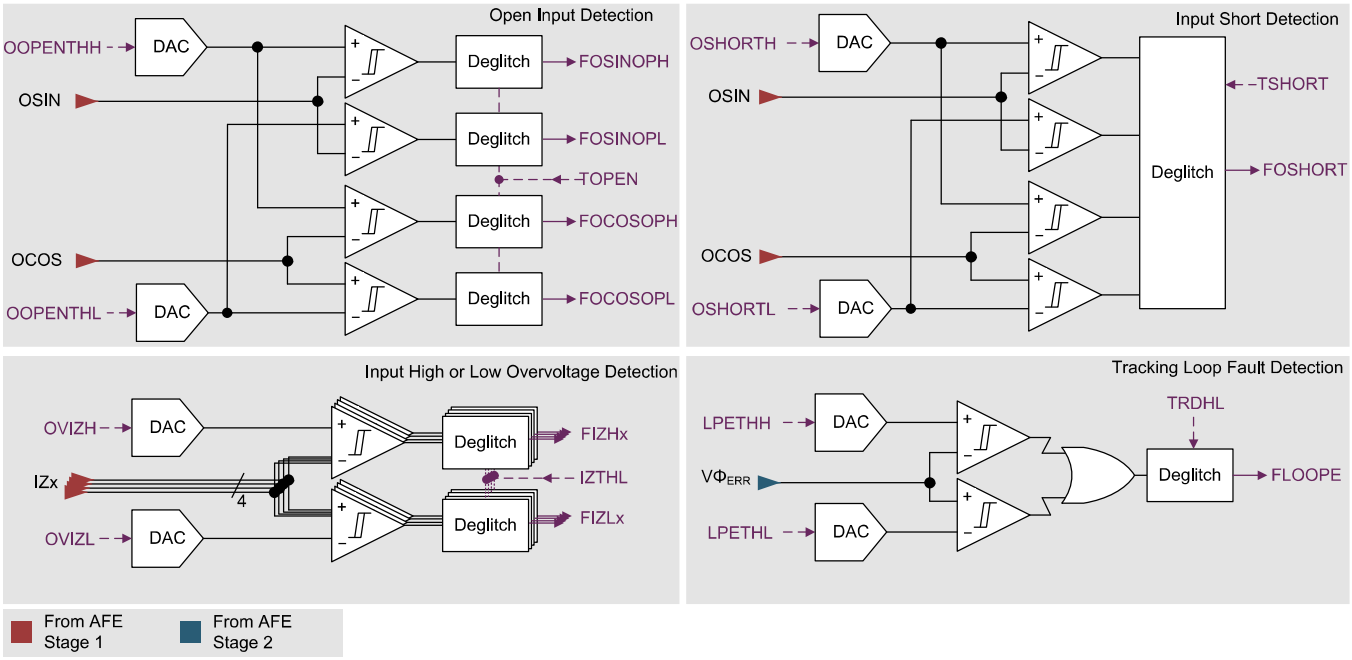


Figure 22. Open Input, Short Input, Input Fault and Loop Stability Diagnostics Implementation

In addition to Figure 22, Figure 23 shows the same four diagnostics along with the SPI-adjustable threshold levels of each. Figure 23 also shows a correct sine signal crossing all threshold levels with duration less than the specified deglitch limits and therefore no fault condition is triggered.

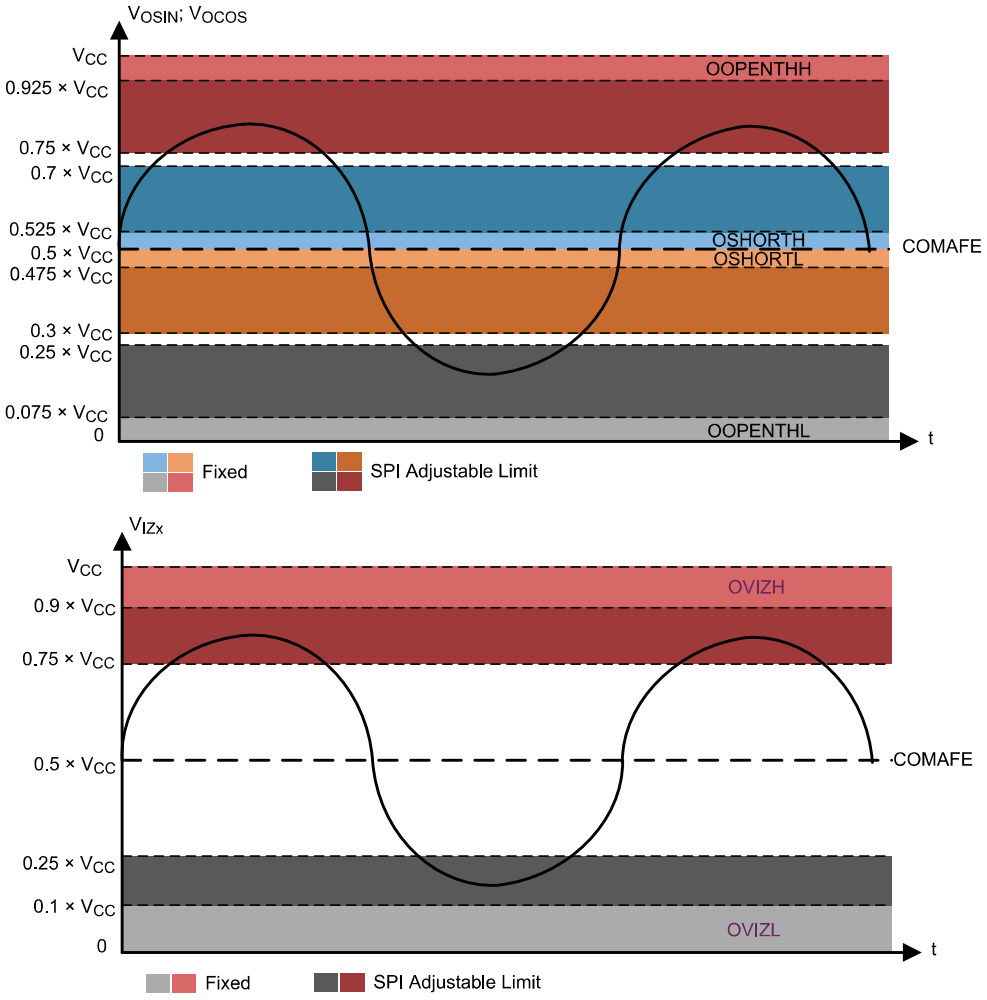


Figure 23. Open Input, Short Input and Input Fault Diagnostics Threshold Levels

7.3.6.3.1.1 Input-Short to GND or Input-Short to Battery

This fault is monitored by independently monitoring the IZx inputs expressed as positive and negative overvoltage. The thresholds for these are defined by the OVIZH and OVIZL bits in the DEV_OVUV3 register while the faults are reported by the FIZHx and FIZLx flags (where x = 1 through 4) in the DEV_STAT3 register. The mutual deglitch-time delay is defined by the IZTHL bits in the DEV_OVUV6 register.

7.3.6.3.1.2 Input Mutual Short

This fault is monitored by monitoring OSIN and OCOS outputs independently. For input mutual short the threshold is set by the OSHORTH and OSHORTL bits in the DEV_OVUV1 register while the deglitch-time delay is defined by the TSHORT bits in the DEV_OVUV4 register. The fault flag for this diagnostics is the FOSHORT bit in the DEV_STAT1 register.

7.3.6.3.1.3 Input Open

This fault is monitored by monitoring OSIN and OCOS outputs independently. For open input monitoring the threshold values are set by the OOPENTHH and OOPENTHL bits in the DEV_OVUV3 register and the deglitch time defined by the TOPEN bits in the DEV_OVUV5 register. The fault flags for the open input diagnostic are FOSINOPH, FOSINOPL, FOCOSOPH, and FOCOSOPL in the DEV_STAT1 register.

The open input diagnostic is possible only when the IZx inputs are externally DC biased as shown in Figure 15 because in the case of open input the input pin stays unconnected and the pullup or pulldown resistor sets the pin state to either V_{CC} for the IZ1 and IZ2 pins or GND for the IZ3 and IZ4 pins. Setting the pins as previously described causes the OSIN and OCOS outputs, which are monitored for open input detection, to either swing to V_{CC} or GND while crossing the open input threshold level for a period of time longer than the selected deglitch period.

7.3.6.3.1.4 Tracking Loop Stability

This fault monitors the $V\Phi_{ERR}$ signal with a threshold set by the LPETHH for the high threshold limit and the LPETHL bit for the low threshold limit. The deglitch-time delay is determined by the TRDHL bit while the FLOOPE fault flag reports this fault.

7.3.6.3.1.5 Signal Integrity Check

This fault monitors the IZx pins (where x = 1 through 4) in the same way as the input short-to-ground or input short-to-battery diagnostic while being controlled by the DVMSENH and DVMSENL threshold levels set in the DEV_OVUV2 register and a fixed 5-µs deglitch filter time. The difference with this fault is that these levels are fixed voltage levels and are not dependent of the voltage at the V_{CC} pin. The diagnostics flags for this diagnostics are OMIZxH and OMIZxL in the DEV_STAT3 register. Figure 24 shows the implementation of the signal integrity check and the SPI adjustable levels.

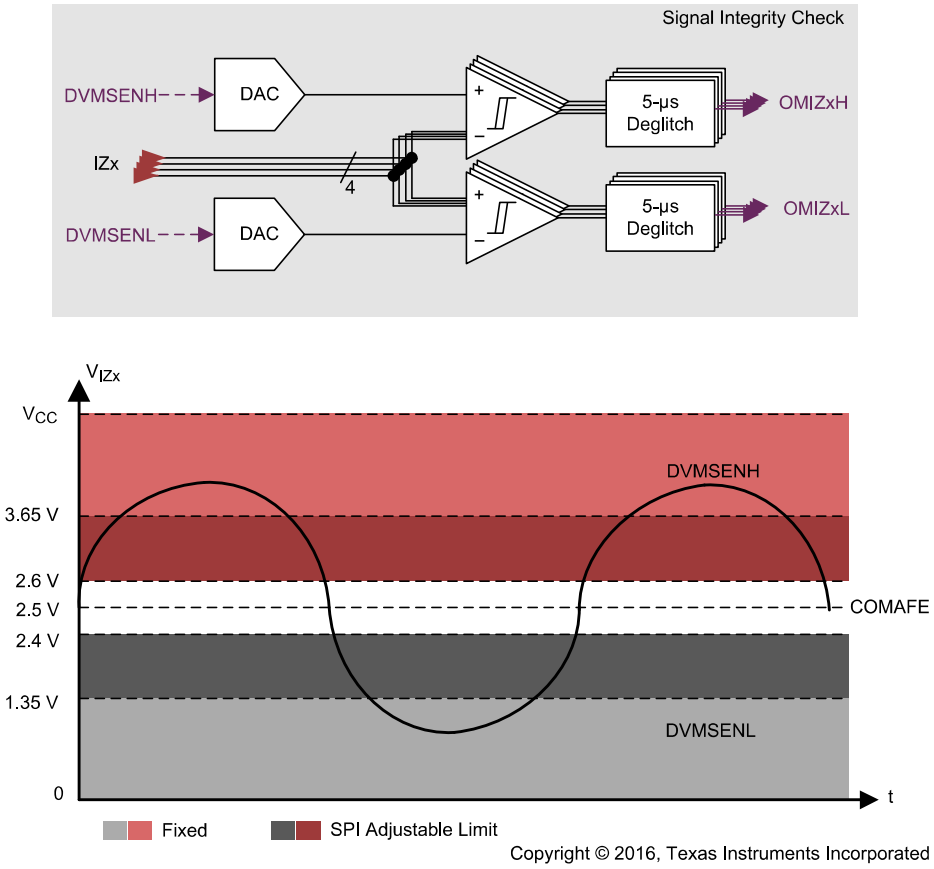


Figure 24. Signal Integrity Check Implementation and SPI Adjustable Thresholds

7.3.6.3.1.6 Exciter Monitor

The diagnostic employs the exciter monitor circuit that is described in the *Analog Front-End* section to track the duty cycle of the exciter reference pulse. During normal device operation the duty cycle of the reference pulse is 50% regardless of the exciter frequency. In the case where one of the OE1 or OE2 outputs is disconnected from the IE1 or IE2 inputs, the reference pulse changes the duty in a way that if OE1 is disconnected from IE1 then the comparator output is stuck low meaning the duty cycle is 0%. If OE2 is disconnected from IE2 then the

comparator is stuck high meaning 100% duty cycle. To ensure that noise does not affect the diagnostic the thresholds are chosen to be 20% when the output is stuck low and 80% when stuck high. The fault flags for this diagnostics are in the DEV_STAT4 register and are FEXTMONH for a duty cycle higher than 80% and FEXTMONL for a duty cycle lower than 20%. The deglitch time for this fault is defined by the TEXTMON setting in the DEV_OVUV6 register.

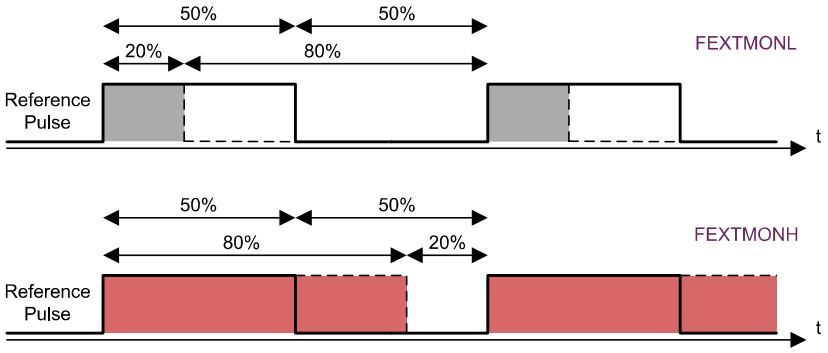


Figure 25. Exciter Monitor High and Low Diagnostics

7.3.6.3.2 Exciter Amplifier Diagnostics

The PGA411-Q1 exciter amplifier implements the following diagnostics:

- Single-ended overvoltage output
- Differential output undervoltage and overvoltage
- Excited output current limit

7.3.6.3.2.1 Single-Ended Overvoltage Output

Because of the implementation of the exciter amplifier in bridge-tied load topology, each output amplifier block is independently monitored for overvoltage condition at the output of the OE1 or OE2 pin in reference to GND. In case when the output signal at any of these pins is higher than 115% of the selected output value, the exciter amplifier will disable the outputs. The deglitch time for this diagnostic t_{DEGL} is fixed at 10 µs. This diagnostic covers fault conditions where the outputs of the exciter amplifier are shorted to an external high-voltage source. Figure 26 shows the implementation.

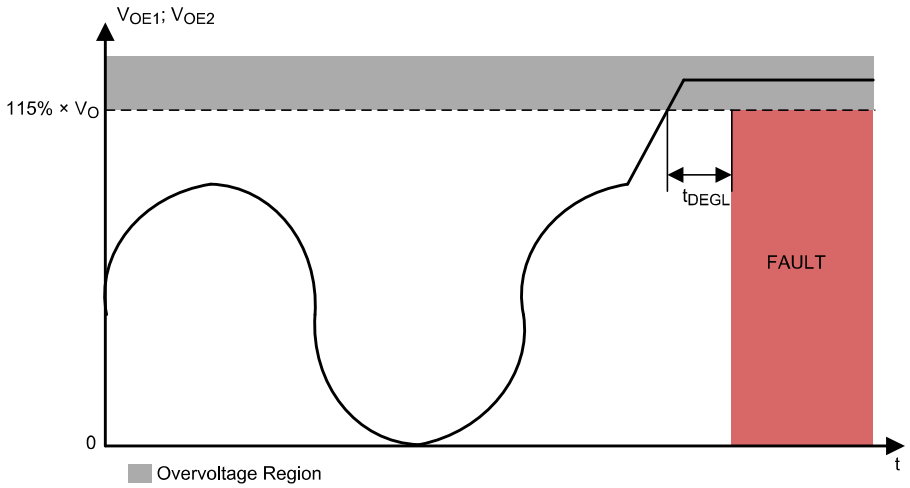


Figure 26. Single-Ended Output Overvoltage Diagnostic

7.3.6.3.2.2 Differential Output Undervoltage and Overvoltage

This diagnostic is the differential exciter-coil monitor for detection of exciter load undervoltage and overvoltage. The threshold values are fixed and depend on the mode of operation of the exciter output. In 4-V_{RMS} output-mode of operation the differential undervoltage threshold is set at 3 V and the differential overvoltage threshold is set at 8 V. In 7-V_{RMS} output-mode of operation the undervoltage threshold is 7 V and the overvoltage threshold is 14 V. The deglitch time for this diagnostics is SPI programmable by using the DEV_OVUV3 register bits EXTUVT for the undervoltage fault and EXTOVT for the overvoltage fault. The fault flags for this diagnostic are EXTUV and EXTOV in the DEV_STAT1 register.

Figure 27 shows the diagnostic for the differential output undervoltage and overvoltage.

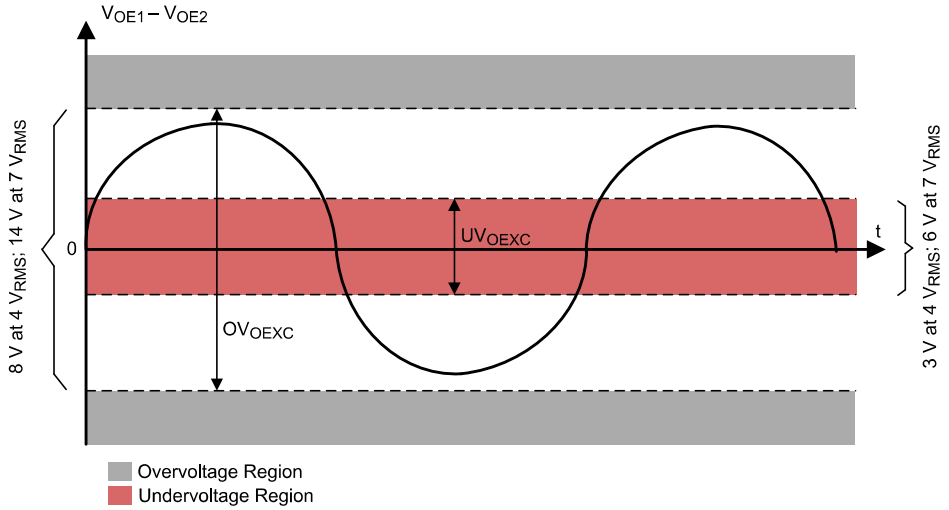


Figure 27. Differential Output Undervoltage and Undervoltage Diagnostic

In addition, a multiple-configuration differential undervoltage detection is defined by the EXTUVF_CFG bits in the DEV_PHASE_CFG register. Because the exciter output topology is a bridge-tied load drive, the two independent amplifiers monitor for undervoltage at the respective outputs. The default PGA411-Q1 configuration for reporting the differential undervoltage mode reporting the fault if either of these outputs detects undervoltage (logical OR). Other possible options for detecting this fault include when both outputs detect undervoltage (logical AND), or if either output or both outputs have an undervoltage (logical AND/OR). The last detection scheme makes sense because the deglitch time for undervoltage on both outputs (logical AND) is approximately 25 to 50 times shorter than the deglitch time for undervoltage on any output (logical OR) and the deglitch time depends on the selected SPI-programmable deglitch value.

NOTE

When using low exciter frequencies of 10.87 kHz or 10 kHz, the logical OR setting (EXTUVF_CFG = 00) is recommended.

7.3.6.3.2.3 Exciter-Output Current Limit

The exciter-output current limit monitors the current output from each amplifier. The current limit for each amplifier is individually adjusted by setting the EXTILIMTH_L1_2 and EXTILIMITH_H1_2 bits in the DEV_OVUV1 register between 150 mA and 300 mA. The maximum setting (bits set to 111) current limit of these registers is higher than the linear step size of the other bit settings; EXTILIMTH_H1_2 max is 370 mA and EXTILIMTH_L1_2 max is 600 mA. The deglitch period is fixed at 5 µs. In the fault condition where any of the current-limit thresholds is crossed for longer than the deglitch time, the EXTILIM fault flag in the DEV_STAT1 register is set and the device reacts according to exciter current-limit policy described in the *Fault Reporting* section. Figure 28 shows the currents through the resolver exciter coil. The exciter amplifier current limits implementation.

Under some conditions, the current limiting feature may come into effect before the overcurrent flag EXTILIM can be set. In these cases other fault flags such as EXTUV can be used to detect these types of overcurrent events.

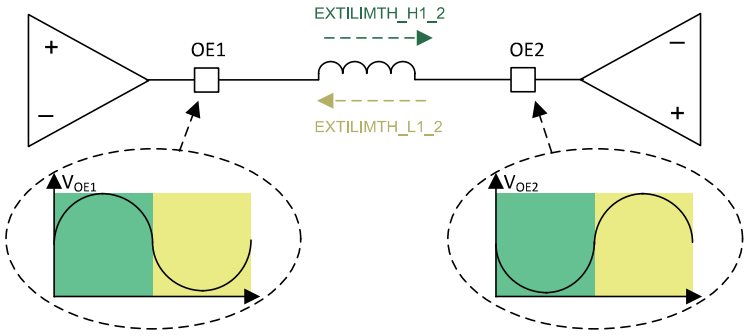


Figure 28. Exciter Amplifier Current Limit Diagnostic

7.3.6.3.3 Thermal Protection

The PGA411-Q1 device implements temperature sensors that are strategically located close to the exciter power amplifier and the V_{DD} digital regulator. The temperature sensors have thermal shutdown protection and a temperature prewarning capabilities. In the case of a thermal shutdown event, the PGA411-Q1 device is completely shut down and the device can be re-enabled only after the thermal shutdown condition is removed. During a thermal prewarning event, the condition is reported through the FSTD2 status flag in the DEV_STATUS4 register and a device FAULT condition is asserted as described in the *Device Functional Modes* section. In this case, the microcontroller unit (MCU) can manually disable the system before the thermal shutdown protection goes into effect. The deglitch time for the thermal prewarning fault, FTSD2, and the deglitch time for the thermal shutdown fault is 1.1ms.

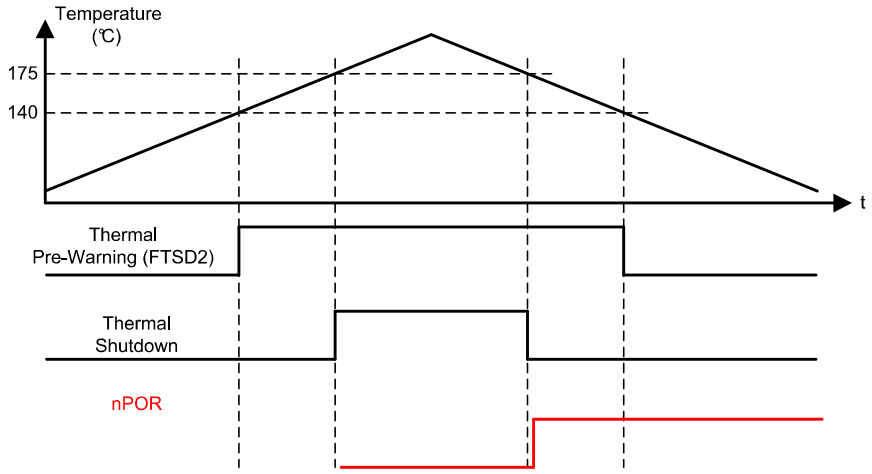


Figure 29. PGA411-Q1 Thermal Protection

7.3.7 Clock Generation

The PGA411-Q1 device can generate a digital system clock through an internal oscillator or an external crystal oscillator. The system clock is generated by setting the state of the ECLKSEL pin low (GND) to select the internal 20-MHz oscillator, or high (V_{IO}) to select the external oscillator. Using an external crystal because of limitations in the internal oscillator is highly recommended. Additionally, loss of clock monitor diagnostics are only applicable when selecting the external oscillator. To select an external crystal oscillator, connect a 20-MHz quartz crystal or resonator between the XIN and XOUT pins and capacitors to the DGND pin as shown in Figure 30. The recommended value for the capacitors is 15 pF.

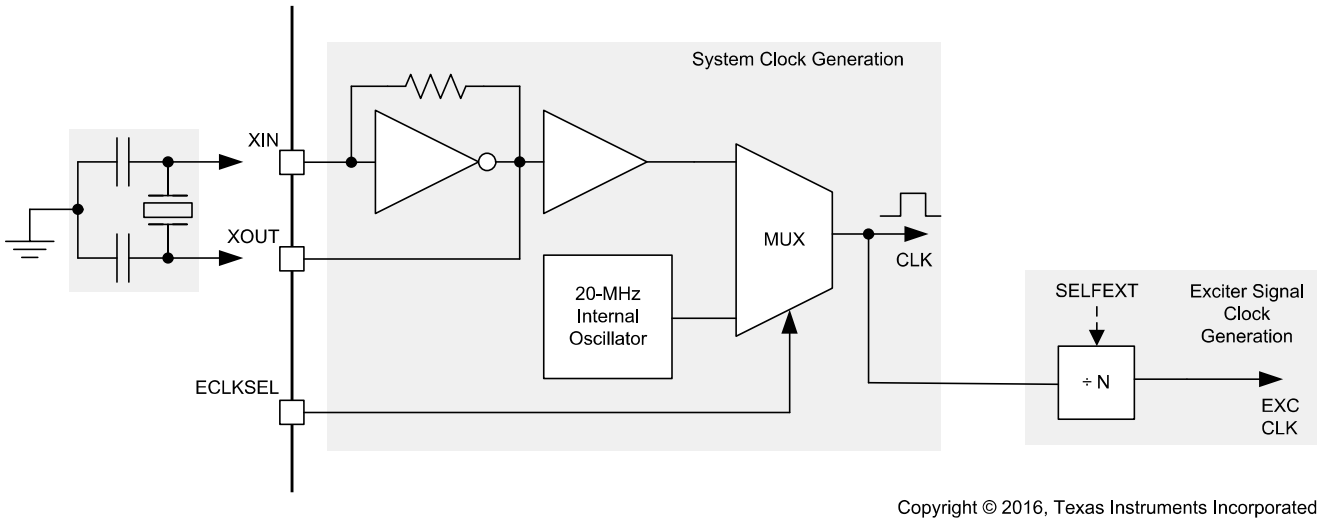


Figure 30. PGA411-Q1 Clock Generation

The exciter signal generator receives the digital clock signal from the main device oscillator and, by setting the SELFEXT bits, determines the exciter frequency.

7.3.7.1 Loss-of-Clock Monitor

When the ECLKSEL pin on the PGA411-Q1 device is set high (which means the main system clock is referenced to an external clock generated by a crystal or resonator element) the internally generated clock is used to monitor for correct operation of the device system clock. This monitoring occurs in the loss-of-clock monitor circuit which is designed to track the system clock and report a fault condition during two types of misbehavior. These misbehaviors are described as follows:

Device system-clock stuck condition This misbehavior is a fault case where the main device clock is high or low for a longer period of time.

Clock frequency out-of-range This misbehavior is a fault case where the main device clock drifts by –30% or 40% from the specified clock frequency.

Four consecutive counts of a clock-stuck or frequency out-of-range condition must occur before the PGA411-Q1 device determines an oscillator fault has occurred. In the case of a fault, the device enters the RESET state where the internal reset (nPOR) signal is asserted for as long as the fault is present. The loss-of-clock circuit is enabled in the DIAGNOSTICS state after the analog built-in self-test (BIST) is complete.

When the main device clock is sourced only by the internally generated clock of the PGA411-Q1 device, this functionality is not possible and the loss-of-clock circuit is disabled.

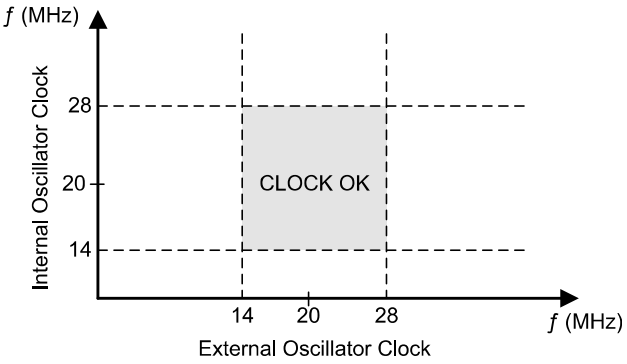


Figure 31. PGA411-Q1 Clock Monitor

7.3.8 V_{DD} Regulator

The V_{DD} regulator receives a 5-V input supply voltage form the V_{CC} pin and generates a stabile 1.8-V supply for the internal digital-logic circuits. The reference for the V_{DD} regulator is generated by the internal bandgap circuit of the PGA411-Q1 device. The V_{DD} pin is used for filtering and requires an external filtering capacitor. The V_{DD} regulator can supply a current up to 10 mA from the V_{DD} pin to power external circuits.

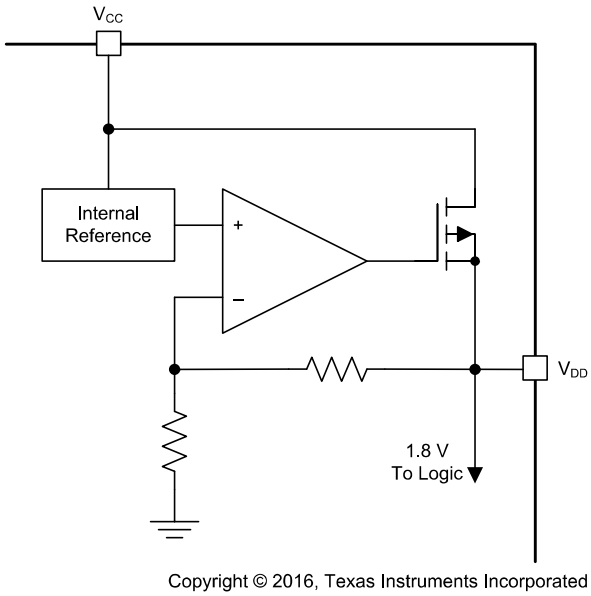


Figure 32. V_{DD} Regulator

The V_{DD} regulator, as well as the V_{CC} power-supply input, have integrated diagnostics that ensure proper operation of the overall PGA411-Q1 device. These diagnostics include undervoltage and overvoltage monitoring at the V_{CC} pin. The integrated diagnostics of the V_{DD} regulator include V_{DD} undervoltage and overvoltage and V_{DD} regulator overcurrent protection. See the *Fault Reporting* section for more information. The fault flags for the V_{CC} overvoltage, V_{DD} overvoltage, and V_{DD} overcurrent are the FVCCOV, FVDDOV, and FVDDOC flags in the DEV_STAT4 register.

NOTE

Under some conditions the overcurrent protection will limit the output current before the FVDDOC flag is set. In these cases, the undervoltage flag can be used for detection. This also applies to the exciter current limit fault flag EXTILIM and corresponding exciter undervoltage flag.

7.3.9 Digital Input and Output

All digital I/O pins in PGA411-Q1 device are referenced to the VIO input pin. The PGA411-Q1 device supports digital voltage levels between 3.3 V and 5 V.

The following PGA411-Q1 pins are considered digital I/O pins: OUTA, OUTB, ECLKSEL, BMODE0, TEST, NRESET, INHB, FAULTRES, PRD, FAULT, NCS, SCLK, SDI, SDO, AMODE, OMODE, VA0, VA1, ORD[11:0], and OUTZ.

7.3.10 Output Data Interface

7.3.10.1 Digital Parallel Output

The digital parallel output is the default data interface of the PGA411-Q1 output. To enable the parallel output interface, se the OMODE pin high (V_{IO}). The device is configured in the encoder-emulated output mode (described as follows) when the OMODE pin is set low (DGND).

The digital parallel output provides an update to the angle or velocity sample value every 100 ns at the ORD[11:0] pins which can be expressed as a 10-Msps output-update rate.

When the parallel output interface is enabled, the angle and velocity data is read from the ORD11 (MSB) to ORD0 (LSB) pins. The digital data at the parallel output is in 2s complement format. While this format is not important for the angle output because the value is always positive, the velocity output can be either positive or negative depending on the direction of the resolver rotation. In the case the resolver sensor rotation is clockwise (CW) and the value of the digital parallel-output velocity is positive. If the resolver sensor rotation is counter-clockwise (CCW), the output value is negative. In the case where the device is used in 10-bit mode (BMODE0 is low) the ORD10 and ORD11 pins are low (zeros) for a positive angle or velocity output or high (ones) for a negative velocity.

While the OMODE selection pin switches the ORD[11:0] pins between the parallel data output and the emulated encoder output, the VA0 and VA1 pins enable and disable the ORD[11:0] pins while also selecting the output parameter. Setting the ORD[11:0] pins in a high impedance (Hi-Z) state allows for systems to use multiple PGA411-Q1 devices controlled by a single MCU. The *System Examples* section shows an example of multiple PGA411-Q1 devices controlled by a single MCU.

Table 2 lists the VA0 and VA1 pin configurations.

Table 2. ORD[11:0] Output Selection

VA0	VA1	FUNCTION
0	0	ORD[11:0] set to Hi-Z
1	1	
0	1	Angle output at ORD[11:0]
1	0	Velocity output at ORD[11:0]

The INHB pin controls the update of the data output for the PGA411-Q1 device. When the INHB pin is high (VIO), the output data is sampled at the ORD[11:0] pins as soon as the data is available. When the INHB pin is set low (DGND), the data output at theORD[11:0] pins is held at the last sampled output. In a synchronous data-transfer system sampling the data at the output of the PGA411-Q1 device on every clock period is possible by applying a clock signal at the INHB input with a frequency lower than 10 MHz.

7.3.10.2 ORD Clock

An ORD clock output is present on the ORDCLK pin (ORD[13]) to allow for ORD[12:0] outputs to be settled before reading. The ORD clock is a 10-MHz clock that has the same update rate as the tracking loop data on ORD[12:0]. The positive edge of the ORD clock occurs 25 ns after ORD data has changed and is the ideal time to capture the settled ORD data. The ORD clock output is disabled during the offset correction sequence (see the *Automatic Offset Correction* section), if the inhibit pin is low, or if the tracking loop is disabled. Figure 33 shows the timing characteristics of ORDCLK in combination with the angle or velocity data available on ORD[12:0].

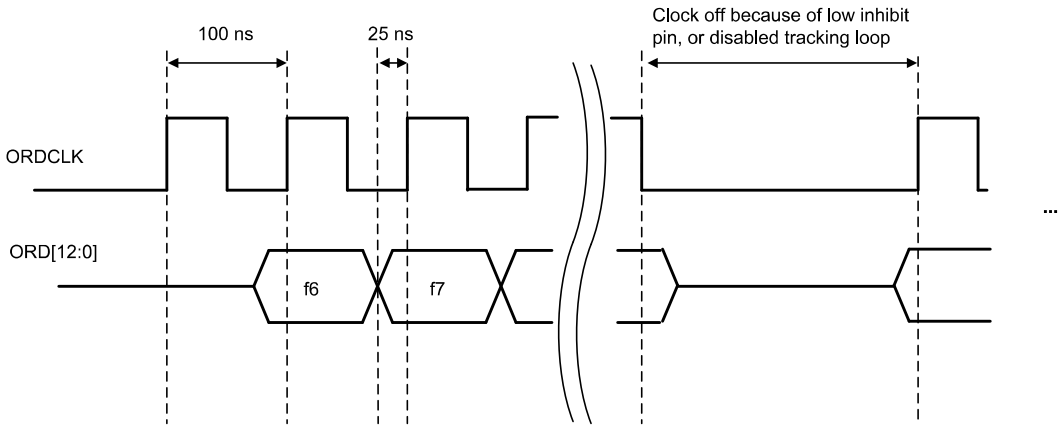


Figure 33. ORD Timing Characteristics

7.3.10.3 SPI Output

The angle and velocity data are also available in the register memory space and can be polled through the SPI. The corresponding locations are the ORDANGLE bit in the DEV_STAT5 register for angle data value and the ORDVELOCITY bit in the DEV_STAT6 register for velocity data value.

Use the following equations to convert the PGA411-Q1 parallel output or SPI data into meaningful angle and velocity values:

- 10-bit angle:

$$\varphi\,(\text{degrees}) = 360 \times \frac{\text{ORDx}}{2^{10}} \tag{10}$$

- 12-bit angle:

$$\varphi\,(\text{degrees}) = 360 \times \frac{\text{ORDx}}{2^{12}} \tag{11}$$

- 10-bit velocity:

$$\vartheta\,(\text{RPM}) = 60 \times \frac{f_{clk} \times (\text{ORDx} + 1)}{2^{21}} \tag{12}$$

where

- where f_{clk} is the device clock frequency (typically 20 MHz)

- 12-bit velocity

$$\vartheta\,(\text{RPM}) = 60 \times \frac{f_{clk} \times (\text{ORDx} + 1)}{2^{25}} \tag{13}$$

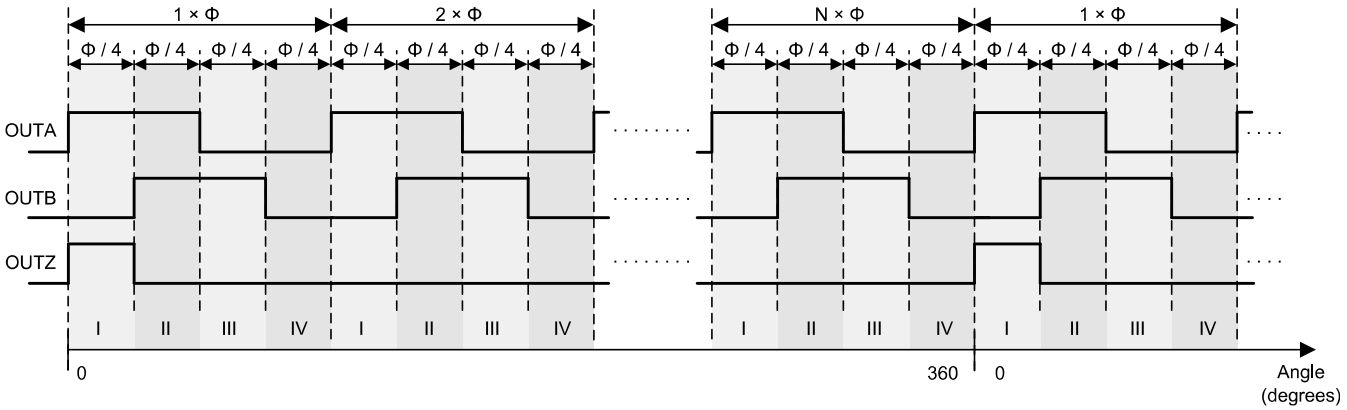
NOTE

An important takeaway from these velocity calculations is that the minimum change in velocity that can be read is 36 RPM in 12-bit mode and 572 RPM in 10-bit mode

7.3.10.4 Encoder-Emulated Output

The PGA411-Q1 device is capable of emulating quadrature-encoder output signals with index pulse and commutation signals. The quadrature-encoder output signals, A, B, and Z, are permanently available at the OUTA, OUTB, and OUTZ pins and are multiplexed on the ORD6, ORD7, and ORD8 pins. The commutation output signals, U, V, W, U1, V1, and W1, are multiplexed onto the ORD0 through ORD5 pins only. When the OMODE pin is set low (DGND) the PGA411-Q1 device is configured in encoder-emulator mode and the ORD0 through ORD5 pins output the assigned emulator signal. This signal multiplexing allows the MCU to switch between the parallel output interface and the encoder-emulated output by changing the state of the OMODE pin.

Depending on the resolution set by the BMODE0 pin, the quadrature encoder provides 256 pulses on the OUTA and OUTB pins when the device operates in 10-bit mode or 1024 pulses on the OUTA and OUTB pins when operating in 12-bit mode. The index pulse on the OUTZ pin is generated once during each revolution when the angle output is at 0 degrees. Figure 34 shows this functionality.



BMODE0	RESOLUTION	N
0	10 bit	256
1	12 bit	1024

Figure 34. PGA411-Q1 Quadrature Encoder Emulation

As shown in Figure 34, the number of A and B pulses also define the number of periods for each revolution. Use Equation 14 to calculate the minimal emulated angle with 22 (4 quadrature) combinations of A and B.

$$\Delta\varphi \text{ (degrees)} = \frac{\varphi}{4} = \frac{360}{4 \times N} \tag{14}$$

The commutation encoder emulation is determined by the number of poles (or poles multiplier) selected by the NPLE bits in the DEV_CONFIG1 register. For this case, use Equation 15 to calculate the emulated angle step.

$$\Delta\varphi \text{ (degrees)} = \varphi = \frac{360}{12 \times \text{NPLE}} \tag{15}$$

The PGA411-Q1 device supports pole section up to 4x.

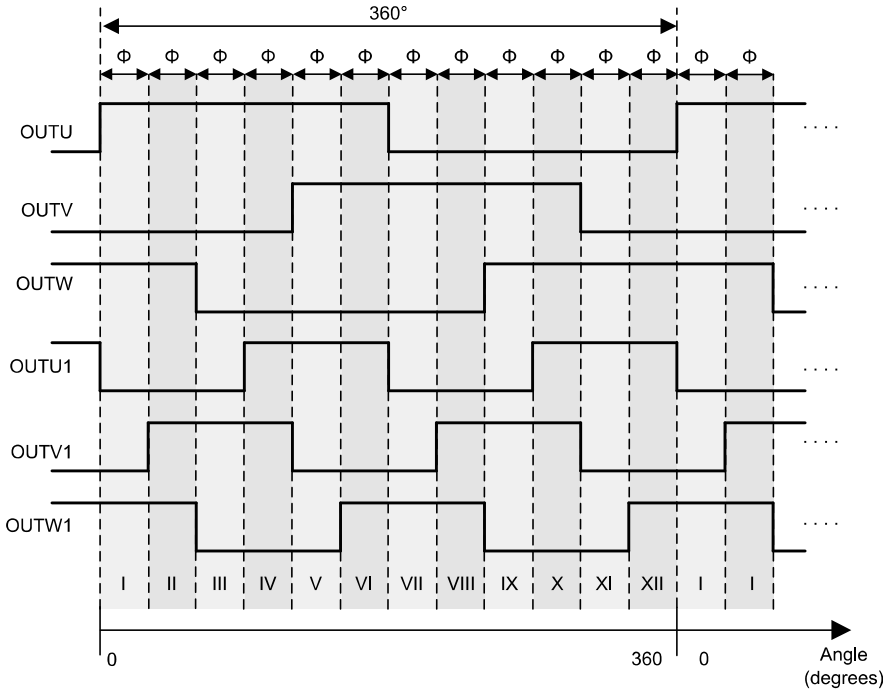


Figure 35. PGA411-Q1 Commutation Encoder Emulation

7.3.10.5 Analog Output

Analog representation of the angle output can be monitored at the AOUT pin. The PGA411-Q1 device implements a 10-bit DAC to convert the ORD digital-parallel output into an analog value between 0.5 V and 4.5 V. Because the analog DAC is limited to 10 bits at the input, in 12-bit resolver mode only the ORD[11:2] bits are ported into the input of the DAC. This feature is intended to be used only for initial evaluation and debug. For production, connect this pin to ground through a 0-Ω resistor. Figure 36 shows the analog voltage representation of the angle.

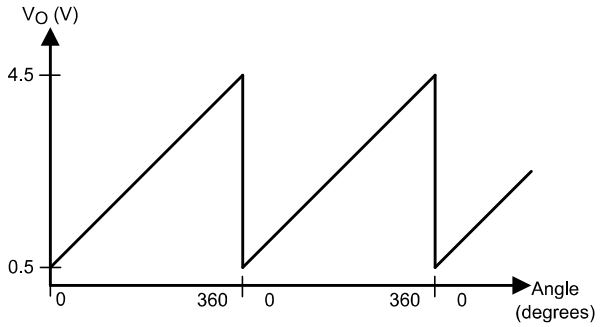


Figure 36. Analog Angle Output

7.3.11 Fault Reporting

Fault Reporting in the PGA411-Q1 device is signaled through the FAULT pin and SFAULT SPI register. The FAULT pin is an open-drain output structure. The pin is LOW when no fault is reported. The pin is in Hi-Z state when a fault is present in the system. An external pullup resistor is required to bring this rail HIGH when the pin enters the Hi-Z state during a fault. To clear the fault state in the system, when all fault conditions have been removed the FAULTRES pin must be toggled (high-low-high) and the PGA411-Q1 device transitions back into normal mode of operation.

The fault flags themselves are SPI fault bits that can be found in the DEV_STAT1, DEV_STAT3, and DEV_STAT4 SPI registers. Most of these fault flags will be cleared upon a SPI read command (assuming the fault itself is no longer present in the system). This behavior allows the MCU to identify transient faults, that may no longer be present, during the next scheduled SPI read.

For evaluation or testing purposes, the FAULTRES pin can be held LOW to keep the exciter enabled even during fault conditions.

Optionally, masking some faults that can signal a fault condition in the system is possible. By doing so, the PGA411-Q1 device reports the fault through the assigned SPI fault flag however no action occurs as long as the mask is set.

To help protect the output exciter amplifier, some faults disable the exciter coil by setting the EXTEN SPI bit to 0 which disables the exciter power amplifier (pins OE1 and OE2) . Exciter override bits are defined for some of these faults to keep the exciter amplifier enabled if that fault occurs. If the exciter is disabled through a SPI command, a 100-µs delay is recommended before the device changes state or is re-enabled.

Table 3 lists all the PGA411-Q1 faults that are reported through the FAULT pin and affect the output of the exciter power amplifier.

Table 3. PGA411-Q1 Fault Reporting Summary

FAULT DESCRIPTION	SPI FAULT BIT	FAULT PIN MASK BIT	FAULT PIN STATE	EXCITER OUTPUT	EXCITER OVERRIDE
EXCITER AMPLIFIER					
Invalid exciter mode selection	EXTMODE = 00		Hi-Z / High	Off	
	EXTMODE = 11				
Differential exciter overvoltage	EXTOV	MEXTOV			
Single-ended exciter overvoltage					
Differential exciter undervoltage	EXTUV	MEXTUV		Off(1)	ENEXTUV
Exciter current-limit fault	EXTILIM			Off	
AFE					
Exciter-monitor high fault	FEXTMONH	MEXTMON	Hi-Z / High	Off	
Exciter-monitor low fault	FEXTMONL				
AFE zero-offset calibration fault	FAFECAL	MAFECAL		On	
Input IZx (x = 1 through 4) high overvoltage	FIZHx	MIZOVx		Off(1)	ENINFAULT
Input IZx (x = 1 through 4) low overvoltage	FIZLx	MIZUVx			
Input IZ1/IZ3, or IZ2/IZ4 short fault	FOSHORT	MFOSHORT			
Sine input (IZ2/IZ4) high-open fault	FOSINOPH	MFOSINOPH			
Cosine input (IZ1/IZ3) high-open fault	FOCOSOPH	MFOCOSOPH			
Sine input (IZ2/IZ4) low-open fault	FOSINOPL	MFOSINOPL			
Cosine input (IZ1/IZ3) low-open fault	FOCOSOPL	MFOCOSOPL			
Digital tracking-loop input-error fault	FLOOPE	MFLOOPE			ENFLOOPE
POWER SUPPLY					
Exciter power supply (boost) overvoltage	FBSTOV		Hi-Z / High	Off	
V_{CC} supply overvoltage	FVCCOV				
V_{DD} regulator output overvoltage	FVDDOV				
V_{DD} regulator output overcurrent	FVDDOC			On	
Exciter thermal warning fault	FTSD2				
V_{CC} supply undervoltage	(RESET state)		Low	Off	
V_{DD} regulator output undervoltage					
FUNCTIONAL					

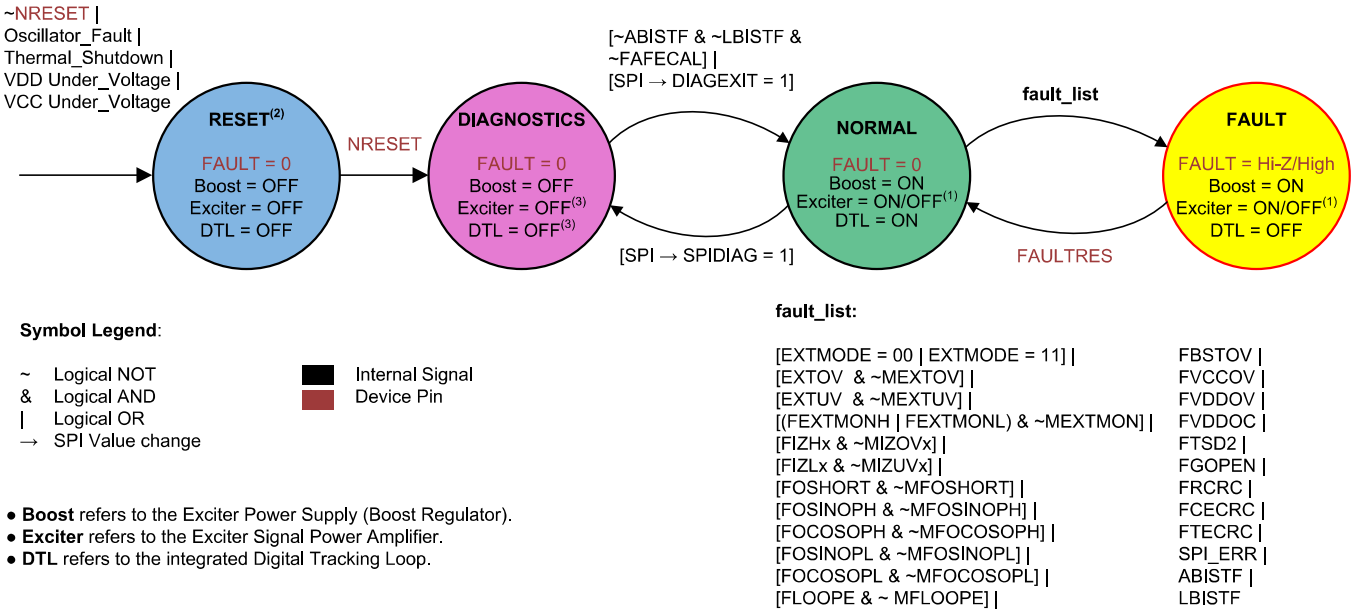
(1) The exciter output can be kept enabled if the corresponding over drive bit is set.

Table 3. PGA411-Q1 Fault Reporting Summary (continued)

FAULT DESCRIPTION	SPI FAULT BIT	FAULT PIN MASK BIT	FAULT PIN STATE	EXCITER OUTPUT	EXCITER OVERRIDE
Configuration and control registers CRC fault	FRCRC			Off	
User EEPROM space CRC fault	FCECRC				
Trim EEPROM space CRC fault	FTECRC		Hi-Z / High	On	
SPI communication fault	SPI_ERR				
Analog BIST fault	ABISTF			Off(1)	ENBISTF
Logic BIST fault	LBISTF				
Oscillator fault	(RESET state)		Low	Off	
FAULT pin read-back missmatch error	IOFAULT		—	Off(1)	ENIOFAULT

7.4 Device Functional Modes

The PGA411-Q1 device implements a digital state machine that is responsible for device functional operation, decision making, and system monitoring. See Figure 2 shows a detailed timing diagram of device power up. When the SPI is active the current device-operating state is found by reading the DEVSTATE bits in the DEV_STAT7 register.



- **Boost** refers to the Exciter Power Supply (Boost Regulator).
- **Exciter** refers to the Exciter Signal Power Amplifier.
- **DTL** refers to the integrated Digital Tracking Loop.

(1) Depends on *Exciter Override* selection, behavior implementation, or both as listed in Table 3.

(2) Not a physical state. When the device is in the RESET state, an nPOR signal is asserted to digital logic.

(3) Setting the EXTEN bit to 1 enables the exciter amplifier. Setting the LPEN bit to 1 enables the digital tracking loop.

Figure 37. State Diagram

7.4.1 PGA411-Q1 Reset

The RESET state is not a physical state-machine controller state. The RESET state in Figure 37 signifies an nPOR asserted in the PGA411-Q1 device, forcing the digital logic into reset (digital is frozen). On nPOR release the digital logic begins operating from the DIAGNOSTICS state.

In the system, the NRESET pin asserts the nPOR in the device logic. When the NRESET pin is low (DGND), the PGA411-Q1 logic is frozen and the device is in the RESET state. When the NRESET pin is pulled up, the logic is enabled after a 70-µs deglitch period and the device is operational.

In the RESET state, all functional blocks inside the PGA411-Q1 device are disabled, including the exciter boost regulator, exciter output amplifier, digital tracking loop, AFE, V_{DD} regulator, and oscillator. The state of the FAULT pin is low.

Device Functional Modes (continued)

During active device operation in any state the PGA411-Q1 device can cause an internal reset because of the following:

- An undervoltage event on the V_{CC} pin
- A V_{DD} regulator undervoltage event on the V_{DD} pin
- An oscillator fault condition signaled by the loss-of-clock monitor as described in the *Loss-of-Clock Monitor* section
- A device overtemperature condition which causes the thermal-protection circuit to generate a thermal-shutdown signal

The device resumes normal operation when the fault is cleared and the state of the NRESET pin is HIGH (VIO) which removes the nPOR.

7.4.2 DIAGNOSTIC State

The DIAGNOSTIC state is the first functional state in which the digital logic operates when the nPOR internal signal is removed. No faults are present and the NRESET pin is pulled up.

In the DIAGNOSTICS state the exciter boost regulator and the V_{DD} regulator are enabled. The exciter output amplifier, the digital tracking loop, and the diagnostics monitor are disabled. The FAULT pin state is LOW.

In this state the PGA411-Q1 device runs all internal checks before proceeding to the NORMAL operating state. These internal checks include the following:

- EEPROM CRC check
- Analog BIST diagnostics
- Logic BIST diagnostics
- AFE auto-offset calibration

The device transitions to the NORMAL operating state when the internal checks are complete and no faults have been reported. In the case of a fault, the device is locked in the DIAGNOSTICS state. When a fault is reported, the user has the ability to force the device to exit the DIAGNOSTICS state by setting the DIAGEXIT bit in the DEV_CONTROL1 register. When the user forces exit from the DIAGNOSTICS state, the PGA411-Q1 device transitions into the NORMAL operating state, however the faults continue to be reported through the corresponding SPI flags.

When the PGA411-Q1 device is in the NORMAL operating state, it can transition back to the DIAGNOSTICS state to rerun the start-up diagnostics when requested by the system. The device can transition back to the DIAGNOSTICS state by setting the SPIDIAG bit in the DEV_CONTROL3 register. The SPIDIAG and the DIAGEXIT bits are self-clearing bits and therefore return to 0 (reset) when the action is complete.

NOTE

If the user enters the DIAGNOSTICS state by SPI command after the device has powered-up normally and 150 ms have passed (the blanking time is ended), a fault may be flagged because the entering the diag mode will automatically disable the exciter and tracking loop. The user can reenable the exciter and tracking loop by SPI command and wait for the short fault to go away, clearing with a SPI read later.

7.4.3 NORMAL Operating State

The NORMAL operating state is the default active state of the device. The exciter amplifier, digital tracking loop, and the diagnostics monitor are enabled and operational in this state. These blocks are enabled in the following order:

- Exciter amplifier
- Digital tracking loop
- Diagnostics monitor

The EXTEN and the LPEN bits in the DEV_CONTROL3 register can be used as monitors to determine the state of the exciter amplifier and the tracking loop. These bits can also manually enable and disable these blocks.

Device Functional Modes (continued)

When all of the previously listed blocks are enabled, the device provides valid angle and velocity data at the output. While in this state the FAULT pin is LOW.

In case of a fault in the NORMAL operating state, the PGA411-Q1 device transitions into the FAULT state.

7.4.4 FAULT State

A device fault is indicated by setting the FAULT pin in the Hi-Z state in which case the PGA411-Q1 device is in the FAULT state. While in this state, the digital tracking loop is disabled and no angle or velocity data is updated at the output if the device. The exciter output amplifier can either be enabled or disabled depending on the type of fault. The following faults cause a transition to the FAULT state but do not disable the exciter amplifier output:

- AFE zero offset calibration (FAFECAL)
- V_{DD} regulator-output overcurrent (FVDDOC)
- Exciter thermal-warning fault (FTSD2)
- User EEPROM-space CRC fault (FCECRC)
- Trim EEPROM-space CRC fault (FTECRC)
- SPI communication fault (SPI_ERR)

The following faults also signal the FAULT state but the user can configure the system to keep the exciter amplifier enabled by setting the respective override bit:

- Differential exciter undervoltage (EXTUV) with the override bit, ENEXTUV
- IZx input-high overvoltage (FIZHx), IZx input-low overvoltage (FIZLx), SIN and COS input short fault (FOSHORT), SIN input-high open fault (FOSINOPH), COS input-high open fault (FOCOSOPH), SIN input-low open fault (FOSINOPL), and COS input-low open fault (FOCOSOPL) with the override bit, ENINFAULT
- Digital tracking-loop fault (FLOOPE) with the override bit, ENFLOOPE
- Analog BIST fault (ABISTF) and Logic BIST Fault (LBISTF) with the override bit, ENBISTF
- FAULT-pin read-back mismatch error IOFAULT with the override bit, ENIOFAULT

All remaining faults transition the device into the FAULT state. Setting the FAULT pin in the Hi-Z state, as described in the *Fault Reporting* section, signals these faults to transition the device into the FAULT state. These faults do not allow enabling of the exciter amplifier until all the faults have been removed and the state machine is transitions back to the NORMAL operating state.

To exit the fault state of the PGA411-Q1, when all fault conditions have been removed, the FAULTRES pin must be toggled (high-low-high) to transition the device back into normal mode of operation. Do not keep the FAULTRES pin low for longer than 1ms and do not use FAULTRES more than once every 500ms. Toggling the FAULTRES pin with a fault condition still present will force the PGA411-Q1 into normal operation, which may cause damage to the PGA411-Q1. This is most likely to occur with high current short circuits on the exciter amplifier.

WARNING

Toggling the FAULTRES pin with a fault condition still present will force the PGA411-Q1 into normal operation, which may cause damage to the PGA411-Q1.

7.4.5 EEPROM Memory

The EEPROM memory space in the PGA411-Q1 device is split into two functional blocks: a User EEPROM space and a reserved, Texas Instruments internal-use EEPROM space used for device trim and manufacturing data values. The user EEPROM-memory space is directly accessed through the SPI registers. The internal digital logic of the device ports the data into the EEPROM shadow registers for the EEPROM memory fields. Table 4 lists of all SPI memory locations that are a part of the user EEPROM space.

NOTE

The factory EEPROM settings are subject to change without notice. Customers should program their own EEPROM settings according to the needs of their applications.

Table 4. User EEPROM Space SPI Mapping

SPI REGISTER	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	FACTORY SETTINGS
DEV_OV UV1	EXTOUT_GL				EXTILIMTH_L1_2			EXTILIMTH_H1_2			OSHORTL			OSHORTH			8B40h
DEV_OV UV2	—							XEXT_AMP	TRDHL		DVMSENH			DVMSENL			00EDh
DEV_OV UV3	EXTUVT			EXTOVT			OVIZL	OVIZH			OOPENTHL			OOPENTHH			FCFFh
DEV_OV UV4	—					TSHORT		TEXTMON			AUTOPHASE_CFG			VEXT_CFG	nBOOST_FF	FSHORT_CFG	07E2h
DEV_OV UV5	—			TOPEN				—									1C00h
DEV_OV UV6	—						IZTHL			BOOST_VEXT_MASK	—		LPETHL		LPETHH		038Fh
DEV_TL OOP_CFG	—					MKP		DKP			OHYS		SENCLK	DKI			0514h
DEV_AFE_CFG	—												GAINCOS		GAINSIN		0005h
DEV_PHASE_CFG	EXTUVF_CFG		PDEN	APEN	EXTMODE		EXTOUT				PHASEDEMOD						1400h
DEV_CONFIG1	—							NPLE		—	SELFEXT			MODEVEXT			0002h
DEV_CLCRC	—								ECCRC								00CEh

All of the SPI locations listed in Table 4 and the functionality of each is described in the *Register Maps* section.

To perform EEPROM operations as EEPROM programming and EEPROM reloading, the EEPROM user-memory space must initially be unlocked. To unlock the user-memory space, a sequence of unlock commands must be written to the EEUNLK bits in the DEV_EE_CTRL4 register. Table 5 lists the unlock sequence.

Table 5. User EEPROM Unlock Sequence

SPI WRITE SEQUENCE	DEV_EE_CTRL4 WRITE ADDRESS	UNLOCK DATA	SPI CRC
1	0x56	0x000F	0x13
2		0x0055	0x08
3		0x00AA	0x0F
4		0x00F0	0x14

NOTE

To unlock the user EEPROM space, the PGA411-Q1 device must be in the DIAGNOSTICS state and the complete unlock procedure must be complete within 10 ms.

When the user EEPROM is unlocked and the EEPROM shadow registers have been updated, programming occurs by writing the 0xA7 command to the EECMD bit-field in the DEV_EE_CTRL1 register and the 0xA2 command to the to the EECMD bit-field for EEPROM data reload. This bit-field is self-clearing upon execution and can be used indicate that an action is complete which means that, if the EECMD data is read and equal to 0x00, the previous EEPROM operation is complete. The EEPROM reloading operation is not always needed because the EEPROM data values are loaded initially upon device power up when entering the DIAGNOSTICS state (nPOR release).

The PGA411-Q1 EEPROM controller implements a self-contained cyclic-redundancy-check (CRC) algorithm to verify the integrity of the EEPROM stored data. When an EEPROM operation is executed, the CRC controller automatically calculates the correct CRC value and places the value in the ECCRC bit-field in the DEV_CLCRC register. Because the user EEPROM-memory locations are transparent to the SPI memory space, all of the user EEPROM values are listed in Table 6. Because the values are included in device memory, the MCU is required to provide a correct CRC value only according to the *Device Configuration CRC Protection* section. Therefore no user interaction is required when calculating the ECCRC value. However, for increased protection, the MCU can self-calculate the user EEPROM CRC value and compare this value with the ECCRC value for correct CRC calculation and correct user EEPROM-data integrity.

The user EEPROM-CRC algorithm is same as the device-configuration CRC algorithm (ATM HEC poly X8 + X2 + X + 1 with an initial seed of 0xFF and MSB ordering) and is performed on a 136-bit concatenated string, byte-wise beginning with the least-significant byte. To optimize implementation, the PGA411-Q1 device splits the registers into 8-bit chunks for the CRC calculation which are then ordered from most-significant bit to least-significant bit. Table 6 lists the data concatenation for the EEPROM CRC calculation.

Table 6. User EEPROM CRC Bus Order

USER EEPROM REGISTER		136-BIT BUS ORDERING
NAME	DATA SPLIT	
	0s Pad [31:0]	[MSB] 135:104
DEV_CONFIG1	DEV_CONFIG1 [7:0]	103:96
DEV_OVUV5	DEV_OVUV5 [12:10]	95:93
DEV_AFE_CFG	DEV_AFE_CFG [3:0]	92:89
DEV_OVUV2	DEV_OVUV2 [8:0]	88:80
DEV_OVUV4	DEV_OVUV4 [10:5]	79:74
DEV_OVUV6	DEV_OVUV6 [9:0]	73:64
DEV_OVUV4	DEV_OVUV4 [4:0]	63:59
DEV_TLOOP_CFG	DEV_TLOOP_CFG [10:0]	58:48
DEV_PHASE_CFG	DEV_PHASE_CFG [15:0]	47:32
DEV_OVUV1	DEV_OVUV1 [15:0]	31:16
DEV_OVUV3	DEV_OVUV3 [15:0]	15:0 [LSB]

7.4.6 Functional Diagnostics Modules

7.4.6.1 Analog and Logical Built-in Self-Test

The built-in self-test (BIST) is the controller and monitor circuit for performing self-checking diagnostics on critical analog and logic functions. These functions include the following:

- Input short, open, high overvoltage, low overvoltage, and signal integrity comparators
- Tracking loop comparator
- Main V_{CC} supply overvoltage and undervoltage comparator
- Exciter signal-monitor comparator
- Exciter-amplifier power supply
- Clock monitor check

The voltage signals are unchanged during the analog BIST process on the implemented comparators and therefore no real undervoltage or overvoltage occurs in the system because of the BIST. See Figure 38.

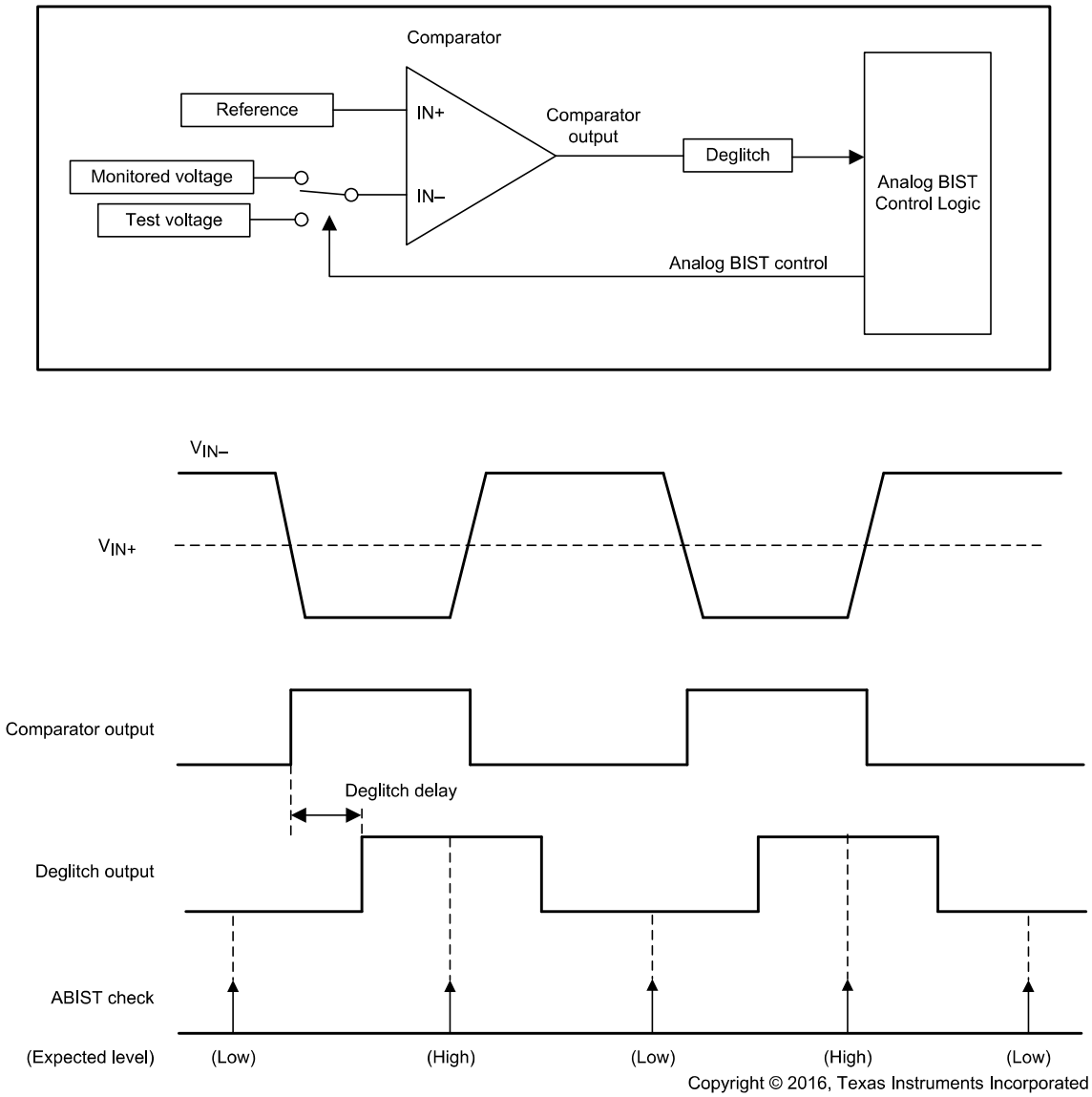


Figure 38. BIST

The clock-monitor BIST is a self-test of the loss of clock function. The enabled diagnostics emulates the clock failure that causes the clock monitor output to toggle. The toggling pattern of the clock monitor is checked by the analog BIST during the self-test, however; the actual oscillator frequency (20 MHz) does not change.

In parallel to the analog BIST, the logical BIST runs stuck-at-fault patterns for logical integrity checking.

The analog and logical BISTs automatically occur whenever the PGA411-Q1 device is in the DIAGNOSTICS state. The result of the analog BIST is monitored on the ABISTF bit while the result of the logic BIST fault is monitored by the LBISTF bit in the DEV_STAT4 register.

The user can manually run the anlog and logic BISTs by setting the ABIST_EN or LBIST_EN bits in DEV_CONTROL2 register. These bits are also used to monitor the BIST run procedure. During the anlog BIST or logic BIST procedure, the ABIST_EN or LBIST_EN bits are held (logical 1) until the procedure is complete after which these bits reset (logical 0).

After reset, the system can read the ABISTF and LBISTF flags for faults during the BIST process.

Figure 39 shows the progress flow of the BIST.

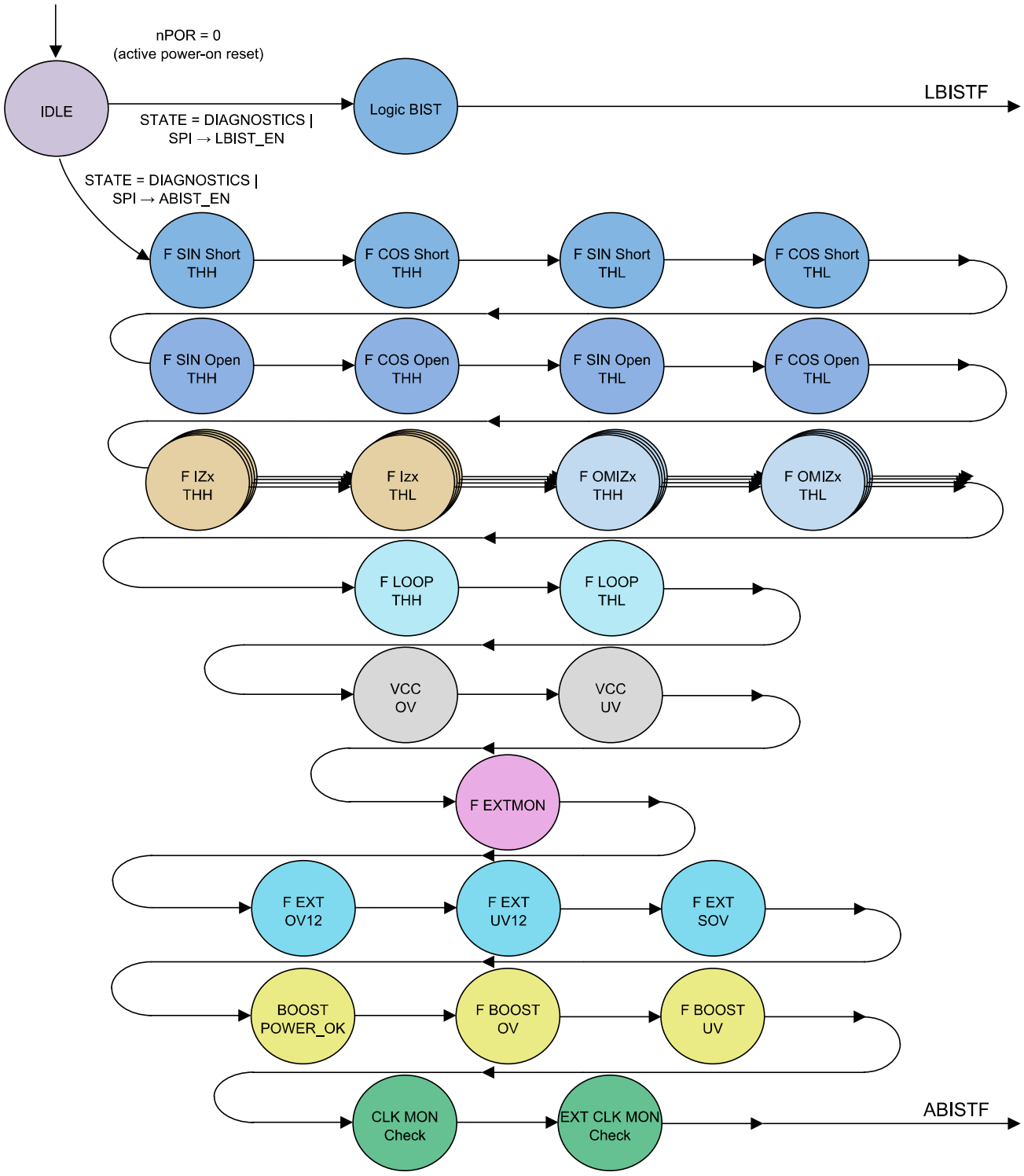


Figure 39. BIST Progress Flow

7.4.6.2 Device Configuration CRC Protection

A CRC-check algorithm is implemented to verify that the contents of the SPI register are programmed correctly. The CRC controller is a diagnostic module that performs a CRC calculation to verify the integrity of the SPI-mapped register space. A checksum representing the content of the diagnostic registers is obtained when the content is read into the CRC controller. The CRC controller must calculate the checksum for a set of data and then compare the calculated checksum value against a predetermined, *good* checksum value calculated by the system MCU.

The CRC check uses a standard CRC-8 (ATM HEC) polynomial, X8 + X2 + X + 1, with an initial seed value 0xFF. The calculation is broken up into 8-bit chunks to optimize implementation with the ordering convention from LS Byte to MS Byte going from LS bit to MS bit. The calculation of a 192-bit string protected by the CRC occurs in a byte-wise order. For example, if the 192-bit register value (in hex) is 8F C0 00 C0 AA AA 07 F2 1C 00 03 8F 05 14 00 00 02 00 00 00 00 then the CRC calculation would be done on the following rearranged string 00 00 00 00 02 00 00 14 05 00 14 05 8F 03 00 1C F2 07 AA AA C0 00 C0 8F.

Table 7 lists the registers that are protected by CRC protection.

Table 7. Configuration CRC Data Bus Order

REGISTER		192-BIT BUS ORDERING
NAME	DATA SPLIT	
DEV_OVUV1	DEV_OVUV1 [15:0]	[MSB] 191:176
DEV_OVUV2	0s pad [15:9]	175:169
	DEV_OVUV2 [8:0]	168:160
DEV_OVUV3	DEV_OVUV3 [15:0]	159:144
DEV_OVUV4	0s pad [15:11]	143:139
	DEV_OVUV4 [10:0]	138:128
DEV_OVUV5	0s pad [15:13]	127:125
	DEV_OVUV5 [12:10]	124:122
	0s pad [9:0]	121:112
DEV_OVUV6	0s pad [15:10]	111:106
	DEV_OVUV6 [9:0]	105:96
DEV_TLOOP_CFG	0s pad [15:11]	95:91
	DEV_TLOOP_CFG [10:0]	90:80
DEV_AFE_CFG	0s pad [15:4]	79:68
	DEV_AFE_CFG [3:0]	67:64
DEV_PHASE_CFG	DEV_PHASE_CFG [15:0]	63:48
DEV_CONFIG1	0s pad [15:9]	47:41
	DEV_CONFIG1 [8:7]	40:39
	0s pad [6]	38
	DEV_CONFIG1 [5:0]	37:32
DEV_CONTROL1	0s pad [15:14]	31:30
	DEV_CONTROL1 [13]	29
	0s pad [12]	28
	DEV_CONTROL1 [11:0]	27:16
DEV_CONTROL2	0s pad [15:6]	15:6
	DEV_CONTROL2 [5:0]	5:0 [LSB]

The following procedure lists steps for a successful configuration CRC calculation:

1. The MCU writes the desired data to the configuration and control registers when the PGA411-Q1 device is in the DIAGNOSTICS state.

   If the DEV_CONTROL1 and DEV_CONTROL2 registers are updated with new data, the device requires unlocking by entering a SPI unlock sequence in the DEV_UNLK_CTRL1 register. See the *Device and EEPROM Unlock Procedure* section for more information.

2. The MCU calculates the correct configuration CRC and applies the final value at the RCRC bit-field in the DEV_CRC register.
3. The CRC check is enabled by setting the CRCCTL bit in the DEV_CRC_CTRL1 register.
4. A CRC check result can be monitored by the FRCRC bit in the DEV_STAT1 register.
5. **Optional**: In case of a CRC mismatch, the fault FRCRC bit is set while the MCU checks the internally calculated CRC result of the device by reading the CRCRC bits in the CRCCALC register. When the value in the CRCRC bit-field matches the value of the RCRC bit-field, the CRC check ends with a satisfactory result.

Table 8 lists a few CRC-8 examples when applied to a 192-bit string.

Table 8. CRC-8 Calculation Examples

192-BIT BUS ORDERING VALUE	CRC-8
0 x 05050505050505050505050505050505050505050505050505	0xBD
0 x 0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A0A	0xA9
0 x 53E53E53E53E53E53E53E53E53E5353E53E53E53E53E5	0x2C
0 x 4AC4AC4AC4AC4AC4AC4AC4AC4AC4A4AC4AC4AC4AC4AC4	0xAE
0 x 78F78F78F78F78F78F78F78F78F78F7878F78F78F78F78F7	0x5E

7.4.6.3 Digital-Output Signal Monitor

The digital-output signal monitor is a real-time logic-level monitor used to monitor the pin state of the PGA411-Q1 digital-output pins for further system-mismatch monitoring. The monitor signals (Sxxx) are reported directly into the SPI memory space. Figure 40 shows the functionality of the output monitor.

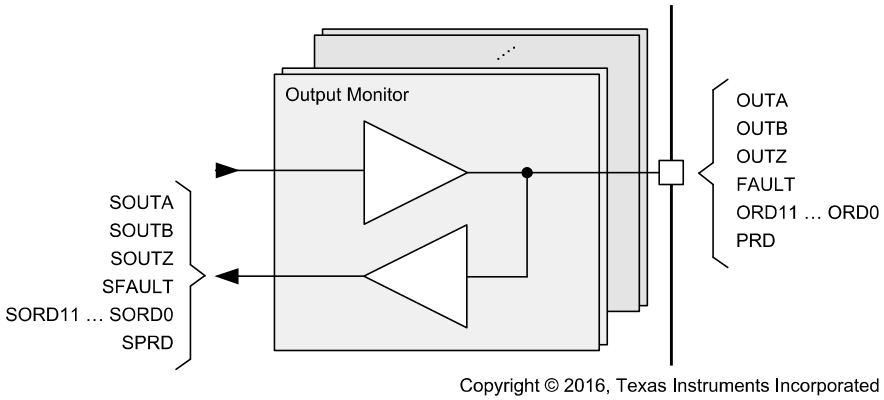


Figure 40. Digital Output Signal Monitor

The monitored digital output pins include the OUTA, OUTB, OUTZ, and FAULT pins reported by the respective SPI flags (SOUTA, SOUTB, SOUTZ, and SFAULT) in the DEV_STAT4 register. The monitor signal of the ORD11 through ORD0 pins and the PRD pin are reported by the SORD and SPRD bits in the DEV_STAT2 register.

The output signal monitor is configured in a way that the PGA411-Q1 device does act when a signal mismatch occurs. The only exception to this rule is when the FAULT pin monitor detects an output mismatch. The FAULT pin signals the IOFAULT fault and transitions the device into the FAULT state as described in the *FAULT State* section.

7.4.6.4 Output Data Parity

For increased safety the PGA411-Q1 device provides a data-parity check output. This check is available through the parallel-data output by using the PRD pin or by reading the output data through the SPI as the PRD bit in the DEV_STAT5 register (angle output) or the DEV_STAT6 (velocity output) register.

The parity-bit calculation for both the parallel data output and SPI is a simple exclusive or (XOR) logic calculation on all ORD bits. Use Equation 16 to calculate the parity (PRD).

PRD = b ^ b ^ ORD[11] ^ ORD[10] ^ ORD[9] ^ ORD[8] ^ ORD[7] ^ ORD[6] ^ ORD[5] ^ ORD[4] ^ ORD[3] ^ ORD[2] ^

ORD[1] ^ ORD[0]

where

- b is 0 for angle and positive velocity or 1 for negative velocity (16)

7.5 Programming

The PGA41x-Q1 SPI includes a four-wire SPI using the following pins:

NCS SPI chip select (active low)

SCLK SPI clock

SDI SPI slave in and master out (SIMO)

SDO SPI slave out and SPI master in (SOMI, tri-state output)

In this case the resolver-to-digital converter is always configured as a slave device.

The SPI frame size is 32 bits, with an MSB-first alignment using the assignments shown in Figure 41.

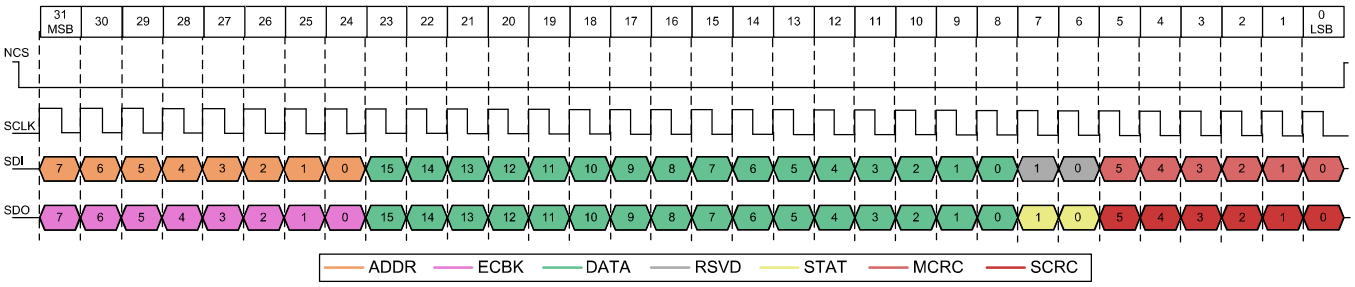


Figure 41. 32-Bit SPI Frame

The master-to-slave communication is 8 bits for address, 16 bits for data, 2 reserved bits (always 00), and 6 bits for CRC.

The slave-to-master response is 8 bits for address echo, 16 bits for data, 2 bits for status, and 6 bits for CRC.

The SPI does not support *back-to-back* SPI frame operation. After each SPI transfer the NCS pin must go from low to high, before the next SPI transfer can begin. The minimum time, t_{w_cs}, between two SPI commands during which the NCS pin must remain high is 200 ns.

The PGA411 device SPI response frame is always one SPI transfer behind the SPI master frame.

NOTE

Upon receiving a SPI read of the angle or velocity data, the PGA411-Q1 goes through 1 to 2 clock cycles to load the angle or velocity data into the SPI to send out.

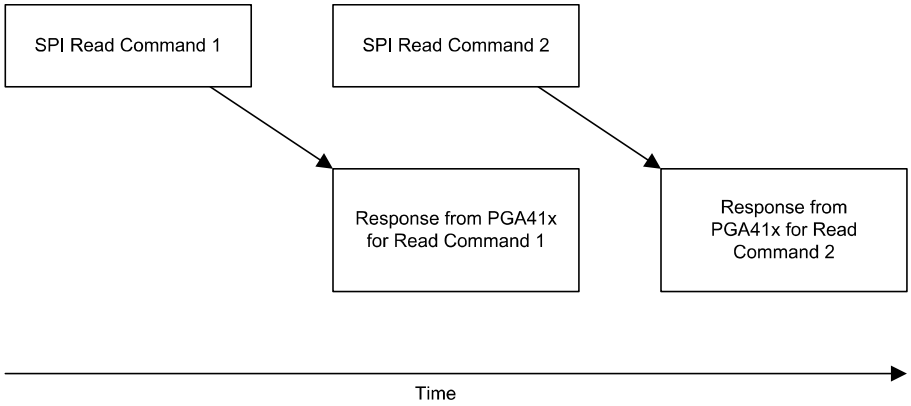


Figure 42. PGA411-Q1 SPI Response Frames

Programming (continued)

7.5.1 Address and Address-Echo Field

In the master SPI frame the address field specifies the register address that is either written to or read from. In the slave SPI frame the address-echo field contains the address of the previously accessed register.

7.5.2 Data Field

In both the SPI master and SPI slave frames the data field contains the 16-bit (MSB ordered) data.

7.5.3 Status Field

The SPI slave frame contains two bits that report the status of the SPI Communication. Table 9 lists the error that is indicated by each SPI status value.

Table 9. SPI Status or Fault Bits

VALUE (HEX)	STATUS DESCRIPTION	PRIORITY
0x0	No Error	4
0x1	SPI CRC Error or Invalid SPI Clock	1
0x2	Data Output mismatch	2
0x3	Address Error	3

A higher priority fault always supersedes a lower priority fault.

NOTE

The data field value in a response frame which includes an error (0x1, 0x2, 0x3) may not be correct and should be discarded.

The DEV_STAT4 register must be read before the DEV_STAT1 register to see when the SPI_ERR flag is set. Reading the DEV_STAT1 register first clears the SPI STAT bits which clears the SPI_ERR flag.

7.5.4 SPI Frame CRC Field

The SPI uses the 24 most significant bits of the SPI frame to generate a CRC value or to check for SPI CRC errors. The polynomial in Equation 17 is applied for CRC calculation on both the master and slave SPI frames.

$$SPI\_CRC6 = X6 + X4 + X3 + X + 1 \quad (17)$$

The operation occurs one bit at a time and begins with the MSB. The initial seed value is 0x3F.

Table 10 lists a set of SPI CRC examples.

Table 10. SPI CRC Examples

24-BIT SPI FRAME	CRC-6
0xAE0000	0x11
0x950055	0x22
0x855555	0x29
0x0D2FFE	0x0D
0x85FFFF	0x38

The following shows example code for calculating the SPI CRC-6 Code.

```
function [5:0] crc6_calc;
integer i;
reg inv;
begin

crc6_calc = 6'h3f; // seed value
// polynomial: x^6+x^4+x^3+x+1
for (i=23;i>=0;i=i-1) begin
inv = crc6_calc[5] ^ data_in[i];
crc6_calc[5] = crc6_calc[4];
crc6_calc[4] = crc6_calc[3] ^ inv;
crc6_calc[3] = crc6_calc[2] ^ inv;
crc6_calc[2] = crc6_calc[1];
crc6_calc[1] = crc6_calc[0] ^ inv;
crc6_calc[0] = inv;
end end endfunction
```

NOTE

The SPI frame CRC uses a different polynomial (CRC-6) than the EEPROM CRC (CRC-8). In the equation above ^ represents the bitwise XOR operator and data_in is the 24-bit SPI frame.

7.5.5 Device and EEPROM Unlock Procedure

To access the DEV_CONTROL1 and DEV_CONTROL2 registers, a predefined device unlock sequence must be applied to the DEV_UNLK_CTRL1 register in the following order:

1. Write 0x000F to DEV_UNLK_CTRL1
2. Write 0x0055 to DEV_UNLK_CTRL1
3. Write 0x00AA to DEV_UNLK_CTRL1
4. Write 0x00F0 to DEV_UNLK_CTRL1

To access the DEV_EE_CTRL1, a predefined EEPROM unlock sequence must be applied to the DEV_EE_CTRL4 register in the following order:

1. Write 0x000F to DEV_EE_CTRL4
2. Write 0x0055 to DEV_EE_CTRL4
3. Write 0x00AA to DEV_EE_CTRL4
4. Write 0x00F0 to DEV_EE_CTRL4

In each case the full length of the sequence write time cannot exceed 10 ms.

7.6 Register Maps

7.6.1 SPI Register Map Layout Configuration

Table 4 provides an overview of each register located in the PGA411-Q1 SPI memory map. For more details refer to the corresponding REGMAP register (see Table 11).

SPI Memory Map

Register Location	Register Name	SPI Read Address	SPI Write Address	Write State	Configuration CRC
0x00	DEV_OVUV1	0x53	0x87	DIAG	YES
0x01	DEV_OVUV2	0x6B	0x26		Yes
0x02	DEV_OVUV3	0x65	0x17		Yes
0x03	DEV_OVUV4	0xEC	0x39		Yes
0x04	DEV_OVUV5	0x52	0x75		Yes
0x05	DEV_OVUV6	0xE9	0x83		Yes
0x06	DEV_TLOOP_CFG	0 xA6	0x42		Yes
0x07	DEV_AFE_CFG	0xC2	0x91		Yes
0x08	DEV_PHASE_CFG	0 x57	0x85		Yes
0x09	DEV_CONFIG1	0xBE	0xEB		Yes
0x0A	DEV_CONTROL1 (1)	0x90	0x0D		Yes
0x0B	DEV_CONTROL2 (1)	0x63	0x38		Yes
0x0C	DEV_CONTROL3	0xDD	0xAE	All	No
0x0D	DEV_STAT1	0x81	N/A (Read-only register)		No
0x0E	DEV_STAT2	0x4D			No
0x0F	DEV_STAT3	0x84			No
0x10	DEV_STAT4	0x1F			No
0x11	DEV_STAT5	0x41			No
0x12	DEV_STAT6	0x6F			No
0x13	DEV_STAT7	0xE1			No
0x14	DEV_CLCRC	0x4F	0xFC	DIAG	No
0x15	DEV_CRC	0x0F	0xE7		No
0x16	CRCCALC	0xD9	N/A (Read-only register)		No
0x17	DEV_EE_CTRL1 (2)	0xE3	0x6E	DIAG	No
0x18	DEV_CRC_CTRL1	0x7A	0xB6		No
0x19	DEV_EE_CTRL4	0xBA	0x56		No
0x1A	DEV_UNLK_CTRL1	0x64	0x95		No

(1) Device unlock sequence required in order to access register.
(2) EEPROM space unlock sequence required in order to access register.

NOTE

The configuration registers that are accessible only in the DIAGNOSTICS state cannot be written in case the PGA411-Q1 device is in the NORMAL operating state. Any attempt to do so causes the *Status Bit Field 0x03* response (such as *Address Not Found*). However, these registers can be read in any state.

7.6.2 REGMAP Registers

Table 11 lists the memory-mapped registers for the REGMAP. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

Table 11. REGMAP Registers

Offset	Acronym	Section
0h	DEV_OVUV1	Go
1h	DEV_OVUV2	Go
2h	DEV_OVUV3	Go
3h	DEV_OVUV4	Go
4h	DEV_OVUV5	Go
5h	DEV_OVUV6	Go
6h	DEV_TLOOP_CFG	Go
7h	DEV_AFE_CFG	Go
8h	DEV_PHASE_CFG	Go
9h	DEV_CONFIG1	Go
Ah	DEV_CONTROL1	Go
Bh	DEV_CONTROL2	Go
Ch	DEV_CONTROL3	Go
Dh	DEV_STAT1	Go
Eh	DEV_STAT2	Go
Fh	DEV_STAT3	Go
10h	DEV_STAT4	Go
11h	DEV_STAT5	Go
12h	DEV_STAT6	Go
13h	DEV_STAT7	Go
14h	DEV_CLCRC	Go
15h	DEV_CRC	Go
16h	CRCCALC	Go
17h	DEV_EE_CTRL1	Go
18h	DEV_CRC_CTRL1	Go
19h	DEV_EE_CTRL4	Go
1Ah	DEV_UNLK_CTRL1	Go

7.6.2.1 DEV_OVUV1 Register (Offset = 0h) [Factory Settings = 8B40h]

DEV_OVUV1 is shown in Figure 43 and described in Table 12.

Figure 43. DEV_OVUV1 Register

15	14	13	12	11	10	9	8
EXTOUT_GL				EXTILIMTH_L1_2			EXTILIMTH_H1_2
R/W-1000b				R/W-101b			R/W-101b
7	6	5	4	3	2	1	0
EXTILIMTH_H1_2		OSHORTL			OSHORTH		
R/W-111b		R/W-000b			R/W-000b		

Table 12. DEV_OVUV1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-12	EXTOUT_GL	R/W	1000b	Exciter Output (Pre-Amplifier) Gain Select: 0000: 1.15 0001: 1.20 0010: 1.25 0011: 1.30 0100: 1.35 0101: 1.40 0110: 1.45 0111: 1.50 1000: 1.55 1001: 1.60 1010: 1.65 1011: 1.70 1100: 1.75 1101: 1.80 1110: 1.85 1111: 1.90
11-9	EXTILIMTH_L1_2	R/W	101b	Exciter Amplifier Current Limit Low Level (current flow from OE1 into OE2): 000 -140 mA 001 -150 mA 010 -165 mA 011 -180 mA 100 -200 mA 101 -230 mA 110 -550 mA (not recommended) 111 -550 mA (not recommended)

Table 12. DEV_OVUV1 Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
8-6	EXTILIMTH_H1_2	R/W	101b	Exciter Amplifier Current Limit High Level (current flow from OE2 into OE1): 000: 150 mA 001: 165 mA 010: 180 mA 011: 200 mA 100: 225 mA 101: 260 mA 110: 300 mA 111: 360 mA
5-3	OSHORTL	R/W	000b	OSIN and OCOS Short Circuit Low Threshold level select: 000: V_{CC} × 0.475 V 001: V_{CC} × 0.45 V 010: V_{CC} × 0.425 V 011: V_{CC} × 0.4 V 100: V_{CC} × 0.375 V 101: V_{CC} × 0.35 V 110: V_{CC} × 0.325 V 111: V_{CC} × 0.3 V
2-0	OSHORTH	R/W	000b	OSIN and OCOS Short Circuit High Threshold level select: 000: V_{CC} × 0.525 V 001: V_{CC} × 0.55 V 010: V_{CC} × 0.575 V 011: V_{CC} × 0.6 V 100: V_{CC} × 0.625 V 101: V_{CC} × 0.65 V 110: V_{CC} × 0.675 V 111: V_{CC} × 0.7 V

7.6.2.2 DEV_OVUV2 Register (Offset = 1h) [Factory Settings = 00EDh]

DEV_OVUV2 is shown in Figure 44 and described in Table 13.

Figure 44. DEV_OVUV2 Register

15	14	13	12	11	10	9	8
RESERVED							XEXT_AMP
R-0000000b							R/W-0b
7	6	5	4	3	2	1	0
TRDHL		DVMSENH			DVMSENL		
R/W-11b		R/W-101b			R/W-101b		

Table 13. DEV_OVUV2 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-9	RESERVED	R	0000000b	
8	XEXT_AMP	R/W	0b	External exciter amplifier selection bit. 0: Use the internal exciter amplifier. 1: Use an external exciter amplifier.
7-6	TRDHL	R/W	11b	Tracking Loop Error deglitch select: (AMODE = L) 00: 90 ms 01: 120 ms 10: 150 ms 11: 180 ms (AMODE = H) 00: 2 ms 01: 4 ms 10: 6 ms 11: 8 ms
5-3	DVMSENH	R/W	101b	IZx Input Integrity Check High Threshold level select: 000: 2.6 V 001: 2.75 V 010: 2.9 V 011: 3.05 V 100: 3.2 V 101: 3.35 V 110: 3.5 V 111: 3.65 V
2-0	DVMSENL	R/W	101b	IZx Input Integrity Check Low Threshold level select: 000: 2.4 V 001: 2.25 V 010: 2.1 V 011: 1.95 V 100: 1.8 V 101: 1.65 V 110: 1.5 V 111: 1.35 V

7.6.2.3 DEV_OVUV3 Register (Offset = 2h) [Factory Settings = FCFFh]

DEV_OVUV3 is shown in Figure 45 and described in Table 14.

Figure 45. DEV_OVUV3 Register

15	14	13	12	11	10	9	8
EXTUVT			EXTOVT			OVIZL	
R/W-111b			R/W-111b			R/W-00b	
7	6	5	4	3	2	1	0
OVIZH		OOPENTHL			OOPENTHH		
R/W-11b		R/W-111b			R/W-111b		

Table 14. DEV_OVUV3 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-13	EXTUVT	R/W	111b	Exciter Amplifier Undervoltage Deglitch: (EXTUVF_CFG = 0x) /(EXTUVF_CFG = 10) 000: 55 µs / 000: 1.2 µs 001: 105 µs / 001: 3.2 µs 010: 155 µs / 010: 5.2 µs 011: 205 µs / 011: 7.2 µs 100: 255 µs / 100: 9.2 µs 101: 305 µs / 101: 11.2 µs 110: 355 µs / 110: 13.2 µs 111: 405 µs / 111: 15.2 µs
12-10	EXTOVT	R/W	111b	Exciter Amplifier Overvoltage Deglitch: 000: 1.2 µs 001: 3.2 µs 010: 5.2 µs 011: 7.2 µs 100: 9.2 µs 101: 11.2 µs 110: 13.2 µs 111: 15.2 µs
9-8	OVIZL	R/W	00b	IZx Input Overvoltage Low Threshold level select: 00: V_{CC} × 0.25 V 01: V_{CC} × 0.2 V 10: V_{CC} × 0.15 V 11: V_{CC} × 0.1 V
7-6	OVIZH	R/W	11b	IZx Input Overvoltage High Threshold level select: 00: V_{CC} × 0.75 V 01: V_{CC} × 0.8 V 10: V_{CC} × 0.85 V 11: V_{CC} × 0.9 V

Table 14. DEV_OVUV3 Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
5-3	OOPENTHL	R/W	111b	OSIN/OCOS Open Circuit Low Threshold level select: 000: V_{CC} × 0.25 V 001: V_{CC} × 0.225 V 010: V_{CC} × 0.2 V 011: V_{CC} × 0.175 V 100: V_{CC} × 0.15 V 101: V_{CC} × 0.125 V 110: V_{CC} × 0.1 V 111: V_{CC} × 0.075 V
2-0	OOPENTHH	R/W	111b	OSIN/OCOS Open Circuit High Threshold level select: 000: V_{CC} × 0.75 V 001: V_{CC} × 0.775 V 010: V_{CC} × 0.8 V 011: V_{CC} × 0.825 V 100: V_{CC} × 0.85 V 101: V_{CC} × 0.875 V 110: V_{CC} × 0.9 V 111: V_{CC} × 0.925 V

7.6.2.4 DEV_OVUV4 Register (Offset = 3h) [Factory Settings = 07E2h]

DEV_OVUV4 is shown in Figure 46 and described in Table 15.

Figure 46. DEV_OVUV4 Register

15	14	13	12	11	10	9	8
RESERVED					TSHORT		
R-00000b					R/W-111b		
7	6	5	4	3	2	1	0
TEXTMON			AUTOPHASE_CFG		VEXT_CFG	nBOOST_FF	FSHORT_CFG
R/W-111b			R/W-00b		R/W-0b	R/W-1b	R/W-0b

Table 15. DEV_OVUV4 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-11	RESERVED	R	00000b	
10-8	TSHORT	R/W	111b	OSIN/OCOS Short Circuit Deglitch Select: 000: 35 µs 001: 50 µs 010: 65 µs 011: 80 µs 100: 95 µs 101: 110 µs 110: 125 µs 111: 140 µs
7-5	TEXTMON	R/W	111b	Exciter Monitor Faults response delay time - used for FEXTMONL and FEXTMONH faults: 000: 35 µs - setting not recommended 001: 50 µs - setting not recommended 010: 65 µs - use at high exciter frequencies only 011: 80 µs - use at high exciter frequencies only 100: 95 µs - use at high exciter frequencies only 101: 110 µs 110: 125 µs 111: 140 µs Setting the deglitch timing too low may cause FEXTMONL/FEXTMONH to always indicate a fault. The deglitch time needs to be larger than one period of the exciter.
4-3	AUTOPHASE_CFG	R/W	00b	Auto-Phase Correction configuration sets the Auto Phase behavior in a way that out of the two input signals (i.e. SIN and COS) the signal with better integrity is chosen to set and reset/time capture the implemented mismatch timers as well as the standard detection which auto selects the used signal. 00: Enhanced Auto Phase by using Short Fault Detection Threshold Levels 01: Enhanced Auto Phase by using Open Fault Detection Threshold Levels x1: Standard Auto Phase configuration
2	VEXT_CFG	R/W	0b	VEXT Configuration bit: set to 1 when the VEXT supply is used for an external exciter amplifier. Set to 0 allow normal boost VEXT monitoring.

Table 15. DEV_OVUV4 Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
1	nBOOST_FF	R/W	1b	Boost Feedforward control: set to 1 to turn feed forward off set to 0 to turn it on.
0	FSHORT_CFG	R/W	0b	0: AND of sin, cos short fault condition sets FOSHORT 1: OR of sin, cos short fault condition sets FOSHORT

7.6.2.5 DEV_OVUV5 Register (Offset = 4h) [Factory Settings = 1C00h]

DEV_OVUV5 is shown in Figure 47 and described in Table 16.

Figure 47. DEV_OVUV5 Register

15	14	13	12	11	10	9	8
RESERVED			TOPEN			RESERVED	
R-000b			R/W-111b			R-00b	
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 16. DEV_OVUV5 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-13	RESERVED	R	000b	
12-10	TOPEN	R/W	111b	OSIN/OCOS Open Circuit Deglitch Select: 000: 35 µs 001: 50 µs 010: 65 µs 011: 80 µs 100: 95 µs 101: 110 µs 110: 125 µs 111: 140 µs
9-0	RESERVED	R	0000000000b	

7.6.2.6 DEV_OVUV6 Register (Offset = 5h) [Factory Settings = 038Fh]

DEV_OVUV6 is shown in Figure 48 and described in Table 17.

Figure 48. DEV_OVUV6 Register

15	14	13	12	11	10	9	8
RESERVED						IZTHL	
R-000000b						R/W-111b	
7	6	5	4	3	2	1	0
IZTHL	BOOST_VEXT_MASK	RESERVED		LPETHL		LPETHH	
R/W-111b	R/W-0b	R/W-00b		R/W-11b		R/W-11b	

Table 17. DEV_OVUV6 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-10	RESERVED	R	000000b	
9-7	IZTHL	R/W	111b	IZx Input High/Low Overvoltage Deglitch select: 000: 1.2 µs 001: 3.2 µs 010: 5.2 µs 011: 7.2 µs 100: 9.2 µs 101: 11.2 µs 110: 13.2 µs 111: 15.2 µs
6	BOOST_VEXT_MASK	R/W	0b	Set to 1 to mask BOOST_VEXT_GOOD, OV and UV and EXCIT_SOV1,2 during ABIST
5-4	RESERVED	R/W	00b	
3-2	LPETHL	R/W	11b	Tracking Loop Error Low Threshold level select: 00: 0.1 V 01: 0.2 V 10: 0.25 V 11: 0.8 V
1-0	LPETHH	R/W	11b	Tracking Loop Error High Threshold level select: 00: 0.1 V 01: 0.2 V 10: 0.25 V 11: 0.8 V

7.6.2.7 DEV_TLOOP_CFG Register (Offset = 6h) [Factory Settings = 0514h]

DEV_TLOOP_CFG is shown in Figure 49 and described in Table 18.

Figure 49. DEV_TLOOP_CFG Register

15	14	13	12	11	10	9	8
RESERVED					MKP		DKP
R-00000b					R/W-10b		R/W-100b
7	6	5	4	3	2	1	0
DKP		OHYS		SENCLK	DKI		
R/W-100b		R/W-01b		R/W-0b	R/W-100b		

Table 18. DEV_TLOOP_CFG Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-11	RESERVED	R	00000b	
10-9	MKP	R/W	10b	Digital Tracking Loop Gain Multiplier: (10/12 bit Mode, AMODE = H) 00: 8 01: 16 10: 32 11: 64
8-6	DKP	R/W	100b	Digital Tracking Loop Gain Constant: (10 Bit Mode) 000: 16 001: 32 010: 64 011: 128 100: 256 101: 512 (12 Bit Mode) 000: 4 001: 8 010: 16 011: 32 100: 64 101: 128
5-4	OHYS	R/W	01b	Output Angle Hysteresis: 00: Disabled 01: 1 LSB 1x: DO NOT USE (may result in angle errors at low rotation speed)
3	SENCLK	R/W	0b	Exciter Clock input Select: 0: Exciter Clock is Referenced to system Clock 1: Not recommended - exciter may not function

Table 18. DEV_TLOOP_CFG Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
2-0	DKI	R/W	100b	PI Controller Feedback Integration Weight: 000: 2^8 bits 001: 2^9 bits 010: 2^{10} bits 011: 2^{11} bits 100: 2^{12} bits 101: 2^{13} bits 110: 2^{14} bits 111: 2^{15} bits

7.6.2.8 DEV_AFE_CFG Register (Offset = 7h) [Factory Settings = 0005h]

DEV_AFE_CFG is shown in Figure 50 and described in Table 19.

Figure 50. DEV_AFE_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
RESERVED				GAINCOS		GAINSIN	
R-0h				R/W-01b		R/W-01b	

Table 19. DEV_AFE_CFG Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-4	RESERVED	R	000h	
3-2	GAINCOS	R/W	01b	COS Input AFE Gain: 00: 0.75 01: 1 10: 2.25 11: 3.50
1-0	GAINSIN	R/W	01b	SIN Input AFE Gain: 00: 0.75 01: 1 10: 2.25 11: 3.50

7.6.2.9 DEV_PHASE_CFG Register (Offset = 8h) [Factory Settings = 1400h]

DEV_PHASE_CFG is shown in Figure 51 and described in Table 20.

Figure 51. DEV_PHASE_CFG Register

15	14	13	12	11	10	9	8
EXTUVF_CFG		PDEN	APEN	EXTMODE		EXTOUT	
R/W-00b		R/W-0b	R/W-1b	R/W-01b		R/W-0000b	
7	6	5	4	3	2	1	0
EXTOUT		PHASEDEMOD					
R/W-0000b		R/W-000000b					

Table 20. DEV_PHASE_CFG Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-14	EXTUVF_CFG	R/W	00b	Exciter fault flag configuration bits - used to select how the exciter UV1 and UV2 indicators are processed to form the exciter UV fault flag. 0x: UV1 OR UV2 w/ 50 to 400 µs deglitching on OR inputs 10: UV1 AND UV2 w/ 1 to 15 µs deglitching on AND output 11: UV1 OR UV2 OR (UV1 AND UV2) with deglitching as defined above
13	PDEN	R/W	0b	Phase Delay Enable: 0: Manual Phase delay is Disabled 1: Manual Phase Delay is Enabled and set by PHASEDEMOD[5:0] Manual Phase delay PDEN takes priority over Auto Phase delay APEN
12	APEN	R/W	1b	Automatic Phase Control Enable: 0: Disabled 1: Enabled
11-10	EXTMODE	R/W	01b	Exciter Mode Select: 00 or 11: Exciter Disabled FAULT = H FEXTMODE = 1 01: $4V_{RMS}$ Mode 10: $7V_{RMS}$ Mode
9-6	EXTOUT	R/W	0000b	Exciter Offset Voltage Adjust (FootRoom): 0000: 2.0 V 0001: 1.9 V 0010: 1.8 V 0011: 1.7 V 0100: 1.6 V 0101: 1.5 V 0110: 1.4 V 0111: 1.3 V 1000: 1.2 V 1001: 1.1 V 1010: 1.0 V 1011: 0.9 V 1100: 0.8 V 1101: 0.7 V 1110: 0.6 V 1111: 0.5 V

Table 20. DEV_PHASE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
5-0	PHASEDEMOD	R/W	000000b	Manual Phase Delay Adjustment: Value [µs] = PHASEDEMOD[4:0] × 0.4 µs PHASEDEMOD[5] is a sign bit: 0: Positive value (1 × value) 1: Negative value (-1 × value)

7.6.2.10 DEV_CONFIG1 Register (Offset = 9h) [Factory Settings = 0002h]

DEV_CONFIG1 is shown in Figure 52 and described in Table 21.

Figure 52. DEV_CONFIG1 Register

15	14	13	12	11	10	9	8
RESERVED							NPLE
R-0000000b							R/W-00b
7	6	5	4	3	2	1	0
NPLE	RESERVED	SELFEXT			MODEVEXT		
R/W-00b	R-0b	R/W-000b			R/W-010b		

Table 21. DEV_CONFIG1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-9	RESERVED	R	0000000b	
8-7	NPLE	R/W	00b	Encoder Number of poles select: 00: 1x 01: 2x 10: 3x 11: 4x
6	RESERVED	R	0b	
5-3	SELFEXT	R/W	000b	Exciter Frequency Select: (SENCLK = 0) 000: 10 kHz 001: 10.87 kHz 010: 11.63 kHz 011: 12.82 kHz 100: 13.89 kHz 101: 15.63 kHz 110: 17.24 kHz 111: 20 kHz
2-0	MODEVEXT	R/W	010b	Exciter Power Supply Voltage Output Select: 000: 10 V 001: 11 V 010: 12 V 011: 13 V 100: 14 V 101: 15 V 110: 16 V 111: 17 V

7.6.2.11 DEV_CONTROL1 Register (Offset = Ah) [Factory Settings = 0000h]

DEV_CONTROL1 is shown in Figure 53 and described in Table 22.

Figure 53. DEV_CONTROL1 Register

15	14	13	12	11	10	9	8
RESERVED		MFOSHORT	RESERVED	MFOSINOPH	MFOCOSOPH	MFOSINOPL	MFOCOSOPL
R-00b		R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b
7	6	5	4	3	2	1	0
MFLOOPE	MEXTOV	MEXTUV	MIZOV	MIZUV	MAFECAL	MEXTMON	DIAGEXIT
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 22. DEV_CONTROL1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-14	RESERVED	R	00b	
13	MFOSHORT	R/W	0b	Mask Input IZ1, IZ2, IZ3, IZ4 Short Fault (FOSHORT) 0: Disabled 1: Enabled
12	RESERVED	R	0b	
11	MFOSINOPH	R/W	0b	Mask Sine Input (IZ2 - IZ4) High Open Fault (FOSINOPH) 0: Disabled 1: Enabled
10	MFOCOSOPH	R/W	0b	Mask Cosine Input (IZ1: IZ3) High Open Fault (FOCOSOPH) 0: Disabled 1: Enabled
9	MFOSINOPL	R/W	0b	Mask Sine Input (IZ2 - IZ4) Low Open Fault (FOSINOPL) 0: Disabled 1: Enabled
8	MFOCOSOPL	R/W	0b	Mask Sine Input (IZ1: IZ3) Low Open Fault (FOCOSOPL) 0: Disabled 1: Enabled
7	MFLOOPE	R/W	0b	Mask Digital Tracking Loop Error Fault (FLOOPE) 0: Disabled 1: Enabled
6	MEXTOV	R/W	0b	Mask Exciter Overvoltage Fault (EXTOV) 0: Disabled 1: Enabled
5	MEXTUV	R/W	0b	Mask Exciter Undervoltage Fault (EXTUV) 0: Disabled 1: Enabled
4	MIZOV	R/W	0b	Mask Input IZ1, IZ2, IZ3, IZ4 Overvoltage (FIZH) 0: Disabled 1: Enabled
3	MIZUV	R/W	0b	Mask Input IZ1, IZ2, IZ3, IZ4 Undervoltage (FIZL) 0: Disabled 1: Enabled

Table 22. DEV_CONTROL1 Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
2	MAFECAL	R/W	0b	Mask AFE Calibration Fault: 0: Disabled 1: Enabled
1	MEXTMON	R/W	0b	Exciter Monitor Faults Mask (FEXTMONL and FEXTMONH) 0: Disabled 1: Enabled
0	DIAGEXIT	R/W	0b	DIAGNOSTIC State Exit. 1: will trigger a device transition from state DIAG to state NORMAL This bit is self-clearing; reading always returns a zero value. This bit can always be written, i.e., it is not write-access protected. A zero-value is used for this bit in the device CRC calculation.

7.6.2.12 DEV_CONTROL2 Register (Offset = Bh) [Factory Settings = 0000h]

DEV_CONTROL2 is shown in Figure 54 and described in Table 23.

Figure 54. DEV_CONTROL2 Register

15	14	13	12	11	10	9	8
ABIST_EN	LBIST_EN	RESERVED					
R/W-0b	R/W-0b	R-000000b					
7	6	5	4	3	2	1	0
RESERVED		RDC_DISABLE	ENINFAULT	ENIOFAULT	ENBISTF	ENEXTMON	ENEXTUV
R-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 23. DEV_CONTROL2 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	ABIST_EN	R/W	0b	Analog built-In self-test Enable (ABIST). This bit returns the value of the ABIST running indicator. This indicator will go high when ABIST is launched, via a write to this reg-bit or during power-up when ABIST is launched automatically, and remain in this state while ABIST is running. A zero-value is used for this bit in the device CRC calculation.
14	LBIST_EN	R/W	0b	Logic built-In self-test Enable (LBIST). This bit returns the value of the LBIST running indicator. This indicator will go high when LBIST is launched, via a write to this reg-bit or during power-up when LBIST is launched automatically, and remain in this state while LBIST is running. A zero-value is used for this bit in the device CRC calculation.
13-6	RESERVED	R	00000000b	
5	RDC_DISABLE	R/W	0b	Resolver To Digital Converter Disable: 0: RDC Analog Front End is Enabled 1: RDC Analog Front End is Disabled
4	ENINFAULT	R/W	0b	Exciter Signal Input Enable Control: 0: The Exciter is Disabled on when detected any of FIZHx, FIZLx, FOSHORT, FOSINOPH, FOSINOPL, FOCOSOPH, FOCOSOPL fault 1: The Exciter will Remain Enabled when a fault is detected
3	ENIOFAULT	R/W	0b	Exciter Digital IO Fault Enable Control: 0: The Exciter is Disabled on a detected IOFAULT fault 1: The Exciter will Remain Enabled when a fault is detected
2	ENBISTF	R/W	0b	Exciter BIST Error Enable Control: : 0: The Exciter is Disabled on a detected BIST fault 1: The Exciter is Enabled regardless of BIST results.
1	ENEXTMON	R/W	0b	Exciter Fault Monitor Enable Control: 0: The Exciter is Disabled on a detected FEXTMONH or FEXTMONL fault 1: The Exciter will Remain Enabled when a fault is detected
0	ENEXTUV	R/W	0b	Exciter Undervoltage Fault Enable Control: 0: The Exciter is Disabled on a detected EXTUV fault 1: The Exciter will Remain Enabled when a fault is detected

7.6.2.13 DEV_CONTROL3 Register (Offset = Ch) [Factory Settings = 0000h]

DEV_CONTROL3 is shown in Figure 55 and described in Table 24.

Figure 55. DEV_CONTROL3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
RESERVED					SPIDIAG	LPEN	EXTEN
R-00000b					R/W-0b	R/W-0b	R/W-0b

Table 24. DEV_CONTROL3 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-3	RESERVED	R	000h	
2	SPIDIAG	R/W	0b	SPI transition from state NORMAL to state DIAG. 1: Transition to DIAG state. Self-clearing bit, reading always returns a zero value.
1	LPEN	R/W	0b	Tracking loop enable control. This control is automatically set to 1 upon device transition to the NORMAL state following a power-on reset. It is also SPI programmable from either the DIAG or NORMAL state. This control is set to 0 when the internal exciter is disabled due to a fault.
0	EXTEN	R/W	0b	Internal Exciter enable control. This control is automatically set to 1 upon device transition to the NORMAL state following a power-on reset. It is also SPI programmable from either the DIAG or NORMAL state. This control is set to 0 when an un-masked fault (see the *Exciter Output, Amplifier, and Power Supply Characteristics* table) becomes active. This state is maintained as long as the fault remains active.

7.6.2.14 DEV_STAT1 Register (Offset = Dh) [Factory Settings = 0000h]

DEV_STAT1 is shown in Figure 56 and described in Table 25.

Figure 56. DEV_STAT1 Register

15	14	13	12	11	10	9	8
FLOOP_CLAMP	FRCRC	FCECRC	FTECRC	EXTILIM	EXTUV	EXTOV	FLOOPE
RC-0b	RC-0b	RC-0b	RC-0b	R-0b	R-0b	R-0b	R-0b
7	6	5	4	3	2	1	0
FOCOSOPL	FOSINOPL	FOCOSOPH	FOSINOPH	STAT		FGOPEN	FOSHORT
R-0b	R-0b	R-0b	R-0b	R-00b		R-0b	R-0b

Table 25. DEV_STAT1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	FLOOP_CLAMP	RC	0b	Digital Tracking loop data clamp flag. This bit will clear on read.
14	FRCRC	RC	0b	Device Configuration and Control register data CRC error flag. This bit will clear on read.
13	FCECRC	RC	0b	User EEPROM space CRC error flag. This bit will clear on read.
12	FTECRC	RC	0b	Trim EEPROM space CRC error flag. This bit will clear on read.
11	EXTILIM	R	0b	Exciter Current Limit Fault. This bit will clear on read.
10	EXTUV	R	0b	Exciter Undervoltage Fault. This bit will clear on read.
9	EXTOV	R	0b	Exciter Overvoltage Fault. This bit will clear on read.
8	FLOOPE	R	0b	Digital Tracking Loop Error Fault. This bit will clear on read.
7	FOCOSOPL	R	0b	Cosine Input (IZ1: IZ3) Low Open Fault. This bit will clear on read.
6	FOSINOPL	R	0b	Sine Input (IZ2 - IZ4) Low Open Fault. This bit will clear on read.
5	FOCOSOPH	R	0b	Cosine Input (IZ1: IZ3) High Open Fault. This bit will clear on read.
4	FOSINOPH	R	0b	Sine Input (IZ2 - IZ4) High Open Fault. This bit will clear on read.
3-2	STAT	R	00b	SPI Interface Status: 00: No Error 01: SPI CRC Error or Invalid SPI Clock during previous frame 10: Data Output mismatch during previous frame 11: Address Error during previous frame This bit will clear on read.
1	FGOPEN	R	0b	Ground Open Fault. This bit will clear on read.
0	FOSHORT	R	0b	Input IZ1, IZ2, IZ3, IZ4 Short Fault. This bit will clear on read.

7.6.2.15 DEV_STAT2 Register (Offset = Eh) [Factory Settings = 0000h]

DEV_STAT2 is shown in Figure 57 and described in Table 26.

Figure 57. DEV_STAT2 Register

15	14	13	12	11	10	9	8
RESERVED	SPRD	SORD					
R-0b	R-0b	R-0b					
7	6	5	4	3	2	1	0
SORD							
R-0b							

Table 26. DEV_STAT2 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	RESERVED	R	0b	
14	SPRD	R	0b	PRD pin Signal Monitor
13-0	SORD	R	0b	ORD[13:0] pin Signal Monitor

7.6.2.16 DEV_STAT3 Register (Offset = Fh) [Factory Settings = 0000h]

DEV_STAT3 is shown in Figure 58 and described in Table 27.

Figure 58. DEV_STAT3 Register

15	14	13	12	11	10	9	8
OMIZ4L	OMIZ2L	OMIZ3L	OMIZ1L	OMIZ4H	OMIZ2H	OMIZ3H	OMIZ1H
RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b	RC-0b
7	6	5	4	3	2	1	0
FIZL4	FIZL2	FIZL3	FIZL1	FIZH4	FIZH2	FIZH3	FIZH1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Table 27. DEV_STAT3 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	OMIZ4L	RC	0b	Sensor input signal IZ4 low reference integrity check indicator: IZ4 voltage level is checked against the DVMSENL selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
14	OMIZ2L	RC	0b	Sensor input signal IZ2 low reference integrity check indicator: IZ2 voltage level is checked against the DVMSENL selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
13	OMIZ3L	RC	0b	Sensor input signal IZ3 low reference integrity check indicator: IZ3 voltage level is checked against the DVMSENL selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
12	OMIZ1L	RC	0b	Sensor input signal IZ1 low reference integrity check indicator: IZ1 voltage level is checked against the DVMSENL selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
11	OMIZ4H	RC	0b	Sensor input signal IZ4 High reference integrity check indicator: IZ4 voltage level is checked against the DVMSENH selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
10	OMIZ2H	RC	0b	Sensor input signal IZ2 High reference integrity check indicator: IZ2 voltage level is checked against the DVMSENH selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
9	OMIZ3H	RC	0b	Sensor input signal IZ3 High reference integrity check indicator: IZ3 voltage level is checked against the DVMSENH selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
8	OMIZ1H	RC	0b	Sensor input signal IZ1 High reference integrity check indicator: IZ1 voltage level is checked against the DVMSENH selected reference. This digital core input is passed thru a 5us de-glitch filter before being logged. This bit will clear on read.
7	FIZL4	R	0b	Input IZ4 Low Overvoltage Fault IZ4 voltage level is checked against the OVIZL selected reference. This bit will clear on read.
6	FIZL2	R	0b	Input IZ2 Low Overvoltage Fault IZ2 voltage level is checked against the OVIZL selected reference. This bit will clear on read.
5	FIZL3	R	0b	Input IZ3 Low Overvoltage Fault IZ3 voltage level is checked against the OVIZL selected reference. This bit will clear on read.
4	FIZL1	R	0b	Input IZ1 Low Overvoltage Fault IZ1 voltage level is checked against the OVIZL selected reference. This bit will clear on read.
3	FIZH4	R	0b	Input IZ4 High Overvoltage Fault IZ4 voltage level is checked against the OVIZH selected reference. This bit will clear on read.

Table 27. DEV_STAT3 Register Field Descriptions (continued)

Bit	Field	Type	Factory Settings	Description
2	FIZH2	R	0b	Input IZ2 High Overvoltage Fault IZ2 voltage level is checked against the OVIZH selected reference. This bit will clear on read.
1	FIZH3	R	0b	Input IZ3 High Overvoltage Fault IZ3 voltage level is checked against the OVIZH selected reference. This bit will clear on read.
0	FIZH1	R	0b	Input IZ1 High Overvoltage Fault IZ1 voltage level is checked against the OVIZH selected reference. This bit will clear on read.

7.6.2.17 DEV_STAT4 Register (Offset = 10h) [Factory Settings = 0000h]

DEV_STAT4 is shown in Figure 59 and described in Table 28.

Figure 59. DEV_STAT4 Register

15	14	13	12	11	10	9	8
FEXTMONH	FEXTMONL	SPI_ERR	FBSTOV	FVDDOC	FTSD2	FEXTMODE	ABISTF
R-0b	RC-0b	RC-0b	R-0b	RC-0b	RC-0b	R-0b	RC-0b
7	6	5	4	3	2	1	0
LBISTF	FVCCOV	FVDDOV	IOFAULT	SFAULT	SOUTA	SOUTB	SOUTZ
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	RC-0b

Table 28. DEV_STAT4 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	FEXTMONH	R	0b	Exciter Monitor IE1, IE2 High fault flag. This bit will clear on read.
14	FEXTMONL	RC	0b	Exciter Monitor IE1, IE2 Low fault flag. This bit will clear on read.
13	SPI_ERR	RC	0b	SPI Communication fault flag.
12	FBSTOV	R	0b	Exciter Power Supply (Boost) Overvoltage flag. This bit will clear on read.
11	FVDDOC	RC	0b	VDD Regulator Overcurrent Flag. This bit will clear on read.
10	FTSD2	RC	0b	Exciter Thermal Warning Fault. This bit will clear on read.
9	FEXTMODE	R	0b	Exciter Mode Fault flag 0: No Fault, 1: The Exciter is disabled via the EXTMODE[1:0] bits
8	ABISTF	RC	0b	Analog BIST (ABIST) Fault Flag. Once set to a '1' , indicating a fault, only a POR or a successful BIST re-run will clear. This bit will also get set if a DIAGEXIT command ocurrs while ABIST is running.
7	LBISTF	R	0b	Logical Bist (LBIST) Fault Flag. Once set to a '1' , indicating a fault, only a POR or a successful BIST re-run will clear.
6	FVCCOV	R	0b	V_{CC} Overvoltage Fault Flag. This bit will clear on read.
5	FVDDOV	R	0b	VDD Overvoltage Fault Flag. This bit will clear on read.
4	IOFAULT	R	0b	Digital Input / Output pin Missmatch Fault. This bit will clear on read.
3	SFAULT	R	0b	FAULT pin Signal Monitor
2	SOUTA	R	0b	OUTA pin Signal Monitor
1	SOUTB	R	0b	OUTB pin Signal Monitor
0	SOUTZ	RC	0b	OUTZ pin Signal Monitor

7.6.2.18 DEV_STAT5 Register (Offset = 11h) [Factory Settings = 0000h]

DEV_STAT5 is shown in Figure 60 and described in Table 29.

Figure 60. DEV_STAT5 Register

15	14	13	12	11	10	9	8
RESERVED	PRD	ORDCLOCK	ORDANGLE				
R-0b	R-0b	R-0b	R-0b				
7	6	5	4	3	2	1	0
ORDANGLE							
R-0b							

Table 29. DEV_STAT5 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	RESERVED	R	0b	
14	PRD	R	0b	ORD Angle Value Parity Bit (Even Parity) PRD is an XOR function of ORD[13:0] Outputs
13	ORDCLOCK	R	0b	ORD Clock Output
12-0	ORDANGLE	R	0b	Angle Position Output Value (Right Justified). Angle values are stored in unsigned 2's complement format. ORD12 is always 0. ORD11 and ORD10 will be 0 if the PGA411-Q1 is in 10-bit mode.

7.6.2.19 DEV_STAT6 Register (Offset = 12h) [Factory Settings = 0000h]

DEV_STAT6 is shown in Figure 61 and described in Table 30.

Figure 61. DEV_STAT6 Register

15	14	13	12	11	10	9	8
RESERVED	PRD	ORDVELOCITY					
R-0b	R-0b	R-0b					
7	6	5	4	3	2	1	0
ORDVELOCITY							
R-0b							

Table 30. DEV_STAT6 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15	RESERVED	R	0b	
14	PRD	R	0b	ORD Angle Value Parity Bit (Even Parity) PRD is an XOR function of ORD[13:0] Outputs
13-0	ORDVELOCITY	R	0b	Rotation Velocity Output Value (Right Justified). The velocity value is stored as signed 2's compliment with the MSB being the sign based on resolution selected (bit 9 for 10-bit or bit 11 for 12-bit). Ignore bits higher than the MSB. Refer to the SPI Output section of the Feature Description for how to translate the ORDVELOCITY bit values into RPM values.

7.6.2.20 DEV_STAT7 Register (Offset = 13h) [Factory Settings = 0000h]

DEV_STAT7 is shown in Figure 62 and described in Table 31.

Figure 62. DEV_STAT7 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
FAFECAL	DEVSTATE	OPTID				REVID	
R-0b	R-0b	R				R	

Table 31. DEV_STAT7 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	0b	
7	FAFECAL	R	0b	Analog Front End Zero-Offset Calibration Fault:
6	DEVSTATE	R	0b	Device State Monitor: 0: Diagnostic State 1: Normal State
5-3	OPTID	R	-	Option Identification Field
2-0	REVID	R	-	Device Revision Information

7.6.2.21 DEV_CLCRC Register (Offset = 14h) [Factory Settings = 00CEh]

DEV_CLCRC is shown in Figure 63 and described in Table 32.

Figure 63. DEV_CLCRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-0b							
7	6	5	4	3	2	1	0
ECCRC							
R/W-11001110b							

Table 32. DEV_CLCRC Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	0b	
7-0	ECCRC	R/W	11001110b	User EEPROM Space CRC value

7.6.2.22 DEV_CRC Register (Offset = 15h) [Factory Settings = 0000h]

DEV_CRC is shown in Figure 64 and described in Table 33.

Figure 64. DEV_CRC Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
RCRC							
R/W-00h							

Table 33. DEV_CRC Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	00h	
7-0	RCRC	R/W	00h	Device Registers data expected CRC value.

7.6.2.23 CRCCALC Register (Offset = 16h) [Factory Settings = 00FFh]

CRCCALC is shown in Figure 65 and described in Table 34.

Figure 65. CRCCALC Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
CRCRC							
R/W-FFh							

Table 34. CRCCALC Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	00h	
7-0	CRCRC	R/W	FFh	Device Registers data Calculated CRC to be compared against expected CRC value in DEV_CRC

7.6.2.24 DEV_EE_CTRL1 Register (Offset = 17h) [Factory Settings = 0000h]

DEV_EE_CTRL1 is shown in Figure 66 and described in Table 35.

Figure 66. DEV_EE_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
EECMD							
R/W-00h							

Table 35. DEV_EE_CTRL1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	00h	
7-0	EECMD	R/W	00h	User EEPROM Space Command Sequence: 0xA7: Bulk EEPROM Program 0xA2: Bulk EEPROM Load The register is cleared upon command execution completion. Note, the SPI read-after-write response is expected to be monitored to determine whether this register has been successfully written to, or not.

7.6.2.25 DEV_CRC_CTRL1 Register (Offset = 18h) [Factory Settings = 0000h]

DEV_CRC_CTRL1 is shown in Figure 67 and described in Table 36.

Figure 67. DEV_CRC_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
RESERVED							CRCCTL
R-0b							R/W-0h

Table 36. DEV_CRC_CTRL1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-1	RESERVED	R	0b	
0	CRCCTL	R/W	0b	CRC Check Sequence Control: 0: Single CRC check is selected 1: Contiguous CRC check is selected (CRC check is performed every 2 ms)

7.6.2.26 DEV_EE_CTRL4 Register (Offset = 19h) [Factory Settings = 0000h]

DEV_EE_CTRL4 is shown in Figure 68 and described in Table 37.

Figure 68. DEV_EE_CTRL4 Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
EEUNLK							
R/W-00h							

Table 37. DEV_EE_CTRL4 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	00h	
7-0	EEUNLK	R/W	00h	User EEPROM Unlock Sequence: 1. 0x0F 2. 0x55 3. 0xAA 4. 0xF0 Must be completed within 10 ms.

7.6.2.27 DEV_UNLK_CTRL1 Register (Offset = 1Ah) [Factory Settings = 0000h]

DEV_UNLK_CTRL1 is shown in Figure 69 and described in Table 38.

Figure 69. DEV_UNLK_CTRL1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-00h							
7	6	5	4	3	2	1	0
DEVUNLK							
R/W-00h							

Table 38. DEV_UNLK_CTRL1 Register Field Descriptions

Bit	Field	Type	Factory Settings	Description
15-8	RESERVED	R	00h	
7-0	DEVUNLK	R/W	00h	Device Control Registers Unlock Sequence. The following sequence unlocks DEV_CONTROL1 and DEV_CONTROL2 registers: 1. 0x0F 2. 0x55 3. 0xAA 4. 0xF0 Must be completed within 10 ms.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

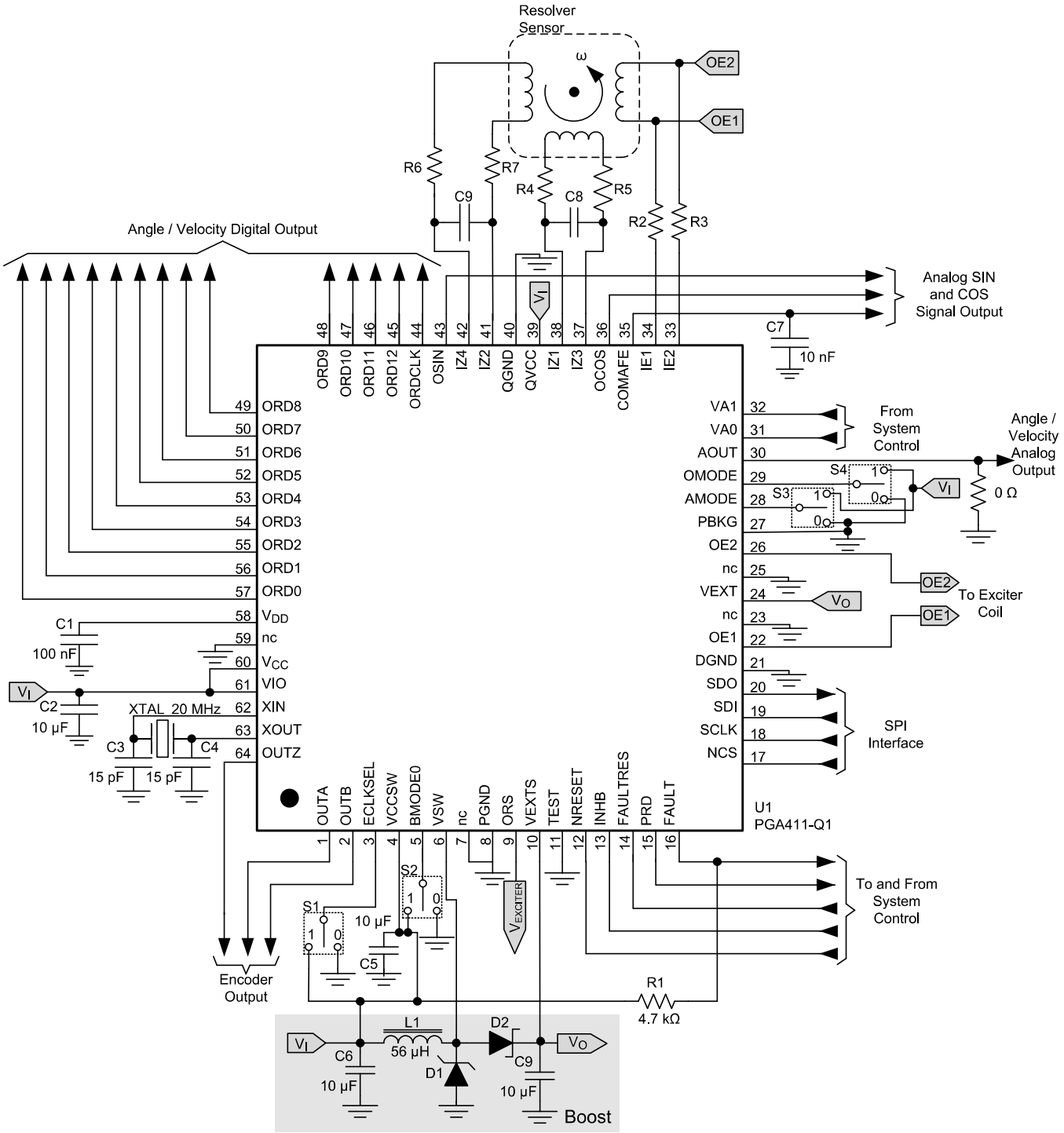
A resolver sensor is the preferred choice for angular position measurements in harsh environments. The resolver sensor resembles a rotary transformer where the output coils are oriented 90° to each other and each produces a voltage complementary to the other. The excitation coil, or the primary coil, is supplied a sine wave. Systems such as traction motors in Electric Vehicles (EV) or Hybrid-Electric Vehicles (HEV), Electric Power Steering (EPS), and Start-Stop Generators typically use resolver sensors.

8.2 Typical Application

The typical application is when the PGA411-Q1 device delivers an excitation output signal using the OE1 and OE2 pins and receives sine and cosine feedback from the IZ1 through IZ4 pins. There are several external components, such as a crystal oscillator, inductor, diodes, and capacitors that are also required in this application. Figure 70 shows an example schematic with the components included.

Typical Application (continued)

8.2.1 Resolver to Digital Converter



NOTE: The maximum current allowed on digital pins such as NRESET and FAULT is 10 mA. Use pullup resistors as needed (the recommended value is 4.7 kΩ).

Figure 70. PGA411-Q1 Typical Application Diagram

Typical Application (continued)

Table 39. PGA411-Q1 Switch Configuration

SW NUMBER	PIN	STATE	DESCRIPTION
S1	ECLKSEL	0	Internal oscillator is used as a system clock
		1	External XTAL oscillator is used as a system clock
S2	BMODE0	0	10-bit angle and velocity resolution
		1	12-bit angle and velocity resolution
S3	AMODE	0	Accelerated mode off
		1	Accelerated mode on
S4	OMODE	0	ORD[11:0] angle and velocity digital output off
		1	ORD[11:0] angle and velocity digital output on

NOTE

The pins that are connected to a switch in the typical application diagram can be connected to a microcontroller to adjust during operation.

Table 40. PGA411-Q1 System Control Pin Configuration

PIN	STATE	DESCRIPTION
VA0 : VA1	00 or 11	ORD[11:0] set to Hi-Z
	01	Velocity output at ORD[11:0]
	10	Angle output at ORD[11:0]
INHB	0	ORD[11:0] data is in hold
	1	ORD[11:0] data is continuously updating
FAULT	0	No faults have been detected
	Hi-Z	Faults are present and the device is in the FAULT state
FAULTRES	0	Faults are cleared and not latched
	1	A fault is latched and signaled by FAULT pin
NRESET	0	The PGA411-Q1 device is in reset
	1	The PGA411-Q1 device is on

8.2.1.1 Design Requirements

The key specifications of any resolver sensor are the excitation voltage, frequency, impedance, and transformation ratio. These factors must be considered while designing with the PGA411-Q1 device. These parameters are typically specified in the data sheet for each resolver sensor; for this example the sensor has an excitation frequency of 10 kHz and the other important parameters are listed in Table 41. Because the PGA411-Q1 device is a highly integrated device, very few components are required outside the chip for the system implementation. Use the values listed in Table 41 as the design parameters.

Table 41. Design Parameters

SPECIFICATION NAME	SPECIFICATION VALUES
Excitation frequency	10 kHz
Excitation voltage	4 V_{RMS}
Resolver sensor input impedance	100 Ω + j × w × 2.54 mH
Transformation ratio	0.35 V/V to 0.5 V/V

8.2.1.2 Detailed Design Procedure

In this design example, the calculation of the system parameters should occur with the sensor specifications of the resolver sensor listed in Table 41.

8.2.1.2.1 Excitation Amplifier Design

Resolver winding impedance has both a resistive and an inductive component. The resistive component of the resolver impedance can vary from as low as 50 Ω to as high as 200 Ω where the reactive inductive component varies with the frequency of operation.

The PGA411-Q1 exciter signal output can be programmed from 10 kHz to 20 kHz. The excitation voltage can be programmed to be either 4 V_{RMS} or 7 V_{RMS}. The differential output voltage in 4 V_{RMS} mode at a gain of 1.5 will be in the range of 10.74 V_{PP} to 11.87 V_{PP}. The maximum output current supported by the PGA411-Q1 device is 145 mA measured at a differential output voltage of 20 V_{PP} between the OE1 and OE2 pins. In this specific example, at 10 kHz, the impedance of the resolver is an addition of 100 Ω and the inductive component is approximately 160 Ω. In 4-V_{RMS} mode, the integrated exciter amplifier of the PGA411-Q1 device can easily drive this coil. The preamplifier stage mentioned in Figure 12 helps in further adjustment of the output voltage.

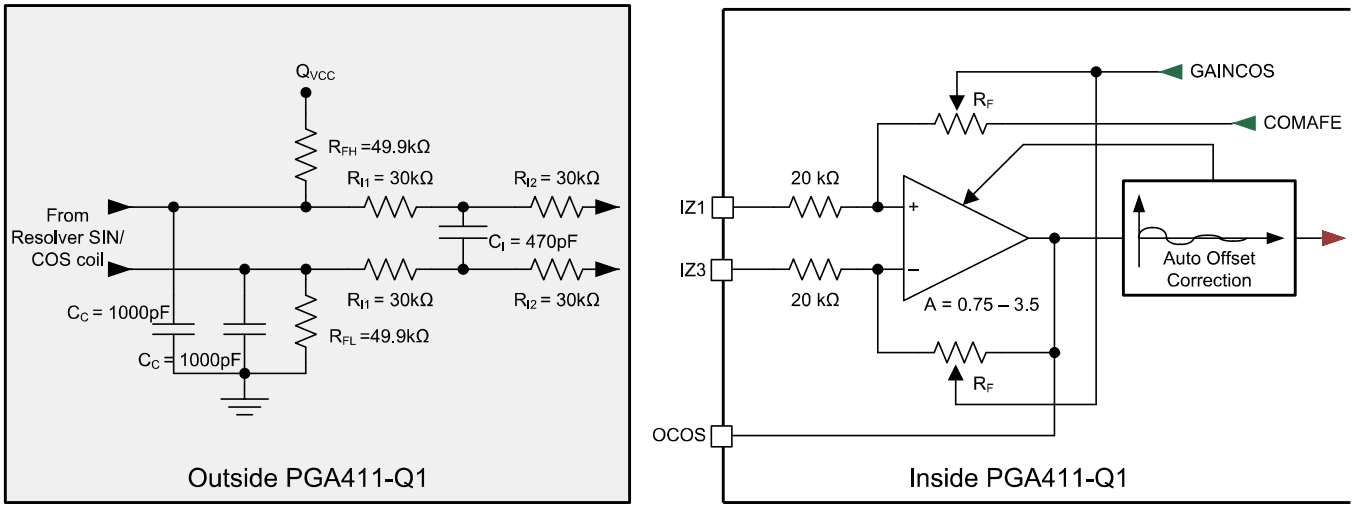
For this design example, the PGA411-Q1 device is set to 4 V_{RMS} mode with a preamplifier gain of 1.9 controlled using EXTOUT_GL, set at 0x0F.

8.2.1.2.2 Boost Power Supply Component Calculations

The maximum output current from the supply is 150 mA. Given the fixed switching frequency of the boost converter (414 kHz), TI recommends using 56 µH of boost inductance along with 10 µF of output capacitance. The input supply to the boost (VCCSW) should range from 4.75 V to 8.5 V. Typically, VCCSW can be supplied with the same 5 V rail as VCC and QVCC, however in applications where high voltages and high currents are needed out of the boost, it is recommended to increase the voltage on VCCSW to achieve desired performance. Resolver sensors The exciter power supply can be programmed through SPI to generate a specific voltage between 13.5 V to 17.5 V in the 7-V_{RMS} mode and 9.5 V to 13.5 V in the 4-V_{RMS} mode. Sufficient headroom must be available from the boost power-supply voltage to have low distortion on the output signal. For this design example, the boost output is programmed as 12 V which is shown in the test results that follow.

8.2.1.2.3 AFE External-Component Value Selection

Because the PGA411-Q1 tracking loop is fed by the SIN and COS signals (through the AFE) from the resolver sensor, conditioning these signals properly is important. Therefore, the selection of external components is critical in the operation of the device. The SIN and COS signals must be amplified properly without causing distortion. Noise must also be suppressed in the monitored frequency range.



R_{IX} Gain setting resistors

C_I Input capacitor

R_{FH} and R_{FL} Open fault resistors

C_C Common-mode capacitors

Figure 71. Selection of External Components for Filtering the IZx pins

As previously described, the AFE gain can be selected between 0.75 and 3.5 which internally changes the R_F resistance as described in Table 42

Table 42. AFE Internal Resistance at Different Gain Levels

GAIN LEVEL	INTERNAL R_F RESISTANCE
0.75	15 kΩ
1	20 kΩ
2.25	45 kΩ
3.5	70 kΩ

Different types of resolver sensors tend to have slightly different transfer coefficients which are usually in the range of 0.35 to 0.5. For this design example, a gain of 1 is selected which corresponds to a resistance of 20 kΩ. If needed, additional resistance can be added to the input signal path to further attenuate the input signal. Be careful because too much gain may cause the OSIN and OCOS outputs to saturate. Use Equation 18 to calculate the overall AFE amplification depending on the resolver SIN and COS signal that must be adjusted so that the OSIN and OCOS output swing is always less than 4 V_{PP}.

$$A\ (V/V) = \frac{R_F}{R_{I(1)} + R_{I(2)} + 20\ k\Omega}$$

where

- OCOS = A × (IZ1 – IZ3) [V_{PP}]
- OSIN = A × (IZ2 – IZ4) [V_{PP}] (18)

To improve noise performance at the input, the input capacitor, C_I, along with the input resistor $R_{I(1)}$ forms a low pass filter with a –3-dB cutoff as shown in Equation 19.

$$f_C\ (-3\ dB) = \frac{1}{2 \times \pi \times 2 \times C_I \times \left(R_{I(1)} \parallel \left[R_{I(2)} + 20\ k\Omega\right]\right)} \quad (19)$$

Use Equation 20 to calculate the time constant, τ.

$$\tau = C_I \times (R_{I(1)} \,||\, [R_{I(2)} + 20\ K\Omega]) \ [s] \quad (20)$$

The time constant is one of the contributors to phase shift between the exciter signal and the SIN and COS signals. Therefore an optimum value must be derived to keep the phase shift in the PGA411-Q1 correction range.

The differential peak-to-peak signal (SIN, COS) of the PGA411-Q1 input must be from 0.188 V to 3 V as well. The resistance values for $R_{I(1)}$ and $R_{I(2)}$ are selected as 30 kΩ based on the previous equations with the internal resistance set at 20 kΩ.

For the open-input diagnostic feature to be operational, the external resistors, R_{FH} and R_{FL}, are implemented which provide DC bias to the IZx inputs in the case when the input coil is disconnected. Table 43 lists the estimated value of these resistors for some assumed voltages at the VEXT pin.

Table 43. Estimated Value for External Resistors at Typical VEXT voltages

VEXT (V)	R_{FH} (KΩ)	R_{FL} (KΩ)
5	20	20
12	50	
24	100	

The input capacitors (C_C) are common-mode capacitors with a value of 1000 pF.

The IE1 and IE2 signals are conditioned in a similar way. Referring to the input specification for these pins, the recommended voltage-input swing should always be less than 4 V_{PP} when measured between pin to ground. Depending on the exciter-amplifier output setting, additional signal attenuation may be required, which can be achieved by adding external resistors as shown in Figure 72.

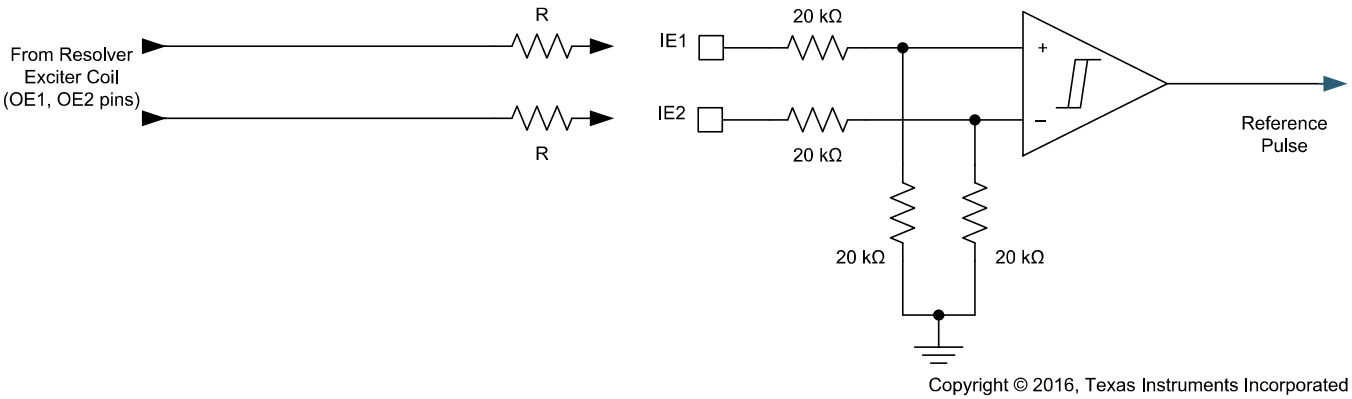


Figure 72. Selection of External Components for the IE1/IE2 Pins

Use Equation 21 to calculate the resistor value, R, depending on the output voltage at OE1 and OE2 pins. The (single-ended) voltage the device sees on the IEx pins (V_{IEX}) needs to be between 0.5 V to 4 V for optimal performance.

$$R = 40\ k\Omega \times \frac{V_{OEx} - V_{IEx}}{V_{IEx}} \ (\Omega) \quad (21)$$

8.2.1.2.3.1 Exciter Signal-Path Output Calculation

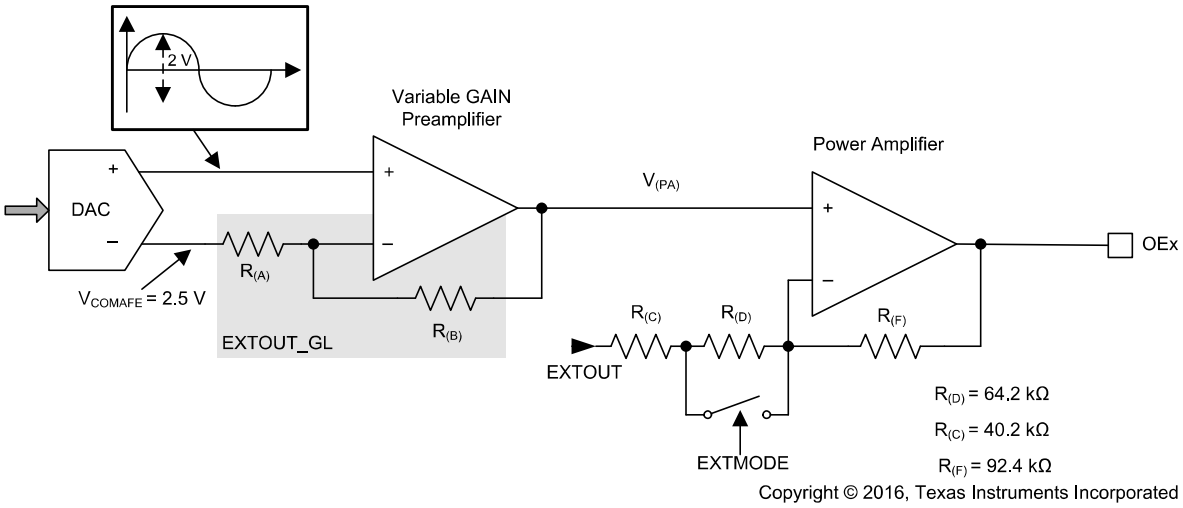


Figure 73. Exciter Output Gain

Use Equation 22 to calculate the value of the variable-gain preamplifier (which is already calculated and selected through the EXTOUT_GL parameter).

$$\frac{V_{(PA)}}{V_{(DAC)}} = EXTOUT\_GL = \frac{R_{(A)} + R_{(B)}}{R_{(A)}} - \frac{V_{COMAFE}}{V_{(DAC)}} \times \frac{R_{(B)}}{R_{(A)}} \quad (22)$$

where

- $V_{(PA)}$ is an internal signal that is the voltage output of the variable GAIN preamplifier

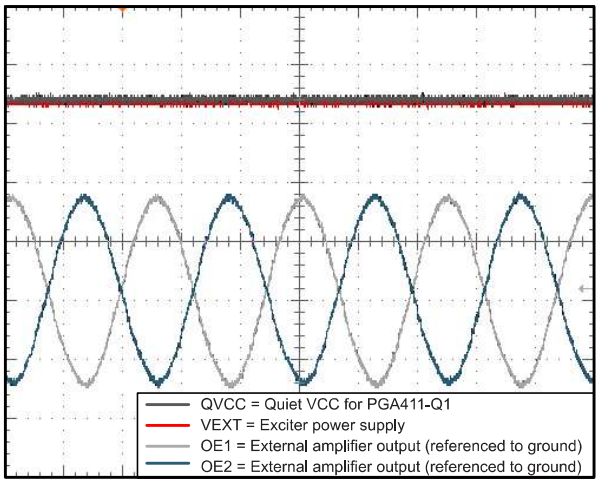
For the power amplifier, use Equation 23 and Equation 24. For the 4-V_{RMS} output, EXTMODE is selected in a way that the switch is open as shown in Equation 23.

$$\frac{V_{OEx}}{V_{(PA)}} = \frac{R_{(C)} + R_{(D)} + R_{(F)}}{R_{(C)} + R_{(D)}} - \frac{V_{EXTOUT}}{V_{(PA)}} \times \frac{R_{(F)}}{R_{(C)} + R_{(D)}} \quad (23)$$

For the 7-V_{RMS} output, EXTMODE is selected in a way that the switch is closed as shown in Equation 24.

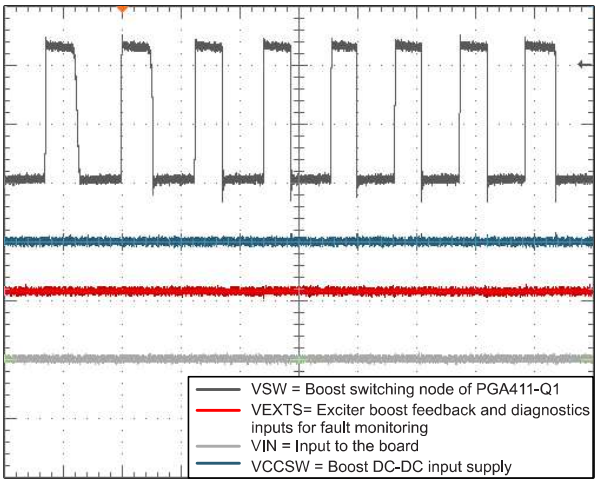
$$\frac{V_{OEx}}{V_{(PA)}} = \frac{R_{(C)} + R_{(F)}}{R_{(C)}} - \frac{V_{EXTOUT}}{V_{(PA)}} \times \frac{R_{(F)}}{R_{(C)}} \quad (24)$$

8.2.1.3 Application Curves



QVCC = VEXT = 5 V

Figure 74. Exciter Amplifier



Operation from 5 V to 12 V

Figure 75. Boost Power Supply

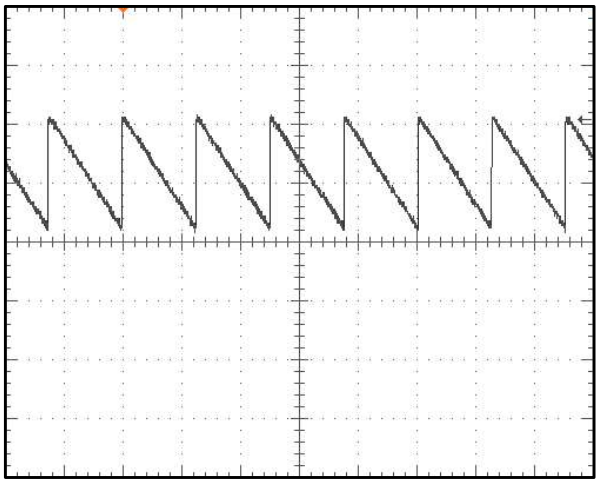


Figure 76. AOUT Signal (With No Resolver Connected)

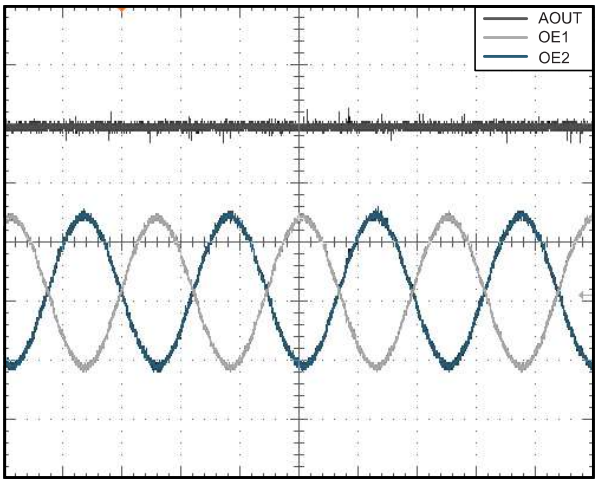


Figure 77. AOUT (Test Signal, With Resolver Connected)

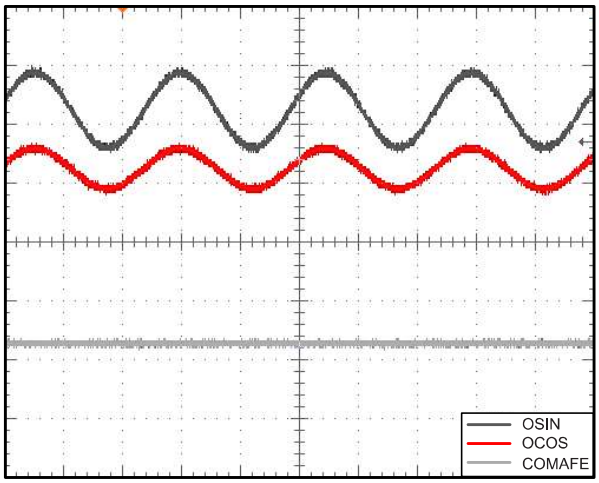


Figure 78. Analog Front-End (AFE) Outputs

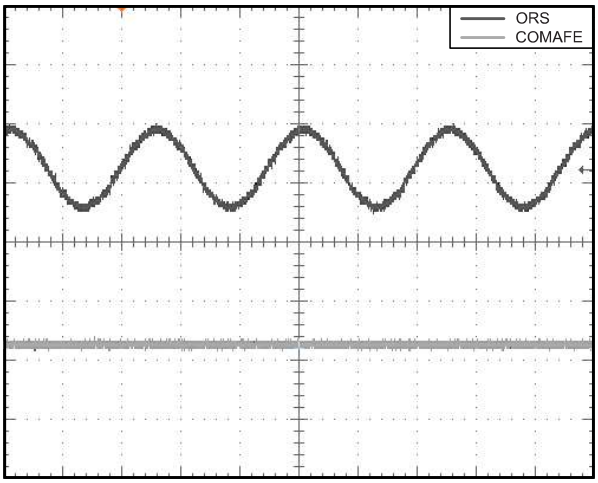
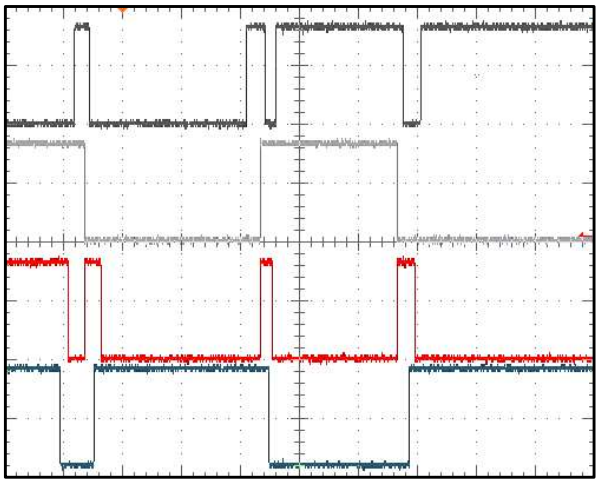
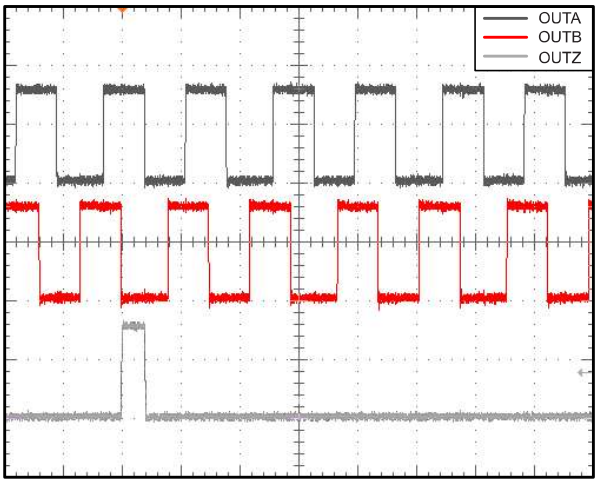


Figure 79. External Amplifier (ORS, COMAFE)



Typical output of ORD pins during rotation

Figure 80. ORD Digital Outputs (ORD1 Through ORD4)



OUT A,B,Z during a constant velocity rotation

Figure 81. Encoder Emulated Outputs (OUTA, OUTB, and OUTZ)

8.3 System Examples

Use the following legends for Figure 82, Figure 83, and Figure 84.

GP_I General-purpose input

GP_O General-purpose output

TIMER_I Input port connected to a timer, counter, capture, or compare module

TIMER_O Output port connected to a timer, counter, capture, or compare module

Data bus

Control interface

System Examples (continued)

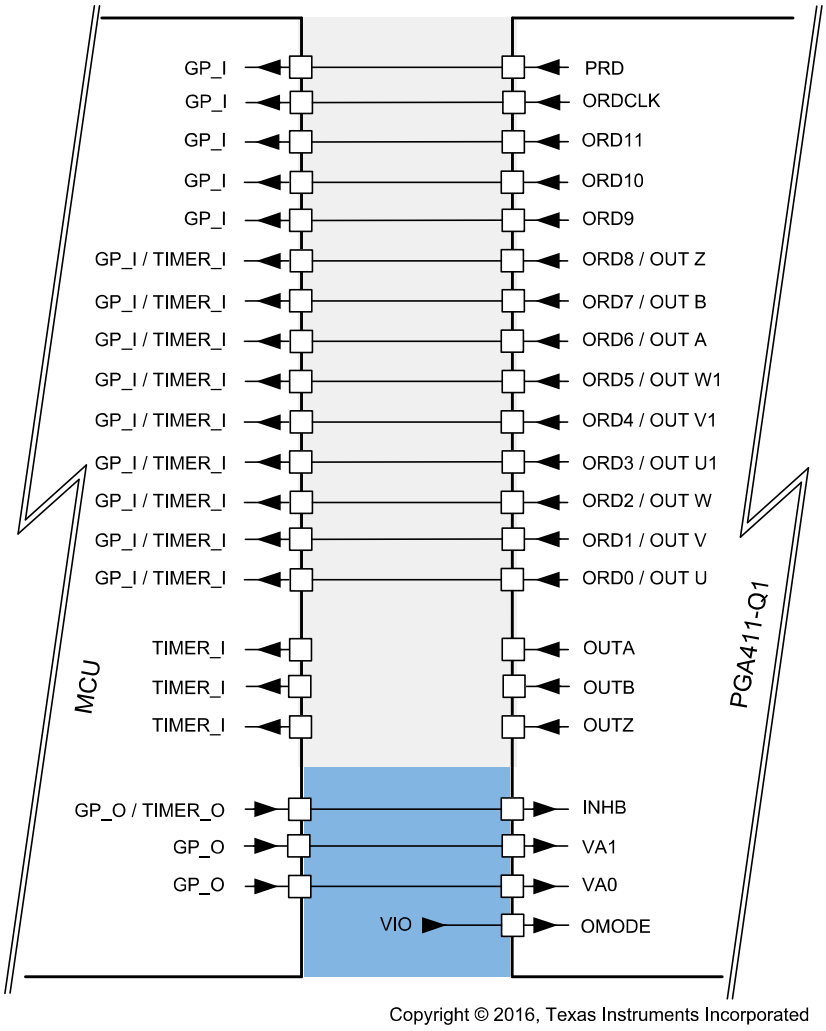
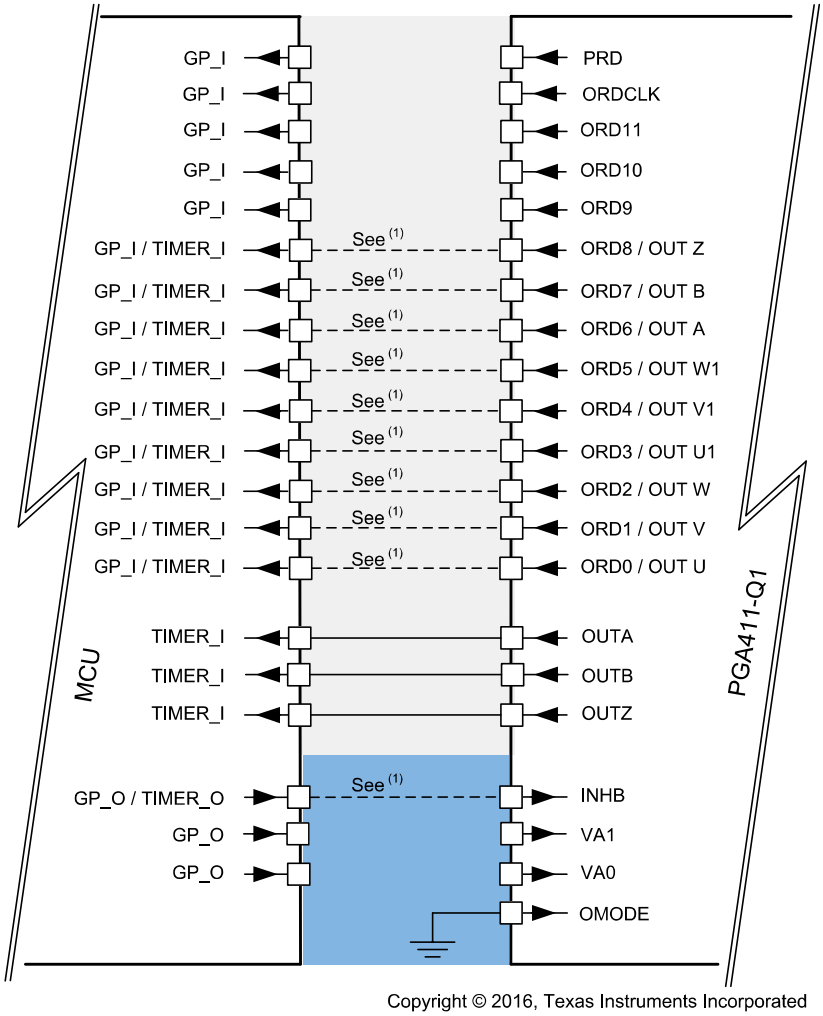


Figure 82. Single PGA411-Q1 Parallel Data Output

System Examples (continued)



(1) Optional

Figure 83. Single PGA411-Q1 Emulated Encoder Data Output

System Examples (continued)

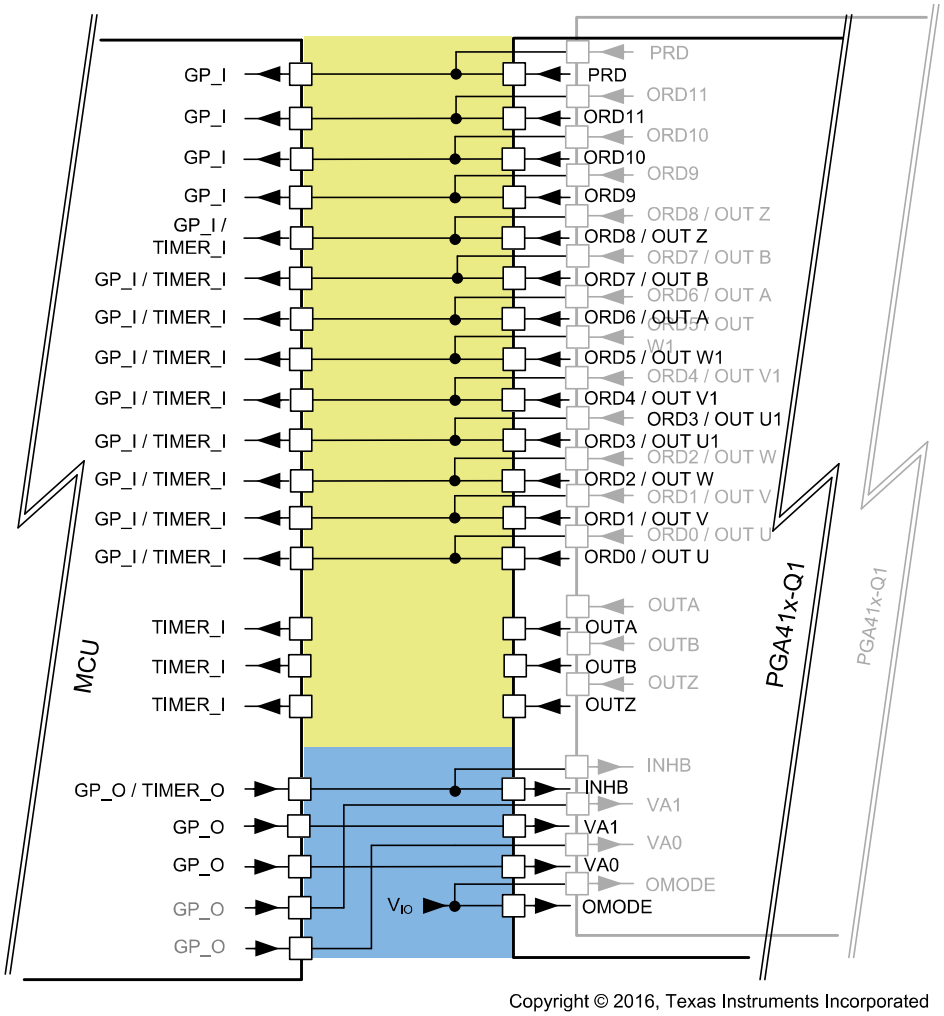


Figure 84. Multiple PGA411-Q1 Parallel Data Output

8.4 Initialization Set Up

Refer to Figure 1 to ensure the commands follow the required SPI sequence and that the NCS pin is turned on before sending the SPI commands. Figure 2 shows the timing of signals. The NRESET pin should remain on during normal operation of the circuit.

9 Power Supply Recommendations

The PGA411-Q1 device has three ground pins which are for the power ground (PGND), digital ground (DGND), and quiet ground (QGND).

NOTE

The PGND and DGND pins are connected inside the PGA411-Q1 device.

TI recommends using a STAR ground technique to connect the grounds and to add decoupling capacitors between the quiet ground, the power, and digital ground.

The V_{DD} regulator receives a 5-V input supply voltage form the V_{CC} pin and generates a stable 1.8-V supply for internal digital-logic circuits. The V_{DD} pin requires an external filtering capacitor. For this filtering, connect a 100-nF capacitor to the V_{DD} pin.

The digital supply voltage for the I/O pins, V_{CC}, VEXT, and QVCC requires good quality ceramic decoupling capacitors. Additional filtering using a ferrite bead and decoupling capacitors is recommended at the QVCC pin.

NOTE

The input supply to the PGA411 V_{CC} and QVCC pins must ramp to 5 V within 4 ms and the supply voltage cannot start below 0 V.

The VCCSW pin is the input to the boost circuit. Typically, the VCCSW pin can be supplied with 5 V which means it can be tied with the other input supply rails of the PGA411-Q1 device. In high current applications or applications that require the boost output to be greater than 14 V, a higher supply voltage may be required.

10 Layout

10.1 Layout Guidelines

A typical printed circuit board (PCB) using the PGA411-Q1 device has four layers. The top and bottom layers are mainly assigned for the signal paths. The first mid layer is assigned as the ground plane and mid layer two is assigned to be the voltage supply planes.

For the boost circuit (see Figure 85), the placement of components L1 and D6 should form the smallest possible switching current loop. The input capacitor, C32, should be placed on the bottom layer and should be located very close to the device. The diode, D5, is not populated and was used only for test and debug. The output capacitors are indicated by C18 and C23.

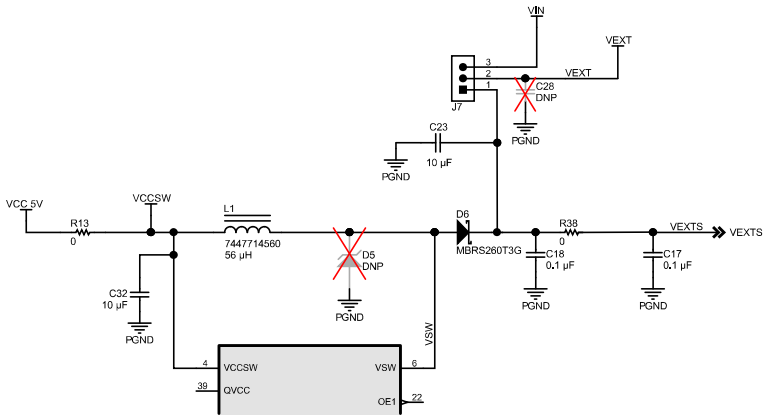


Figure 85. Boost Circuit Schematic

The filtering circuit for the AFE must be referenced to the QVCC and QGND pins.

10.2 Layout Example

Below are several images showing example layout for the PGA411-Q1 and surrounding components. Refer to the application note, *PGA411-Q1 PCB Design Guidelines* (SLAA697), for details on layout recommendations.

Layout Example (continued)

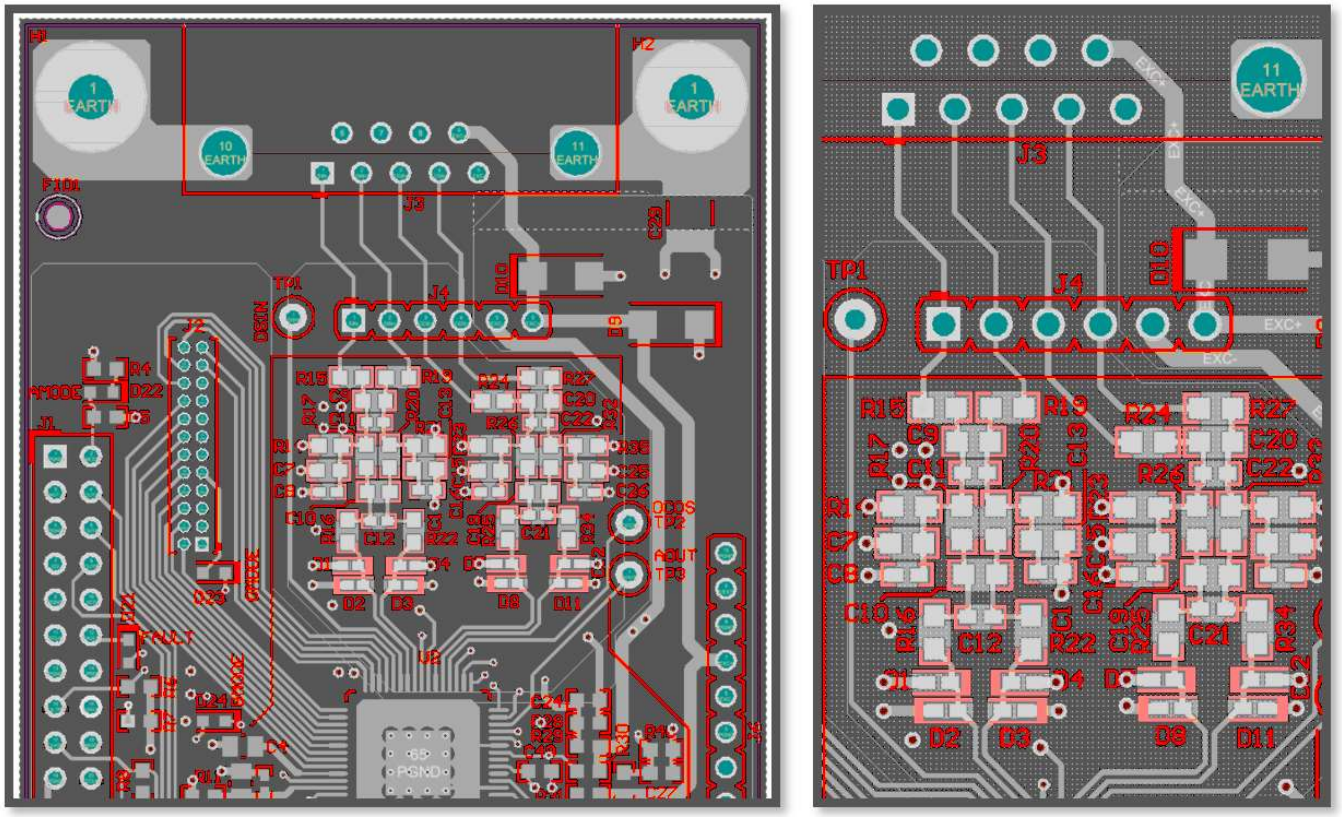


Figure 86. Analog Front-End Layout

Layout Example (continued)

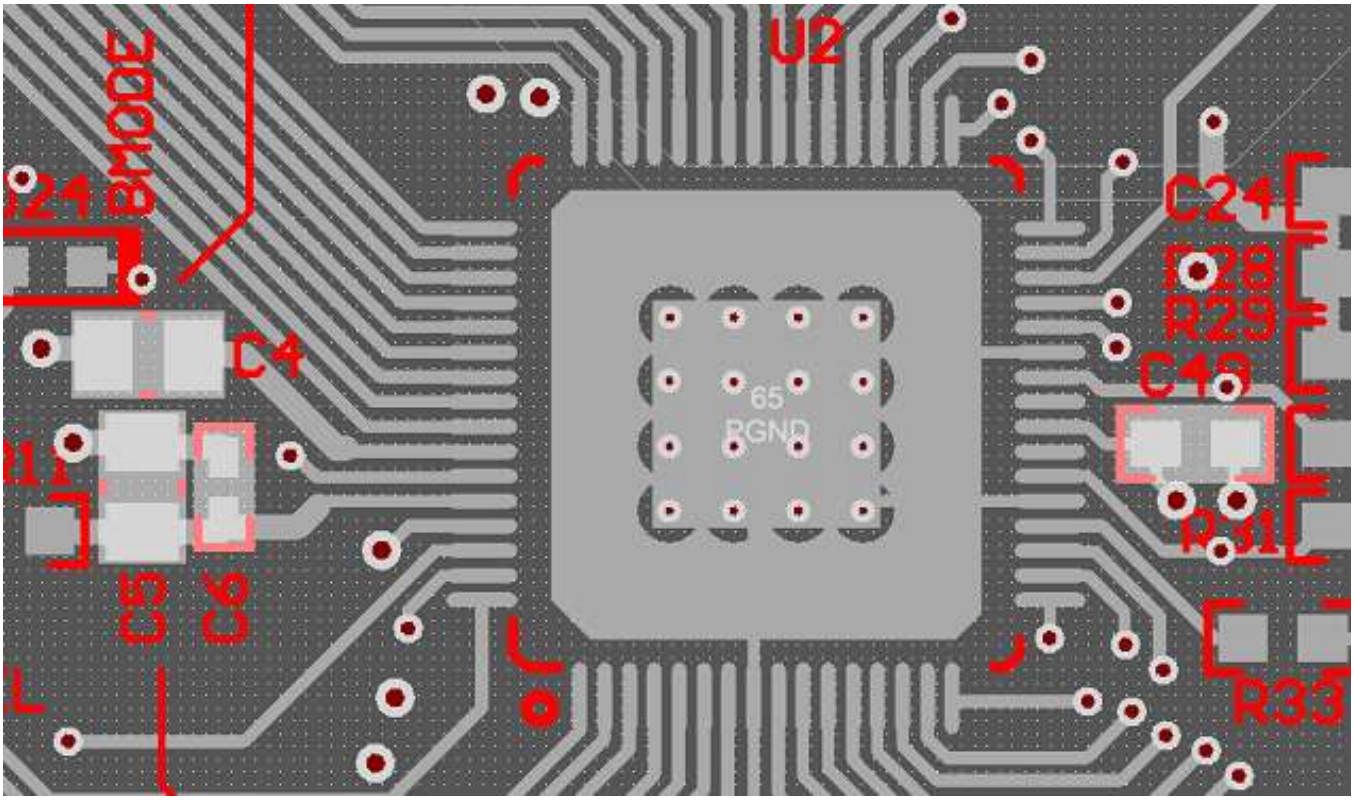


Figure 87. Decoupling Capacitors

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *ALM2402-Q1 Dual Op-amp with High Current Output*, SLOS912
- *Troubleshooting Guide for PGA411-Q1*, SLAA687
- *PGA411-Q1 PCB Design Guidelines*, SLAA697
- *PGA411-Q1 EVM User's Guide*, SLAU658
- *Safety Manual for PGA411-Q1 Resolver Sensor Interface*, SLAA684

11.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA411QPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	PGA411QPAPRQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

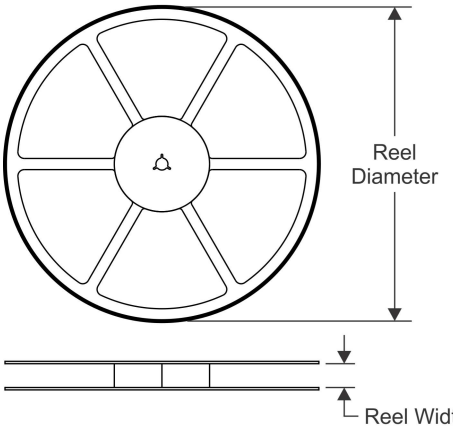
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

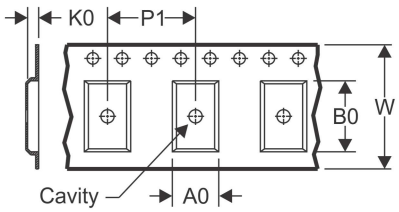
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

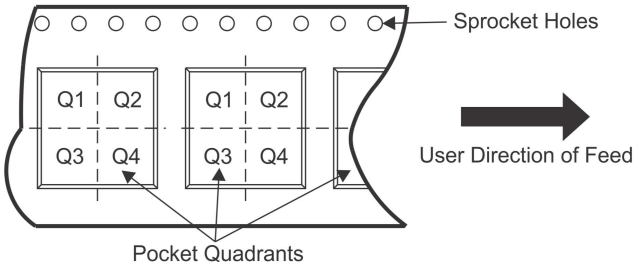


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

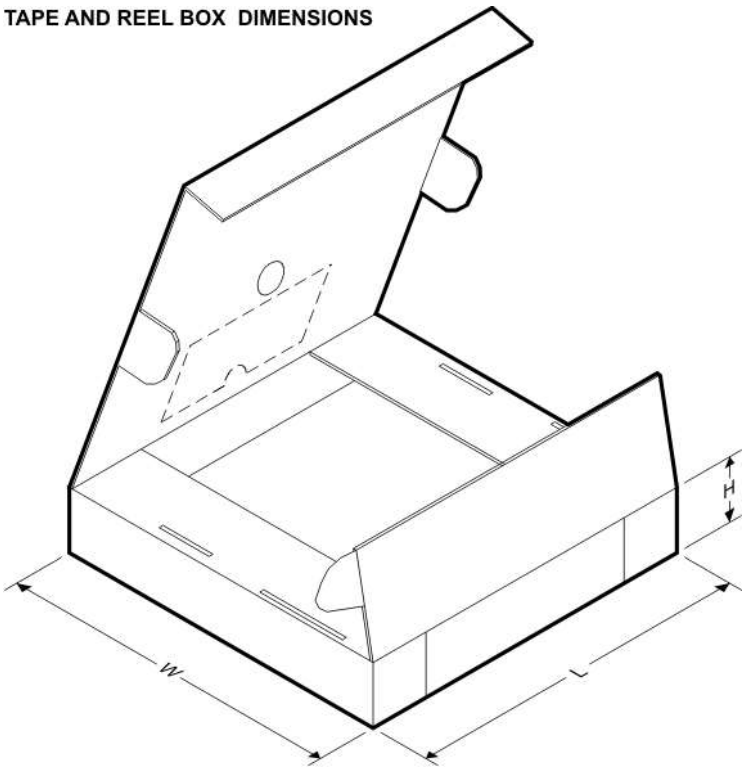
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA411QPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

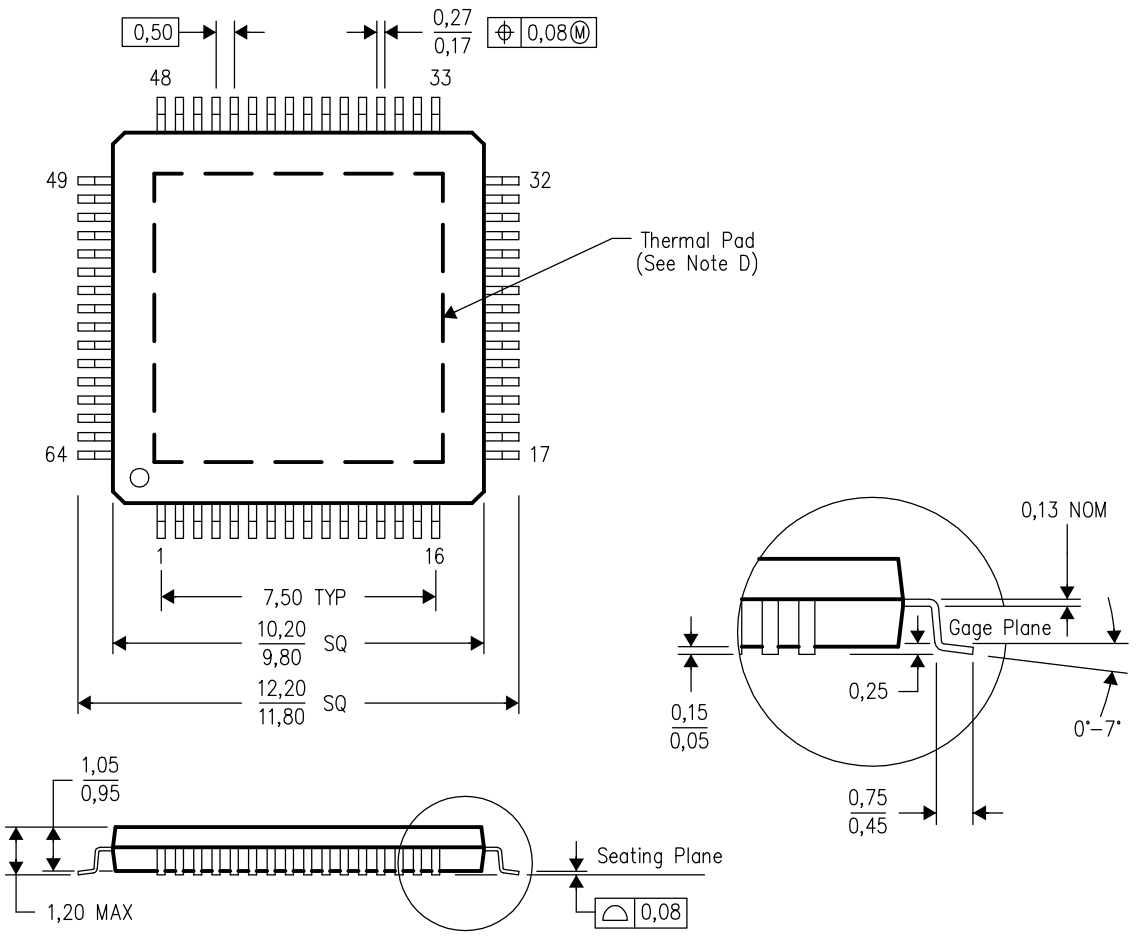
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA411QPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	45.0

PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

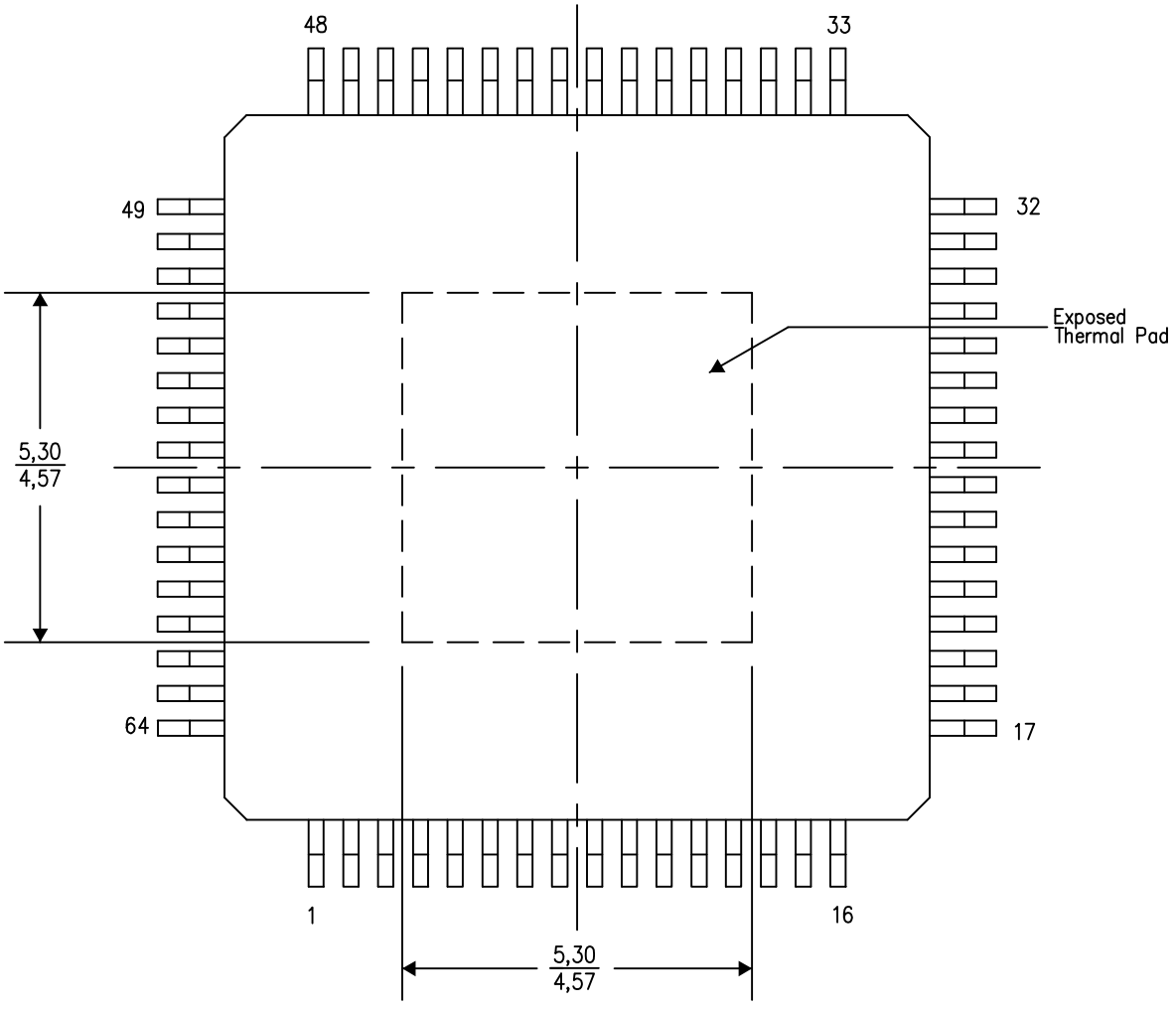
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206326–8/P 05/14

NOTES: A. All linear dimensions are in millimeters

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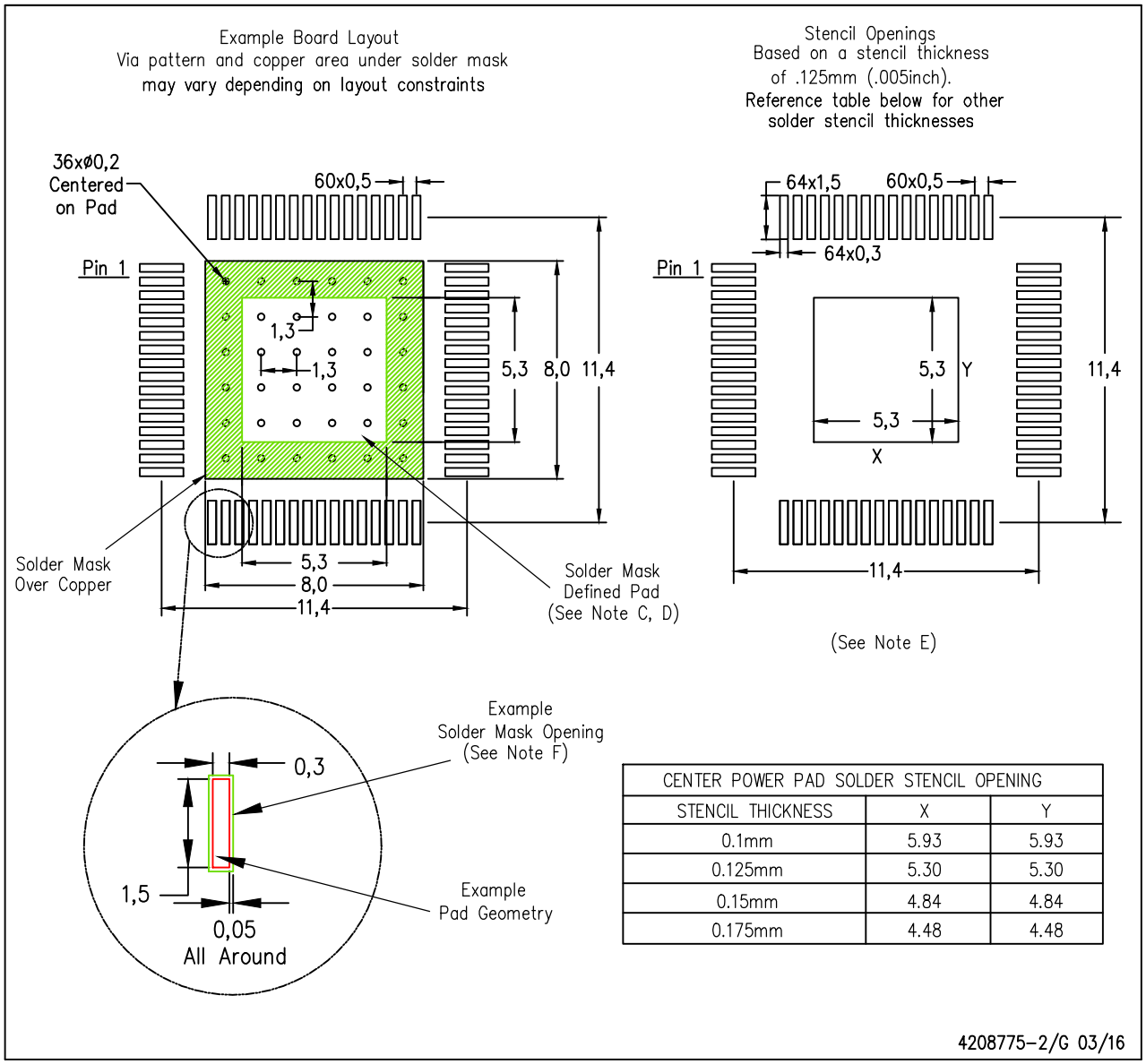
PAP (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	5.93	5.93
0.125mm	5.30	5.30
0.15mm	4.84	4.84
0.175mm	4.48	4.48

4208775–2/G 03/16

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
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