RoHS Compliant

16GB DDR4 SDRAM XR-DIMM

Halogen free / Industrial / Underfill / Coating

Product Specifications

September 17, 2020

Version 0.5

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General Description

Apacer **DD2.22260S.001** is a 2048M x 64 DDR4 SDRAM (Synchronous DRAM) XR-DIMM. This high-density memory module consists of 16 pieces 1024M x 8 bits DDR4 synchronous DRAMs in FBGA packages and a 4K Bits EEPROM. The module is a 300-pins dual in-line memory module and is intended for mounting into a connector socket. The following provides general specifications of this module.

Ordering Information

Part Number	Bandwidth	Speed Grade	Max Frequency	CAS Latency
DD2.22260S.001	19.2 GB/sec	2400 Mbps	1200 MHz	CL17

Density	Organization	Component	Rank
16GB	2048M x 64	1024M x8*16	2

Key Parameters

MT/s	DDR4-1866	DDR4-2133	DDR4-2400	Unit
Grade	-CL13	-CL15	-CL17	
tCK (min)	1.07	0.93	0.83	ns
CAS latency	13	15	17	tCK
tRCD (min)	13.92	14.06	14.16	ns
tRP (min)	13.92	14.06	14.16	ns
tRAS (min)	34	33	32	ns
tRC (min)	47.92	47.05	46.16	ns
CL-tRCD-tRP	13-13-13	15-15-15	17-17-17	tCK

Specifications:

- On-DIMM thermal sensor : Yes
- Organization: 2048 words x 64 bits, 2 ranks
- Integrating 16 pieces of 8G bits DDR4 SDRAM sealed FBGA
- Package: eXtreme Rugged 300-pin connector type dull in-line memory module (XR-DIMM)
- PCB: height 37.25 mm, lead pitch 0.50 mm (pin),
- Serial Presence Detect (SPD)
- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP = 2.5V (2.375V to 2.75V)
- VDDSPD = 2.2V to 3.6V
- 16 internal banks (4 Bank Groups)
- CAS Latency (CL): 13, 14, 15, 16, 17
- CAS Write Latency (CWL): 12,16
- Support Industrial Temp (-40°C~95°C)

  - tREFI 7.8us at -40 °C ≤ TCASE ≤ 85°C

  - tREFI 3.9us at 85 °C < TCASE ≤ 95°C
- Lead-free (RoHS compliant)
- Halogen free
- With coating (CE-1170)
- BGA Underfill with JC738-8
- Connector : BSH-150-01-L-D-A

Features:

- Functionality and operations comply with the DDR4 SDRAM datasheet
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

Pin Assignments

Pin No.	Pin name-Front	Pin No.	Pin name-Back	Pin No.	Pin name-Front	Pin No.	Pin name-Back
1	NC	2	NC	3	NC	4	NC
5	NC	6	NC	7	NC	8	NC
9	NC	10	NC	11	NC	12	NC
13	NC	14	NC	15	NC	16	NC
17	NC	18	NC	19	NC	20	NC
21	VSS	22	VSS	23	DQ4	24	DQ5
25	VSS	26	VSS	27	DQ0	28	DQ1
29	VSS	30	VSS	31	DM0_N/DMI0_N	32	DQS0_C
33	VSS	34	DQS0_T	35	DQ6	36	VSS
37	VSS	38	DQ7	39	DQ2	40	VSS
41	VSS	42	DQ3	43	DQ12	44	VSS
45	VSS	46	DQ13	47	DQ8	48	VSS
49	VSS	50	DQ9	51	DQS1_C	52	VSS
53	DQS1_T	54	DM1_N/DBI1_N	55	VSS	56	VSS
57	DQ14	58	DQ15	59	VSS	60	VSS
61	DQ11	62	DQ10	63	VSS	64	VSS
65	DQ20	66	DQ21	67	VSS	68	VSS
69	DQ16	70	DQ17	71	VSS	72	VSS
73	DM2_N/DBI2_N	74	DQS2_C	75	VSS	76	DQS2_t
77	DQ22	78	VSS	79	VSS	80	DQ23
81	DQ18	82	VSS	83	VSS	84	DQ19
85	DQ28	86	VSS	87	VSS	88	DQ29
89	DQ24	90	VSS	91	VSS	92	DQ25
93	DQS3_C	94	VSS	95	DQS3_T	96	DM3_N/DBI3_N
97	VSS	98	VSS	99	DQ31	100	DQ30
101	VSS	102	VSS	103	DQ27	104	DQ26
105	VSS	106	VSS	107	CB4	108	CB5
109	VSS	110	VSS	111	CB0	112	CB1
113	VSS	114	VSS	115	DM8_N/DBI8_N	116	DQS8_C
117	VSS	118	DQS8_T	119	CB6	120	VSS

Pin No.	Pin name-Front	Pin No.	Pin name-Back	Pin No.	Pin name-Front	Pin No.	Pin name-Back
121	VSS	122	CB2	123	CB7	124	VSS
125	VSS	126	CB3	127	RESET_N	128	VSS
129	CKE1	130	CKE0	131	VDD	132	VDD
133	ACT_N	134	BG1	135	ALERT_N	136	BG0
137	VDD	138	VDD	139	A11	140	A12
141	A7	142	A9	143	VDD	144	VDD
145	A5	146	A8	147	A4	148	A6
149	VDD	150	VDD	151	A2	152	A3
153	EVENT_N	154	A1	155	VDD	156	VDD
157	CK1_T	158	CK0_T	159	CK1_C	160	CK0_C
161	VDD	162	VDD	163	A0	164	PARITY
165	A10/AP	166	BA1	167	VDD	168	VDD
169	BA0	170	CS0_N	171	RAS_N/A16	172	WE_N/A14
173	VDD	174	VDD	175	CAS_N/A15	176	ODT0
177	A13	178	CS1_N	179	VDD	180	VDD
181	C0/CS2_N	182	ODT1	183	VREFCA	184	VDD
185	SA2	186	C1/CS3_N	187	VSS	188	VSS
189	DQ36	190	DQ37	191	VSS	192	VSS
193	DQ32	194	DQ33	195	VSS	196	VSS
197	DM4_N/DBI4_N	198	DQS4_C	199	VSS	200	DQS4_T
201	DQ39	202	VSS	203	VSS	204	DQ38
205	DQ35	206	VSS	207	VSS	208	DQ34
209	DQ45	210	VSS	211	VSS	212	DQ44
213	DQ41	214	VSS	215	VSS	216	DQ40
217	DQS5_C	218	VSS	219	DQS5_T	220	DM5_N/DBI5_N
221	VSS	222	VSS	223	DQ47	224	DQ46
225	VSS	226	VSS	227	DQ43	228	DQ42
229	VSS	230	VSS	231	DQ53	232	DQ52
233	VSS	234	VSS	235	DQ48	236	DQ49
237	VSS	238	VSS	239	DM6_N/DBI6_N	240	DQS6_C
241	VSS	242	DQS6_T	243	DQ54	244	VSS
245	VSS	246	DQ55	247	DQ50	248	VSS
249	VSS	250	DQ51	251	DQ60	252	VSS

Pin No.	Pin name-Front	Pin No.	Pin name-Back	Pin No.	Pin name-Front	Pin No.	Pin name-Back
253	VSS	254	DQ61	255	DQ57	256	VSS
257	VSS	258	DQ56	259	DQS7_C	260	VSS
261	DQS7_T	262	DM7_N/DBI7_N	263	VSS	264	VSS
265	DQ63	266	DQ62	267	VSS	268	VSS
269	DQ59	270	DQ58	271	VSS	272	VSS
273	SDA	274	SCL	275	SA0	276	VDDSPD
277	VTT	278	VPP	279	SA1	280	VPP
281	NC	282	NC	283	NC	284	NC
285	NC	286	NC	287	NC	288	NC
289	NC	290	NC	291	NC	292	NC
293	NC	294	NC	295	NC	296	NC
297	NC	298	NC	299	NC	300	NC

*IC Component Composition :

256Mx8	A0~A13		
512Mx8	A0~A14,	512Mx4	A0~A14
1024Mx8	A0~A15,	1024Mx4	A0~A15
2048Mx8	A0~A16,	2048Mx4	A0~A16

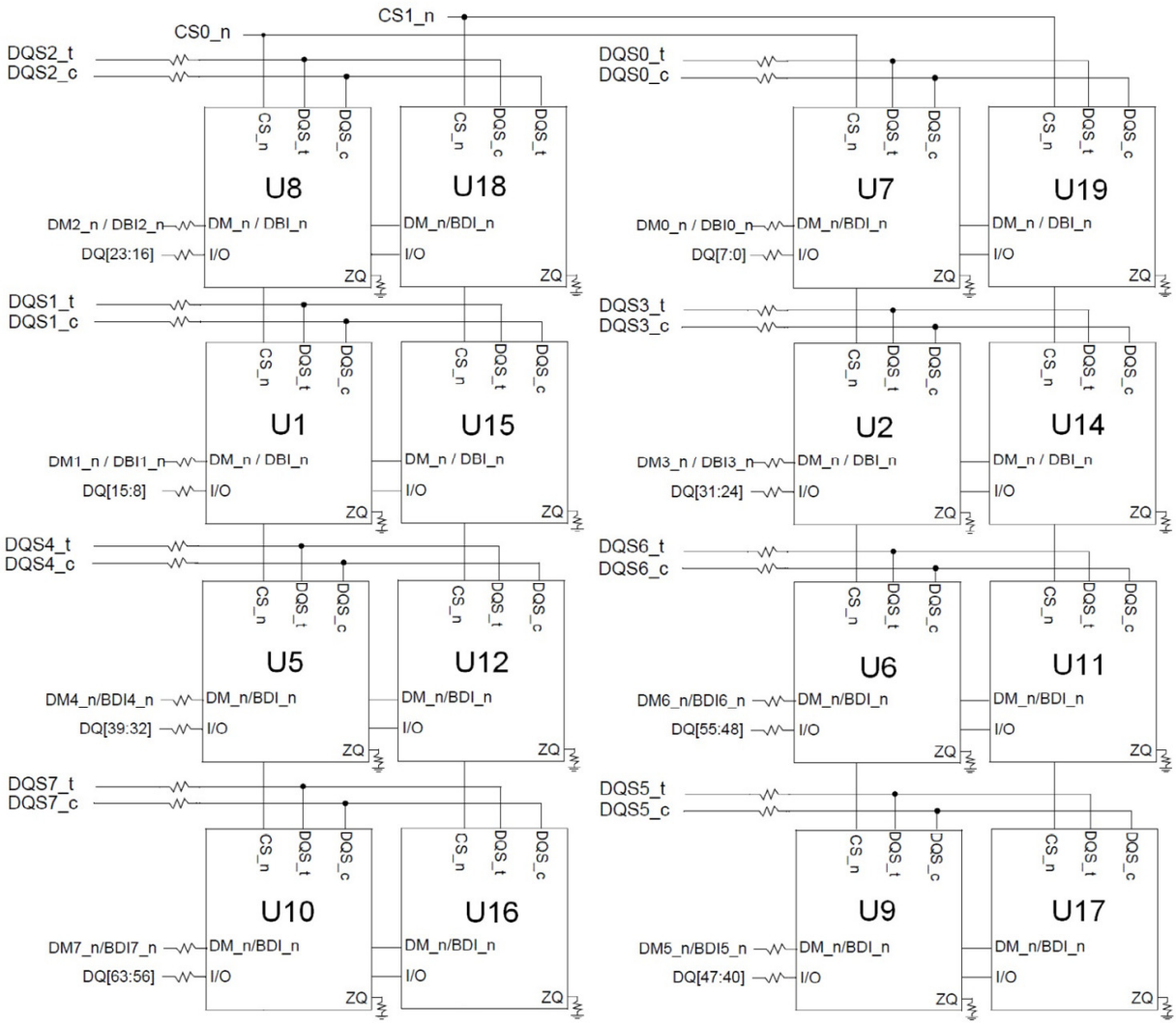
Pin Descriptions

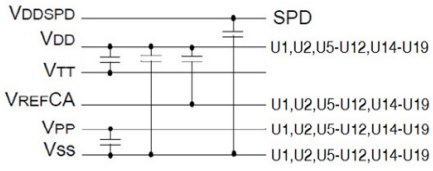
Pin Name	Description
Ax[1*]	SDRAM address bus
BAx	SDRAM bank select
BGx	SDRAM bank group select
RAS_n[2*]	SDRAM row address strobe
CAS_n[3*]	SDRAM column address strobe
WE_n[4*]	SDRAM write enable
CSx_n	DIMM Rank Select Lines
CKEx	SDRAM clock enable lines
ODTx	SDRAM on-die termination control lines
ACT_n	SDRAM input for activate input
DQx	DIMM memory data bus
CBx	DIMM ECC check bits
TDQSx_t ; TDQSx_c	Dummy loads for mixed populations of x4 based and x8 based RDIMMs. Not used on UDIMMs
DQSx_t	Data Buffer data strobes (positive line of differential pair)
DQSx_c	Data Buffer data strobes (negative line of differential pair)
DMx_n, DBIx_n	SDRAM data masks/data bus inversion(x8-based x72 DIMMs)
CKx_t	SDRAM clock input (positive line of differential pair)
CKx_c	SDRAM clocks input (negative line of differential pair)
SCL	I^2C serial bus clock for SPD-TSE and register
SDA	I^2C serial bus data line for SPD-TSE and register
SAx	I^2C slave address select for SPD-TSE and register
PARITY	SDRAM parity input
VDD	SDRAM core power supply
12 V	Optional Power Supply on socket but not used on DIMM
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD-TSE positive power supply
ALERT_n	SDRAM ALERT_n output
VPP	SDRAM Supply
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

*Notes:
1. Address A17 is only valid for 16 Gb x4 based SDRAMs. For UDIMMs this connection pin is NC.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

Functional Block Diagram

Part 1 of 2

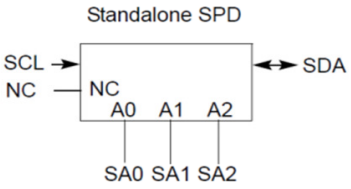


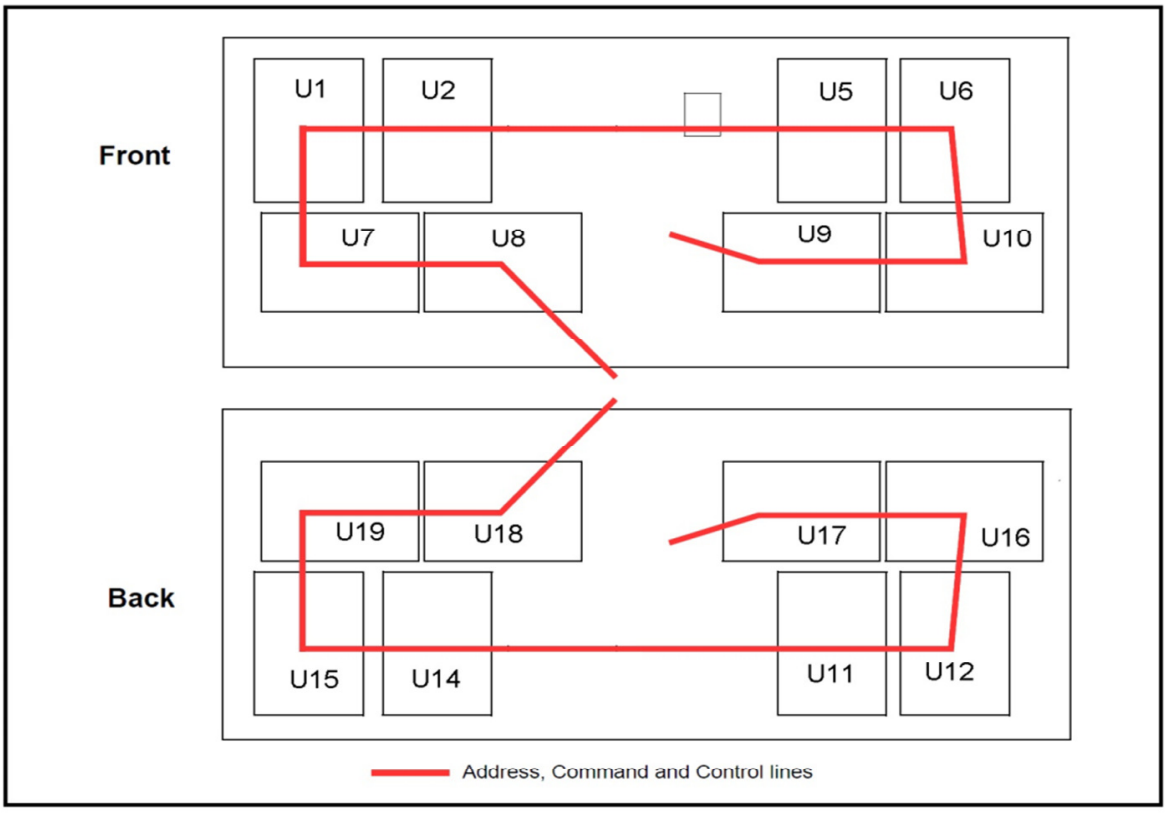


1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. Unless otherwise noted, resistor values are 15 Ω ± 5%.
3. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
4. ZQ resistors are 240 Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.

Part 2 of 2

CKE0	CKE: SDRAMs U1,U2,U5-U10	Parity	Parity: SDRAMs U1,U2,U5-U12,U14-U19
CKE1	CKE: SDRAMs U11,U12,U14-U19	ALERT_n	ALERT_n: SDRAMs U1,U2,U5-U12,U14-U19
ODT0	ODT: SDRAMs U1,U2,U5-U10	CK0_t	CK_t: SDRAMs U1,U2,U5-U10
ODT1	ODT: SDRAMs U11,U12,U14-U19	CK0_c	CK_c: SDRAMs U1,U2,U5-U10
BA[1:0]	BA[1:0]: SDRAMs U1,U2,U5-U12,U14-U19	CK1_t	CK_t: SDRAMs U11,U12,U14-U19
BG[1:0]	BG[1:0]: SDRAMs U1,U2,U5-U12,U14-U19	CK1_c	CK_c: SDRAMs U11,U12,U14-U19
A[16:0]	A[16:0]: SDRAMs U1,U2,U5-U12,U14-U19	C[1:0]	C[1:0]: SDRAMs NC
RESET_n	RESET_n: SDRAMs U1,U2,U5-U12,U14-U19		





Absolute Maximum Ratings

Parameter	Symbol	Description	Units	Notes
Voltage on VDD pin relative to Vss	V_{DD}	- 0.3 V ~ 1.5 V	V	1,2
Voltage on VDDQ pin relative to Vss	V_{DDQ}	- 0.3 V ~ 1.5 V	V	1,2
Voltage on VPP pin relative to Vss	V_{PP}	- 0.3 V ~ 3.0 V	V	3
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 0.3 V ~ 1.5 V	V	1,2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
3. VPP must be equal or greater than VDD/VDDQ at all times

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature Range	-40 to 95	℃	1,2

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40°C~95°C under all operating conditions.

Industrial Temperature:

The industrial temperature device requires that the case temperature not exceed –40°C or +95°C. JEDEC specifications require the refresh rate to double when TC exceeds+85°C; this also requires use of the high-temperature self refresh option.

- MAX operating case temperature. TC is measured in the center of the package.
- A thermal solution must be designed to ensure the DRAM device does not exceed the maximum TC during operation.
- Device functionality is not guaranteed if the DRAM device exceeds the maximum TC during operation.
- If TC exceeds +85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.

Operating Conditions

Recommended DC Operating Conditions – DDR4 (1.2V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Activation Supply Voltage	2.375	2.5	2.75	V	3

Notes:

1. Under all conditions VDDQ must be less than or equal to VDD..
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

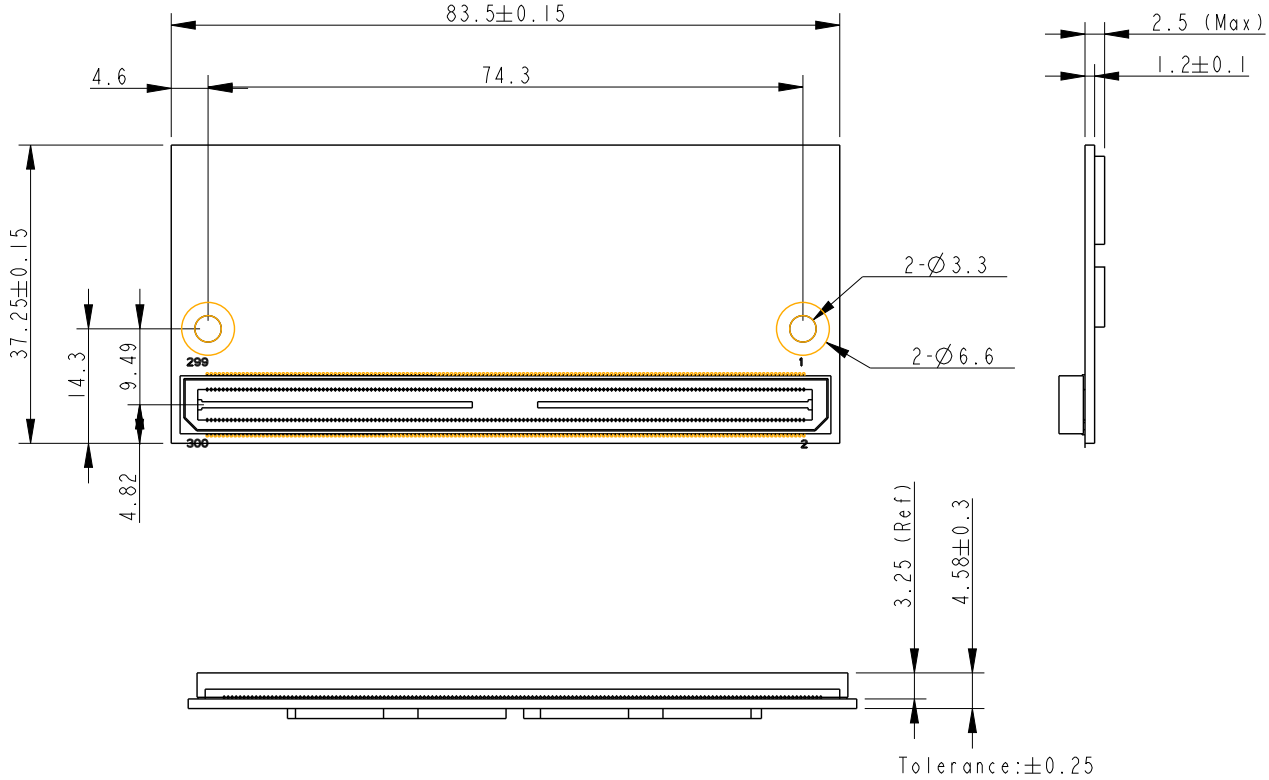
Environmental Requirements

Symbol	Parameter	Rating	Units	Notes
HOPR	Operating Humidity (relative)	10 to 90	%	
TSTG	Storage Temperature	-50 to +100	°C	1
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	kPa	1,2

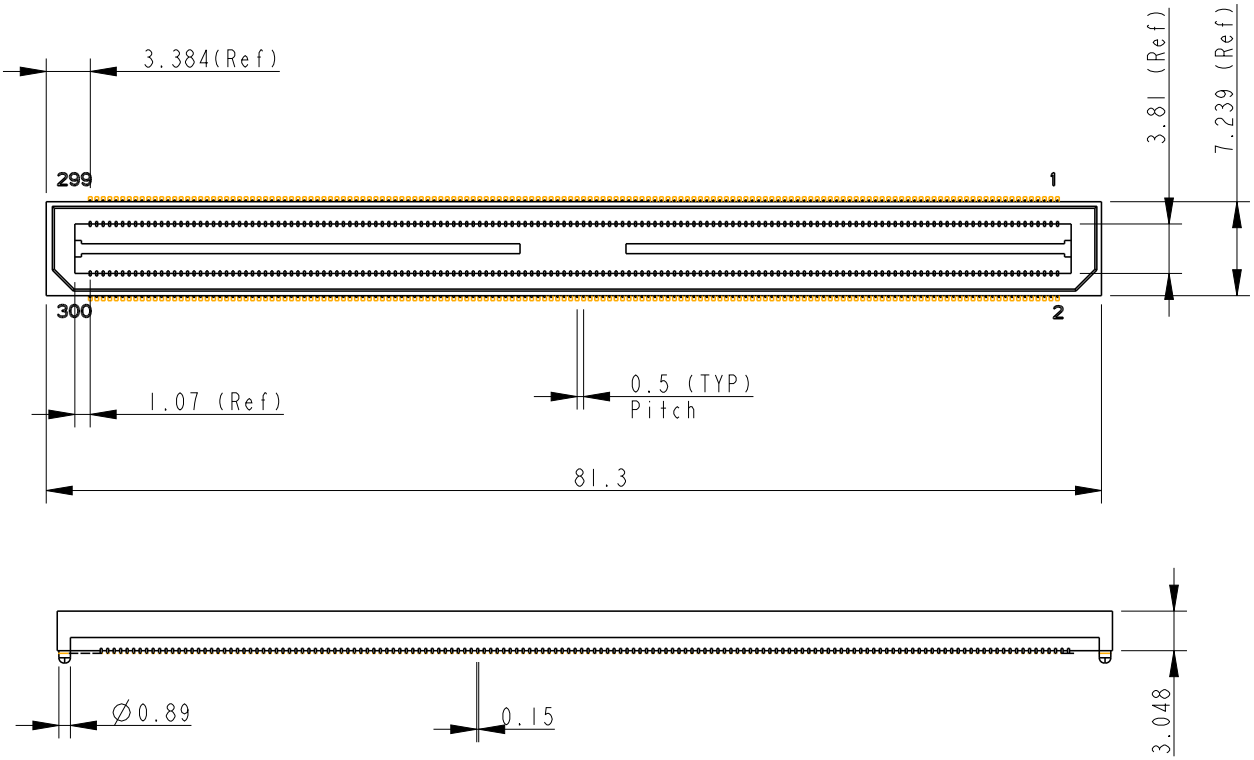
Notes:

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only. and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

Mechanical Drawing



Connector on Memory Module (BSH-150-01-L-D-A)



Revision History

Revision	Date	Description	Remark
0.1	5/5/2014	Initial release	
0.2	11/2/2015	Updated VDDSPD	
0.3	03/15/2017	Add Environmental Requirements	
0.4	09/04/2017	Remove TOPR (Operating Temperature (ambient))	
0.5	07/23/2020	Updated DRAM Component Operating Temperature Range	

Global Presence

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