19-4800; Rev 0; 3/00

MAXIM

3.3V, 622Mbps LVDS, Dual 4:2 Crosspoint Switch

General Description

The MAX3640 is a dual-path crosspoint switch for use at OC-12 data rates. The MAX3640 can be used to receive and transmit 622Mbps low-voltage differential signals (LVDS) across a backplane with minimum jitter accumulation. Each path incorporates input buffers, multiplexers, a crosspoint switch, and output drivers. The four output channels have a redundant set of outputs for test or fanning purposes. The device offers signal-path redundancy for critical data streams.

The MAX3640 has a unique power-saving feature. When a set of four output channels has been de-selected, the output drivers are powered down to reduce power consumption by 165mW. The fully differential architecture ensures low crosstalk, jitter accumulation, and signal skew.

The MAX3640 is available in a 48-pin TQFP package and operates from a +3.3V supply over the 0°C to +85°C temperature range.

Features

- **Single +3.3V Supply**
- **257mW Power Consumption (four output channels enabled)**
- **2.8ps$_{RMS}$ Output Random Jitter**
- **42ps Output Deterministic Jitter**
- **Power-Down Feature for Deselected Outputs**
- **110ps Channel-to-Channel Skew**
- **240ps Output Edge Speed**
- **LVDS Inputs/Outputs**
- **LVDS Output 3-State Enable**

Applications

SONET/SDH Backplanes

High-Speed Parallel Links

Digital Cross-Connects

System Interconnects

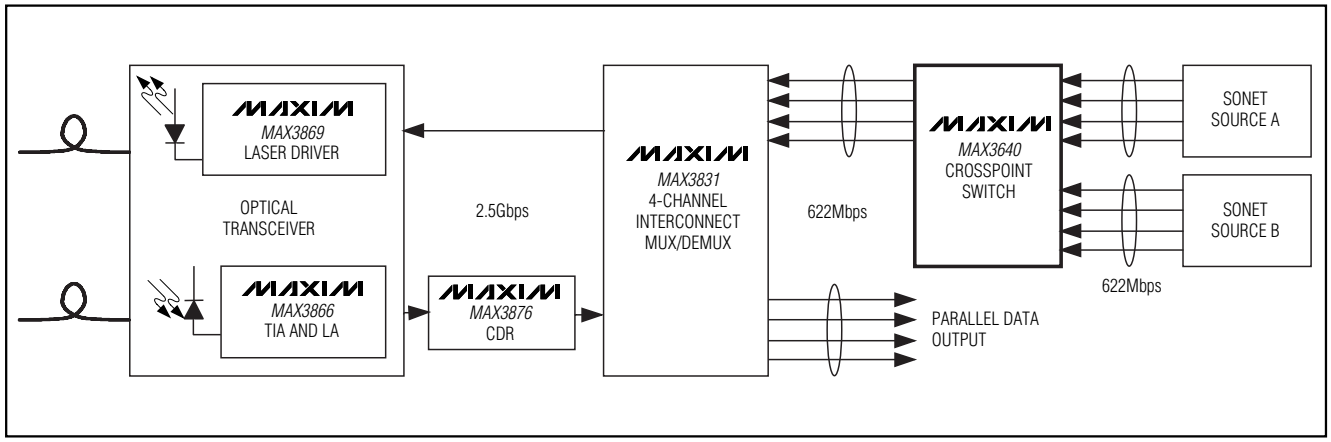
ATM Switch Cores

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3640UCM	0°C to +85°C	48 TQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



3.3V, 622Mbps LVDS, Dual 4:2 Crosspoint Switch

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .....-0.5V to 5.0V
Input Voltage (LVDS, TTL).....-0.5V to (V_{CC} + 0.5V)
Output Voltage (LVDS).....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +85°C)
48-Pin TQFP (derate 12.5mW/°C) 813mW

Operating Temperature Range.....0°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to 3.6V, LVDS differential load = 100Ω ±1%, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Eight outputs enabled		130	175	mA
		Four outputs enabled		78		
LVDS INPUTS AND OUTPUTS						
Input Voltage Range	V_{IN}		0		2400	mV
Differential Input Threshold	V_{IDTH}		-100		100	mV
Threshold Hysteresis	V_{HYST}			90		mV
Differential Input Impedance	R_{IN}		85	100	115	Ω
Input Common-Mode Current	I_{OS}	LVDS input, V_{OS} = 1.2V		245		µA
Output Voltage High	V_{OH}	Figure 1			1.475	V
Output Voltage Low	V_{OL}	Figure 1	0.925			V
Output Voltage Swing	$\|V_{OD}\|$	Figure 1	250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\|\Delta V_{OD}\|$				25	mV
Offset Output Voltage	V_{OS}	Figure 1	1.125		1.275	mV
Change in Magnitude of Output Offset Voltage for Complementary States	$\|\Delta V_{OS}\|$				25	mV
Differential Output Impedance		ENA, ENB = GND		1		MΩ
		ENA, ENB = V_{CC}	80		120	Ω
Output Current		Shorted together			12	mA
TTL INPUTS						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				0.8	V
Input Current High	I_{IH}	V_{IH} = 2.0V	-250			µA
Input Current Low	I_{IL}	V_{IL} = 0.8V	-550			µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to 3.6V, LVDS differential load = 100Ω ±1%, T_A = 0°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Parallel Input/Output Data Rate				622		Mbps
Output Rise/Fall Time	t_r, t_f	20% to 80%	150	240	350	ps
Output Random Jitter	RJ			2.8	4	ps_{RMS}
Output Deterministic Jitter	DJ	(Note 2)		42	200	ps
LVDS Output Differential Skew	t_{SKEW1}			24	50	ps
LVDS Output Channel-to-Channel Skew	t_{SKEW2}				110	ps
LVDS Output Enable Time				266		ns
LVDS Output Disable Time				66		ns
LVDS Propagation Delay from Input to Output	t_D				2.5	ns

Note 1: AC characteristics are guaranteed by design and characterization.

Note 2: Deterministic jitter (DJ) is the arithmetic sum of pattern-dependent jitter and pulse-width distortion. DJ is measured while applying 100mVp-p noise (f ≤ 2MHz) to the power supply.

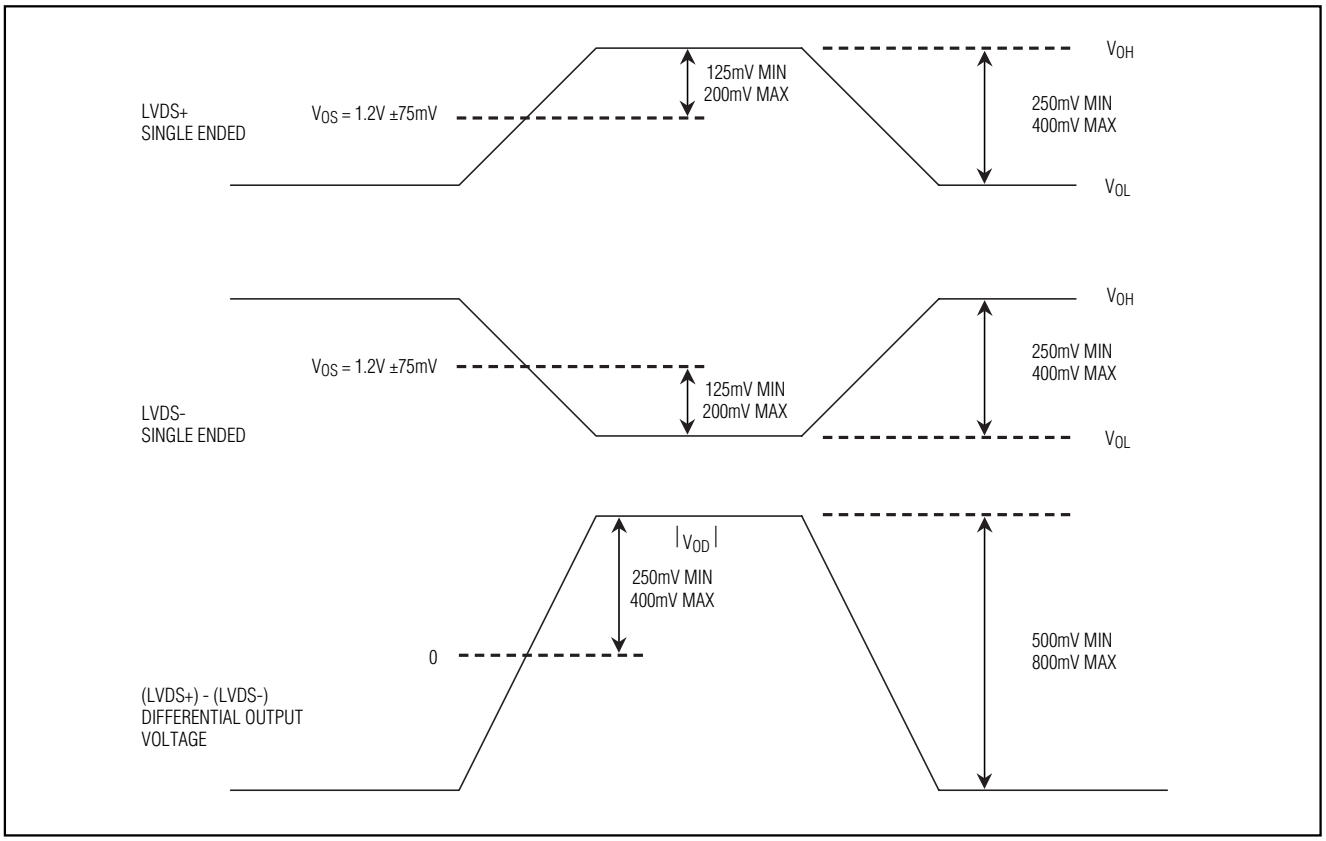


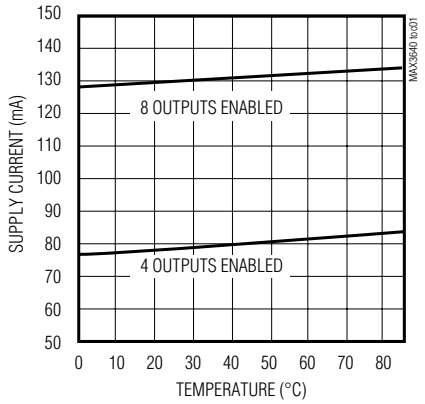
Figure 1. LVDS Output Levels

3.3V, 622Mbps LVDS, Dual 4:2 Crosspoint Switch

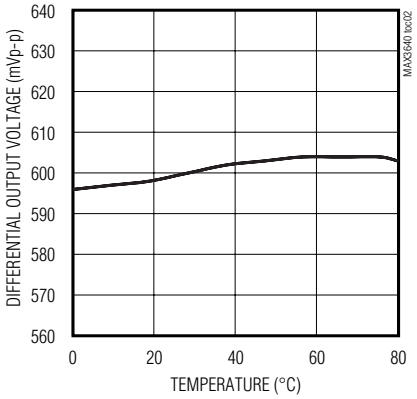
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

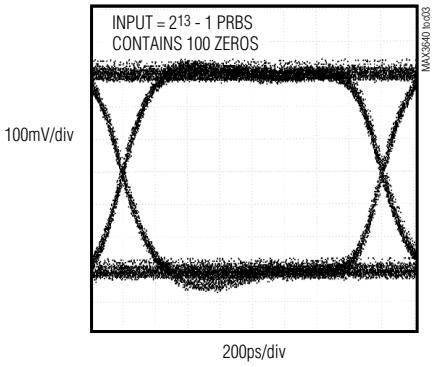
SUPPLY CURRENT vs. TEMPERATURE



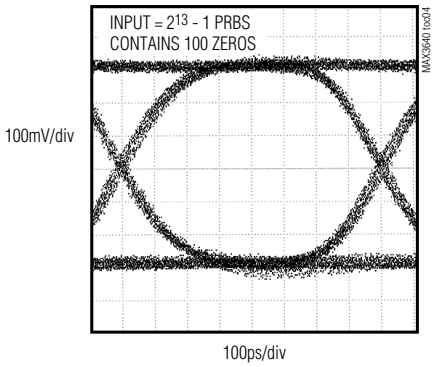
DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



622Mbps EYE DIAGRAM



1.25Gbps EYE DIAGRAM



Pin Description

PIN	NAME	FUNCTION
1, 12, 25, 36, 41	V_{CC}	Positive Supply Voltage
2, 11, 26, 35	GND	Supply Ground
3, 5, 45, 47	DIA3+, DIA4+, DIA1+, DIA2+	Positive LVDS, Channel-A Data Input
4, 6, 46, 48	DIA3-, DIA4-, DIA1-, DIA2-	Negative LVDS, Channel-A Data Input
7, 9, 13, 15	DIB1+, DIB2+, DIB3+, DIB4+	Positive LVDS, Channel-B Data Input
8, 10, 14, 16	DIB1-, DIB2-, DIB3-, DIB4-	Negative LVDS, Channel-B Data Input
17–20	SEL1–SEL4	Crosspoint Switch Select, TTL Input. (Table 1)
21, 23, 27, 29	DOB4-, DOB3-, DOB2-, DOB1-	Negative LVDS, Channel-B Data Output
22, 24, 28, 30	DOB4+, DOB3+, DOB2+, DOB1+	Positive LVDS, Channel-B Data Output
31, 33, 37, 39	DOA4-, DOA3-, DOA2-, DOA1-	Negative LVDS, Channel-A Data Output
32, 34, 38, 40	DOA4+, DOA3+, DOA2+, DOA1+	Positive LVDS, Channel-A Data Output
42	ENB	Channel-B Output Enable, TTL Input. ENB = high enables DOB1–DOB4. ENB = low powers down DOB1–DOB4 and sets them to a high-impedance state.
43	ENA	Channel-A Output Enable, TTL Input. ENA = high enables DOA1–DOA4. ENA = low powers down DOA1–DOA4 and sets them to a high-impedance state.
44	IN_SEL	Input Select Pin, TTL Input. Connect to logic high (or V_{CC}) to select DIA1–DIA4. Connect to logic low (or GND) to select DIB1–DIB4.

Detailed Description

Figure 2 shows the MAX3640's architecture. It consists of two data paths; each data path begins with four differential input buffers. The IN_SEL pin selects whether the A or B channels are passed to the 2x2 crosspoint switch that follows. The SEL_ pins control the routing of the crosspoint switch. Each crosspoint switch output drives a pair of LVDS output drivers. This provides a redundant set of outputs that can be used for fan-out or test purposes. Each set of outputs, DOA_ and DOB_, is enabled or disabled by the ENA and ENB pins. See Table 1 for routing controls.

LVDS Inputs and Outputs

The MAX3640 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 500mV to 800mV differential low-voltage swings to achieve fast transition times, low power dissipation, and improved noise immunity.

For proper operation, the data outputs require 100Ω differential termination between the inverting and noninverting pins. Do not terminate these outputs to ground. See Figure 1 for LVDS output voltage specifications.

The data inputs are internally terminated with 100Ω differential and therefore do not require external termination.

3.3V, 622Mbps LVDS, Dual 4:2 Crosspoint Switch

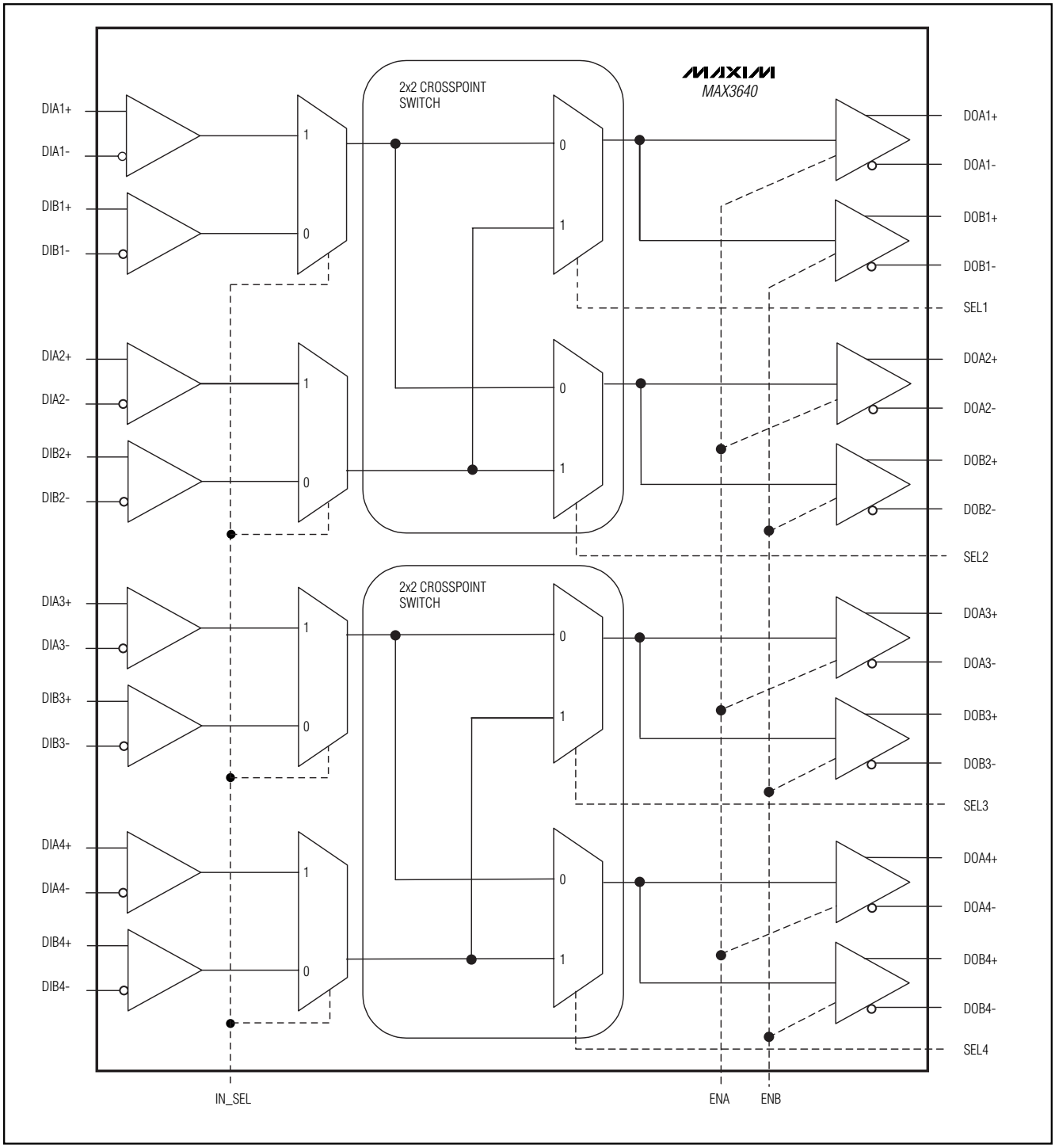


Figure 2. Functional Diagram

Table 1. Output Routing

ROUTING CONTROLS			OUTPUT SIGNALS	
IN_SEL	SEL1	SEL2	Signal at DOA1/DOB1	Signal at DOA2/DOB2
0	0	0	DIB1	DIB1
0	0	1	DIB1	DIB2
0	1	0	DIB2	DIB1
0	1	1	DIB2	DIB2
1	0	0	DIA1	DIA1
1	0	1	DIA1	DIA2
1	1	0	DIA2	DIA1
1	1	1	DIA2	DIA2
IN_SEL	SEL3	SEL4	Signal at DOA3/DOB3	Signal at DOA4/DOB4
0	0	0	DIB3	DIB3
0	0	1	DIB3	DIB4
0	1	0	DIB4	DIB3
0	1	1	DIB4	DIB4
1	0	0	DIA3	DIA3
1	0	1	DIA3	DIA4
1	1	0	DIA4	DIA3
1	1	1	DIA4	DIA4

Note: *Disabling the outputs by using ENA or ENB will drive the DOA_ or DOB_ data outputs to a high-impedance state.*

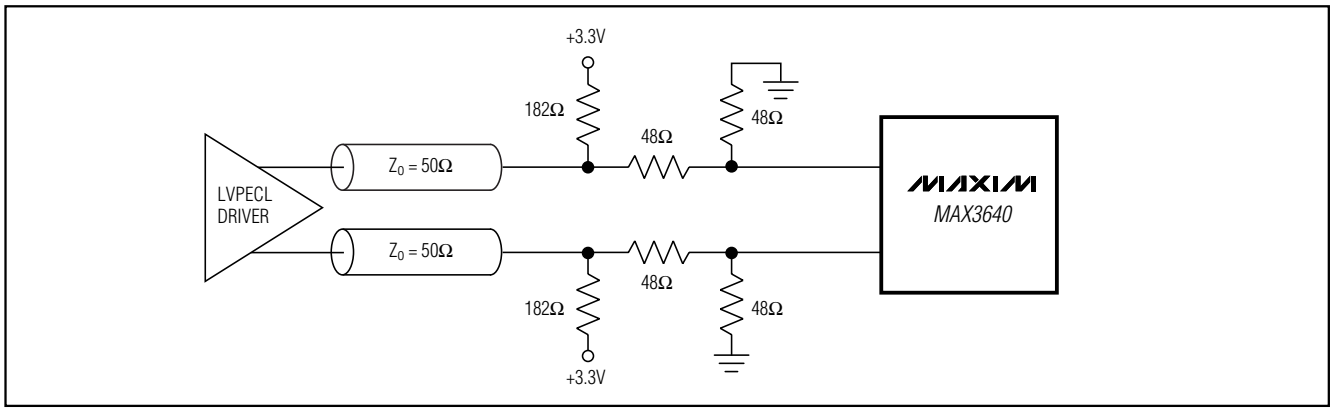


Figure 3. LVPECL to LVDS Interface

3.3V, 622Mbps LVDS, Dual 4:2 Crosspoint Switch

Applications Information

Interfacing LVPECL Outputs to MAX3640 LVDS Inputs

To DC-couple between LVPECL and LVDS, use the resistor network shown in Figure 3. Note that the LVPECL output is optimized for a 50Ω load to V_{CC} - 2V, so an equivalent network is used. Also, the network attenuation should be such that the LVPECL output signal after attenuation is well within the LVDS input range.

Note that the LVDS input impedance is a true 100Ω between the inputs. The differential impedance does not contribute to the DC termination impedance, but does contribute to the AC termination impedance. This means that AC and DC impedance will always be different.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3640 data inputs and outputs.

Interface Models

Figure 4 shows the interface model for the LVDS inputs, while Figure 5 shows the model for the LVDS outputs.

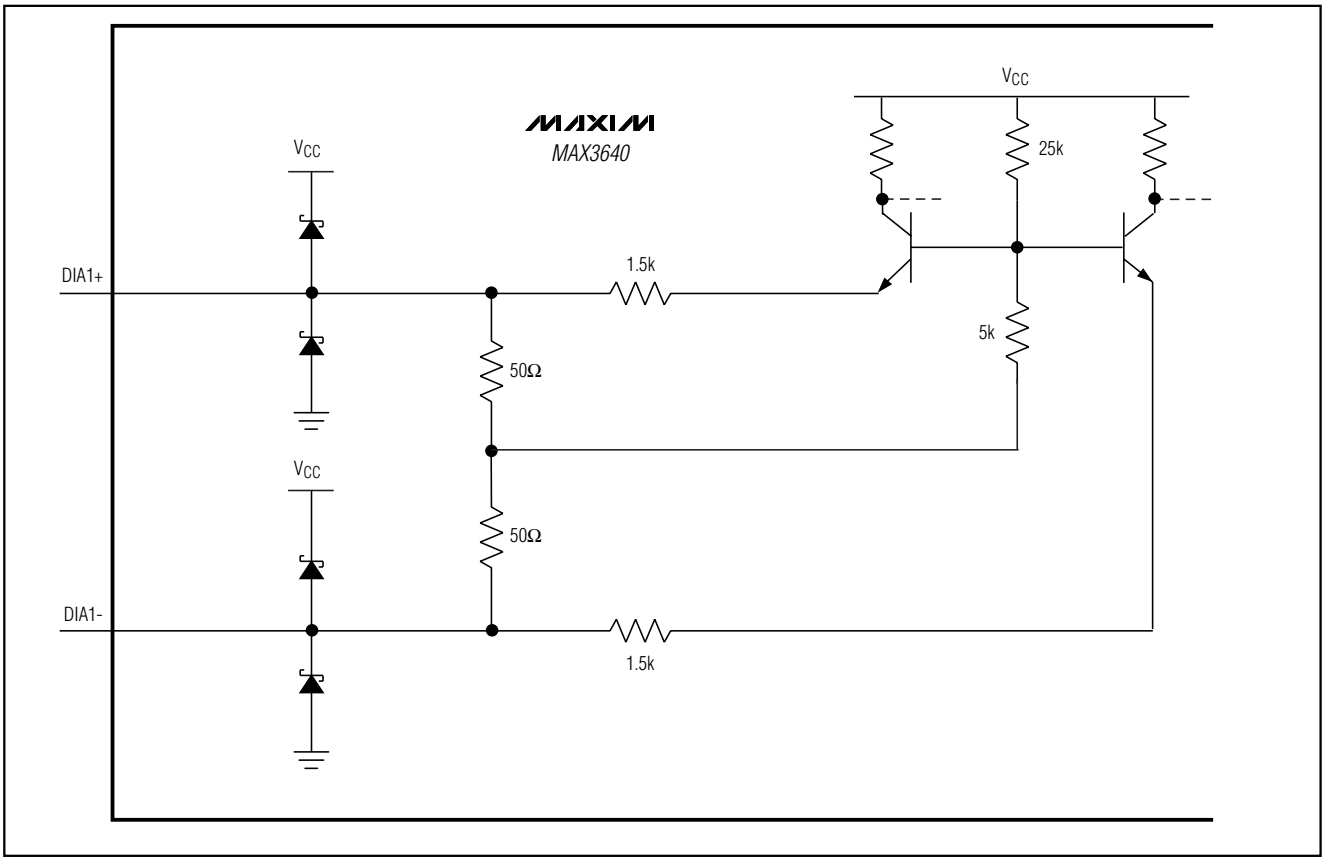


Figure 4. LVDS Input Model

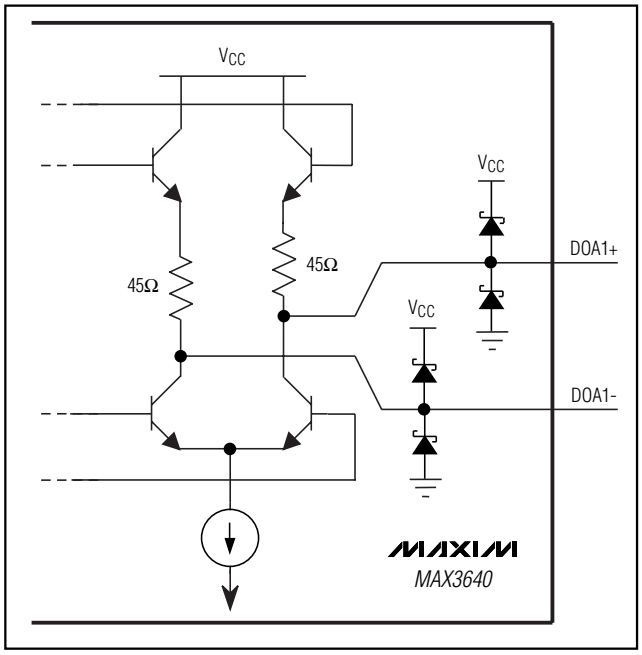
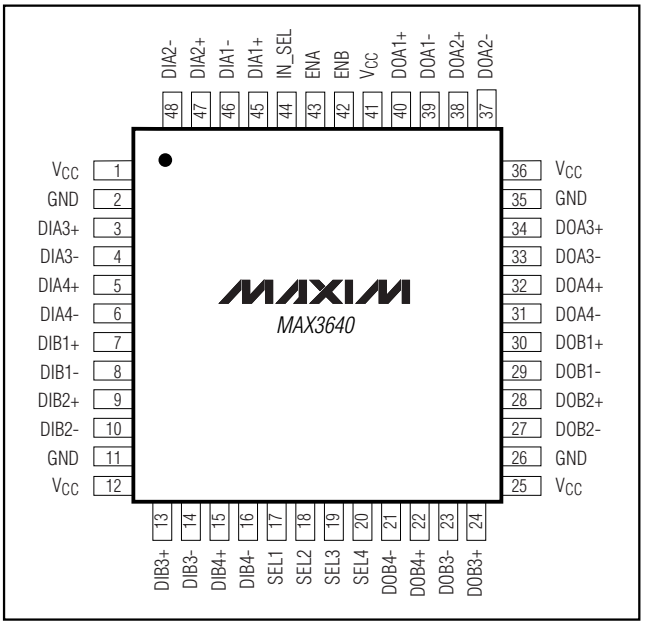


Figure 5. LVDS Output Model

Chip Information

TRANSISTOR COUNT: 2453

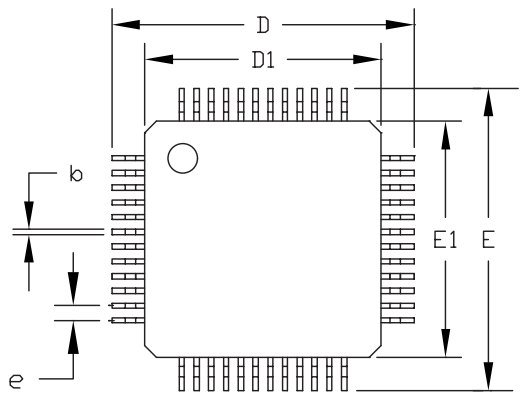
Pin Configuration

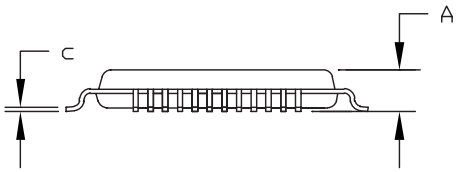


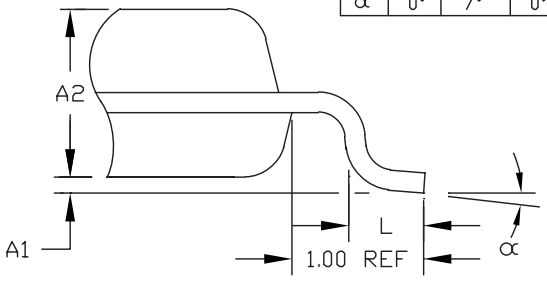
3.3V, 622Mbps LVDS, Dual 4:2 Crosspoint Switch

Package Information

32L/48L.TQFP.EPS







JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	D	1/1

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