ARM® Cortex®-M0
32-bit Microcontroller

NuMicro® Family
Mini58DE Series
Product Brief

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1 GENERAL DESCRIPTION

The NuMicro® Mini58 series is pin-to-pin and function compatible with the NuMicro® Mini51 series, the 32-bit microcontroller (MCU) embedded with the ARM® Cortex®-M0 core. The Mini58 series can bridge the gap and replace the cost equivalent to traditional 8- and 16-bit microcontroller by 32-bit performance and rich functions. The Mini58 series supports a wide range of applications from low-end, price sensitive designs to computing-intensive ones and provides advanced high-end features in economical products.

The Mini58 series can run up to 50 MHz which is faster than 24 MHz in Mini51 series, and operate at a wide voltage range of 2.5V ~ 5.5V and temperature range of -40℃ ~ +105℃. For the Mini58 series, the embedded program flash size upgrades from 16 Kbytes to 32 Kbytes and SRAM upgrades from 2 Kbytes to 4 Kbytes. The Mini58 series also offers size configurable Data Flash (shared with program flash), and 2.5 Kbytes flash for the ISP.

The Mini58 series has many high-performance peripheral functions, such as 22.1184 MHz internal RC oscillator (±1% accuracy), I/O port with up to 30 pins, four 32-bit timers, two UARTs with the RS485 function and IrDA function interface, one SPI interface, two I^2C interfaces, up to three 16-bit PWM generators providing six channels, an 8-channel 10-bit ADC, Watchdog Timer, Window Watchdog Timer, two Analog Comparators and a Brown-out Detector. All these peripherals have been incorporated into the Mini58 series to reduce component count, board space and system cost. Compared to the Mini51 series, the Mini58 series supports additional one UART and one I^2C interface for better and more flexible connectivity applications.

Additionally, the Mini58 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product. The Mini58 series also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded flash updated.

2 FEATURES

- Core
  - ARM® Cortex®-M0 core running up to 50 MHz
  - One 24-bit system timer
  - Supports low power Idle mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watchpoints/four breakpoints
- Built-in LDO for wide operating voltage: 2.5V to 5.5V
- Memory
  - 32 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2.5 KB Flash for loader (LDROM)
  - 4 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - Support 4 ~ 24 MHz external high speed crystal oscillator (HXT) for precise timing operation
  - Support 32.768 kHz external low speed crystal oscillator (LXT) for idle wake-up and system operation clock
  - Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (1% accuracy at 25^0C, 5V)
    - Dynamically calibrating the HIRC OSC to 22.1184 MHz ±1% from -40℃ to 105℃ by external 32.768K crystal oscillator (LXT)
  - Built-in 10 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
  - PLL allowing CPU operation up to the maximum 50 MHz
- I/O Port
  - Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
  - Four I/O modes:
    - Quasi-bidirectional input/output
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - Optional Schmitt trigger input
- Timer
  - Provides two channel 32-bit Timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer

- Supports Event Counter mode
- Supports Toggle Output mode
- Supports external trigger in Pulse Width Measurement mode
- Supports external trigger in Pulse Width Capture mode

- WDT (Watchdog Timer)
  - Programmable clock source and time-out period
  - Supports wake-up function in Power-down mode and Idle mode
  - Interrupt or reset selectable on watchdog time-out
- WWDT (Window Watchdog Timer)
  - 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible
  - Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter
- PWM
  - Up to three built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-time generator for each PWM generator
  - PWM interrupt synchronized to PWM period
  - Supports edge-alignment or center-alignment
  - Supports fault detection
- UART (Universal Asynchronous Receiver/Transmitters)
  - Two UART devices
  - Buffered receiver and transmitter, each with 16-byte FIFO
  - Optional flow control function (CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Supports RS-485 function
- SPI (Serial Peripheral Interface)
  - One SPI device
  - Master up to 25 MHz, and Slave up to 10 MHz
  - Supports Master/Slave mode
  - Full-duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - RX latching data can be either at rising edge or at falling edge of serial clock
  - TX sending data can be either at rising edge or at falling edge of serial clock
  - Supports Byte Suspend mode in 32-bit transmission
- I^2C

- Two I^2C devices
- Supports Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow for versatile rate control
- Supports multiple address recognition (four slave addresses with mask option)

- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 250 kSPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger or external pin trigger
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Built-in CRV (comparator reference voltage)
- ISP (In-System Programming), ICP (In-Circuit Programming), and IAP (In-Application-Programming) update
- BOD (Brown-out Detector)
  - With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
  - Threshold voltage level: 2.0V
- Operating Temperature: -40℃~105℃
- Reliability: EFT > ± 4KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro® Mini58 Series Naming Rule

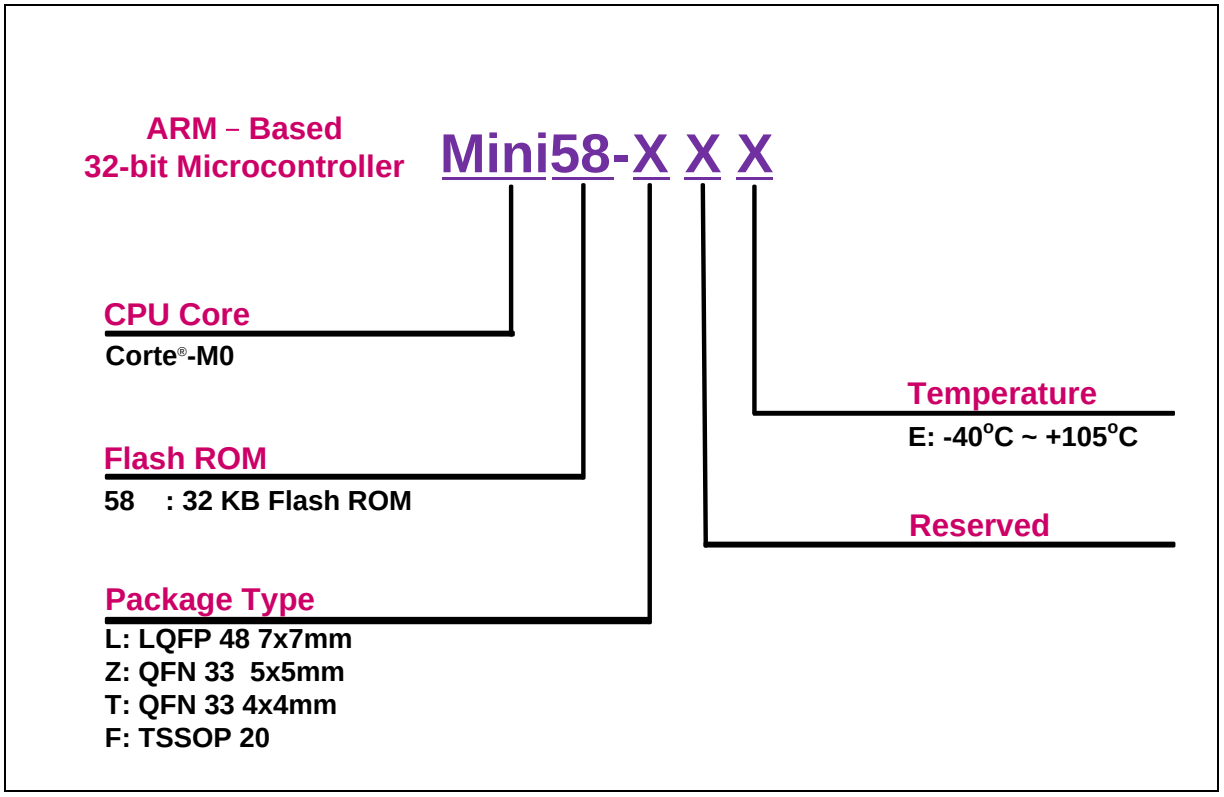


Figure 3.1-1 NuMicro® Mini58 Series Naming Rule

3.2 NuMicro® Mini58 Series Product Selection Guide

Part Number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI58LDE	32 KB	4 KB	Configurable	2.5 KB	up to 30	2x32-bit	2	1	2	2	6	8x10-bit	v	v	LQFP48
MINI58ZDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(5x5)
MINI58TDE	32 KB	4 KB	Configurable	2.5 KB	up to 29	2x32-bit	2	1	2	2	6	8x10-bit	v	v	QFN33(4x4)
MINI58FDE	32 KB	4 KB	Configurable	2.5 KB	up to 17	2x32-bit	2	1	2	-	6	4x10-bit	v	v	TSSOP20

Table 3.2-1 NuMicro® Mini58 Series Product Selection Guide

3.3 PIN CONFIGURATION

3.3.1 LQFP 48-pin

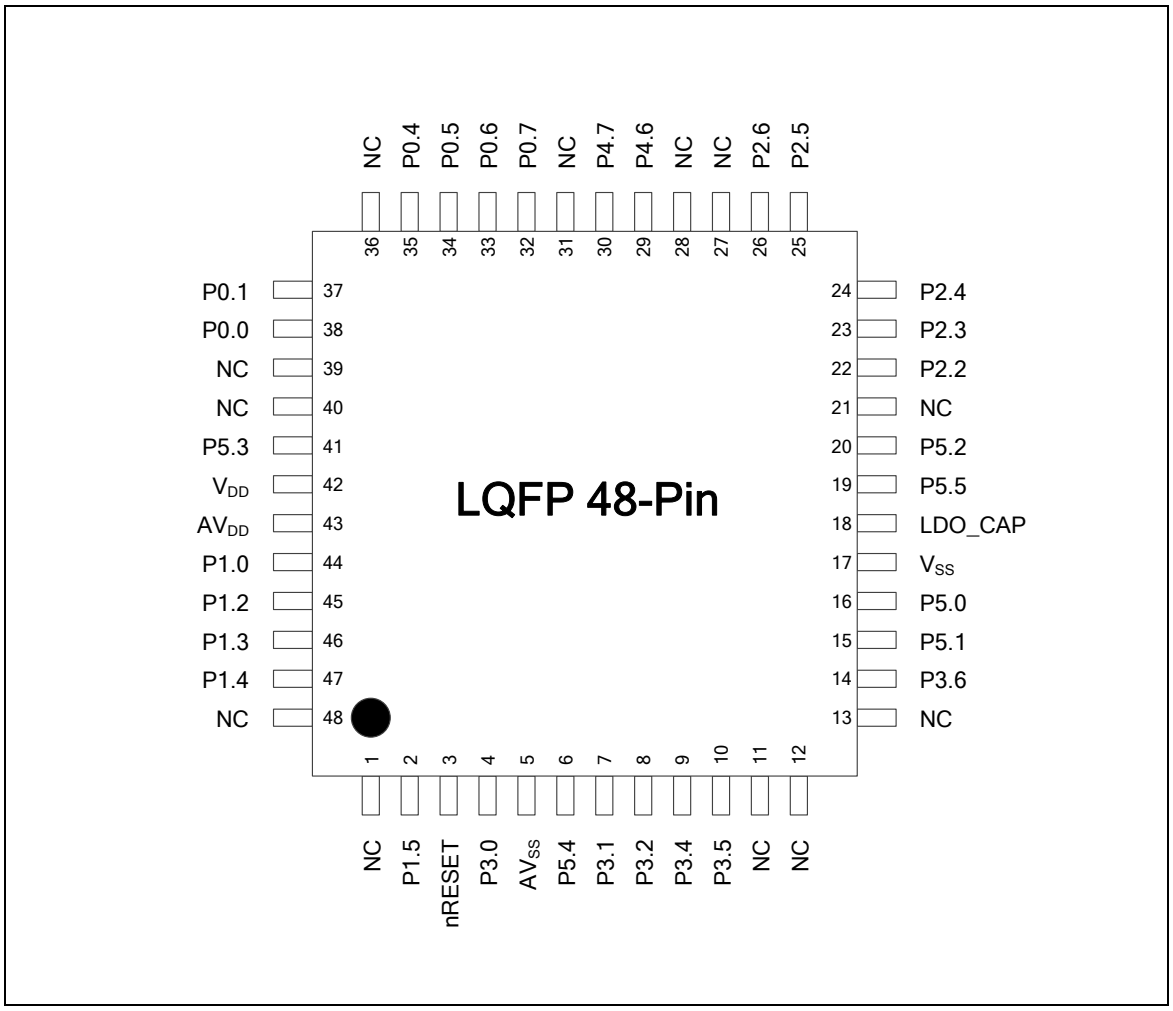


Figure 3.3-1 NuMicro® Mini58 Series LQFP 48-pin Diagram

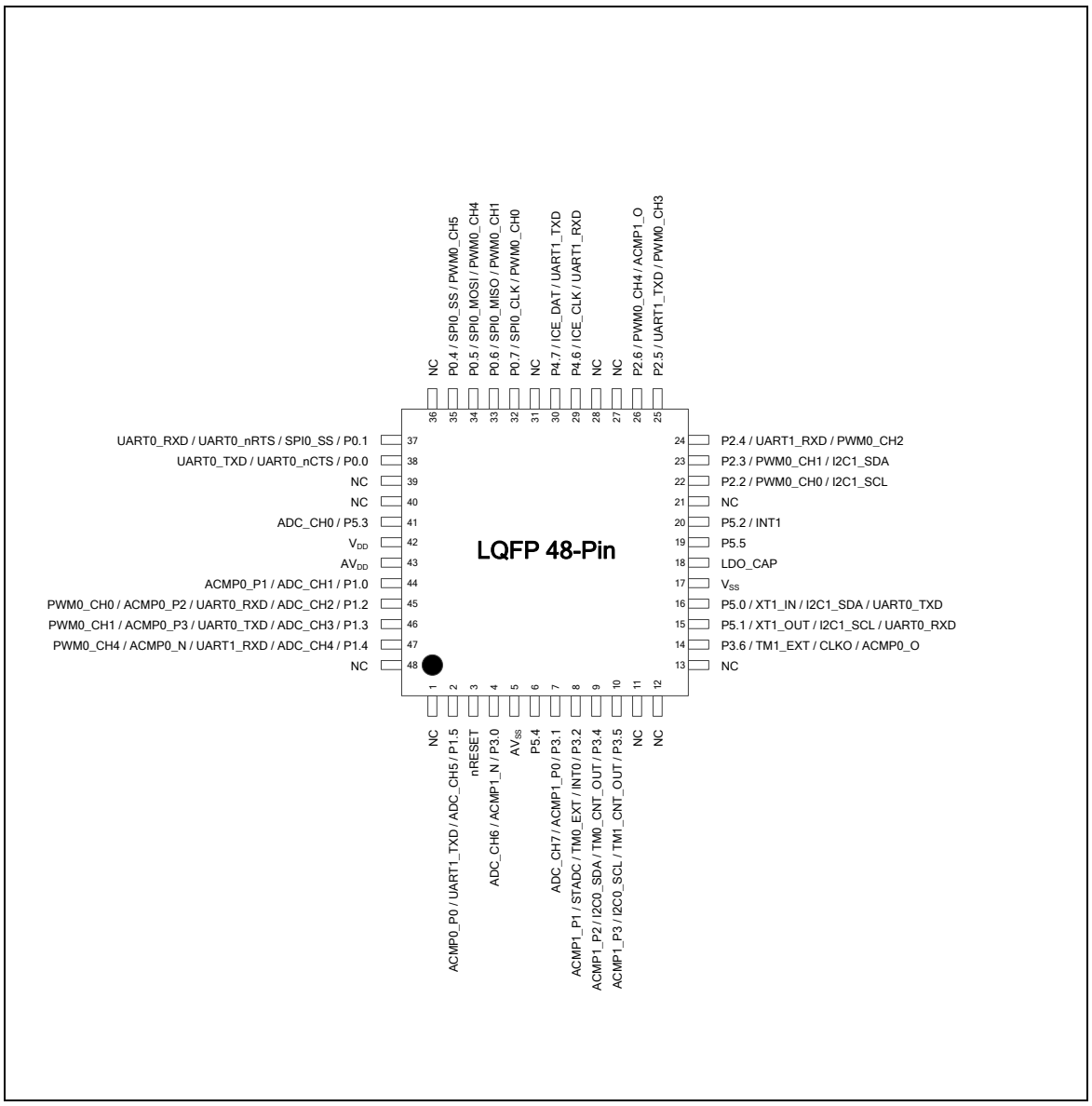


Figure 3.3-2 NuMicro® Mini58 Series LQFP 48-pin Multi-Function Diagram

3.3.2 QFN 33-pin

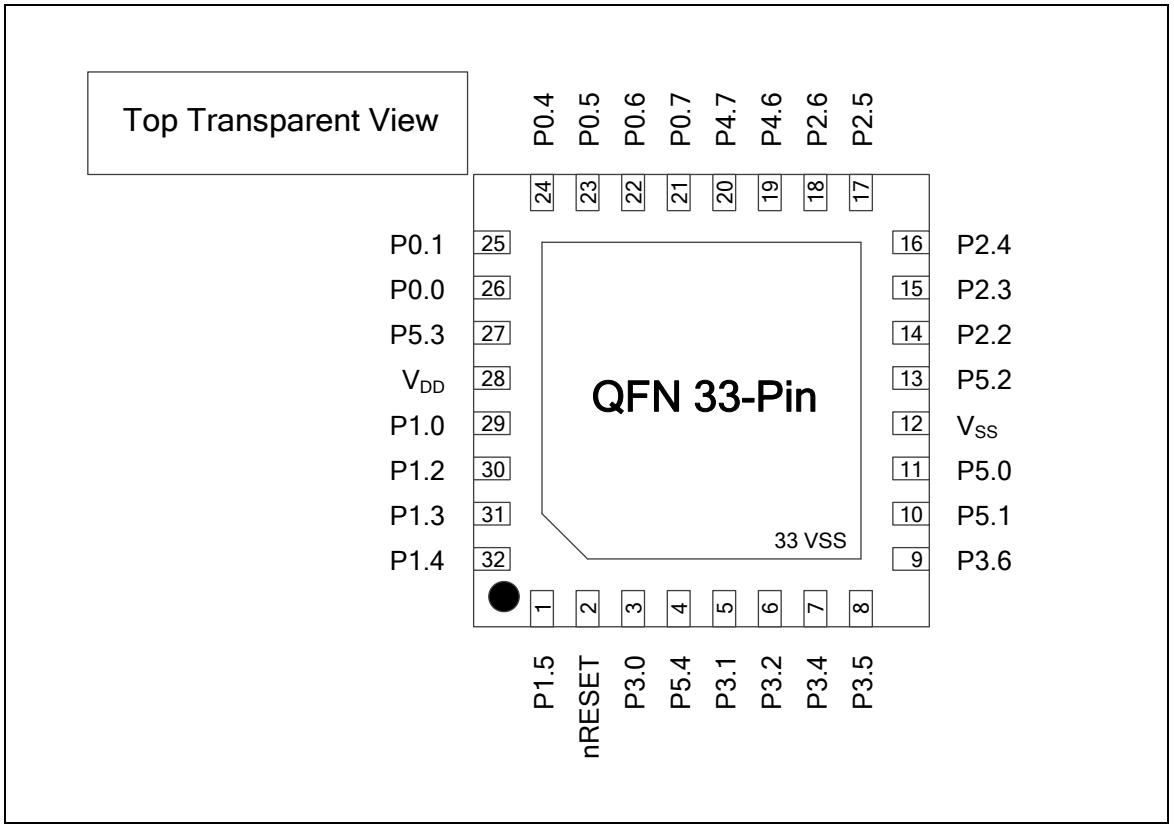


Figure 3.3-3 NuMicro® Mini58 Series QFN 33-pin Diagram

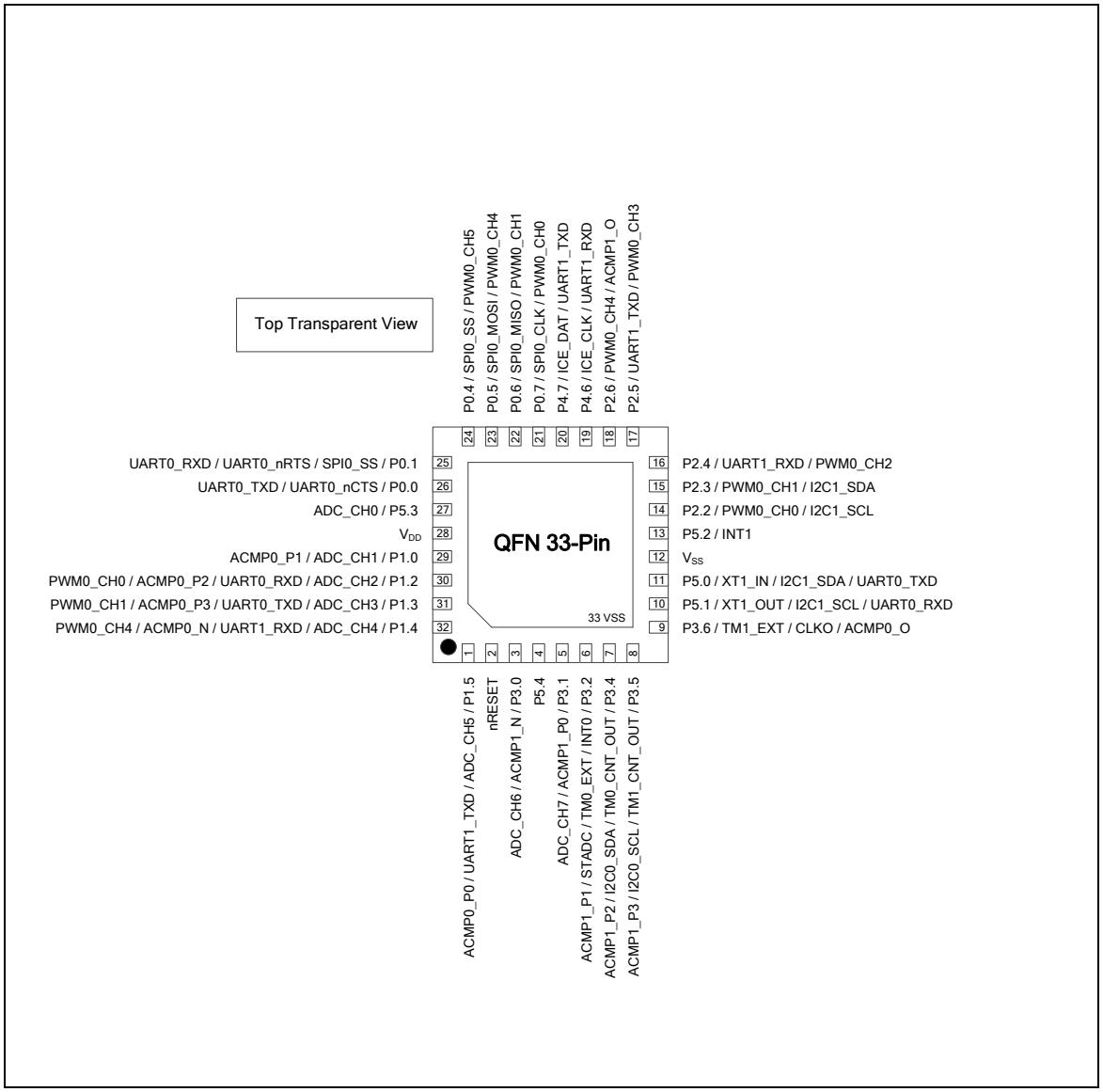


Figure 3.3-4 NuMicro® Mini58 Series QFN 33-pin Multi-funciton Diagram

3.3.3 TSSOP 20-pin

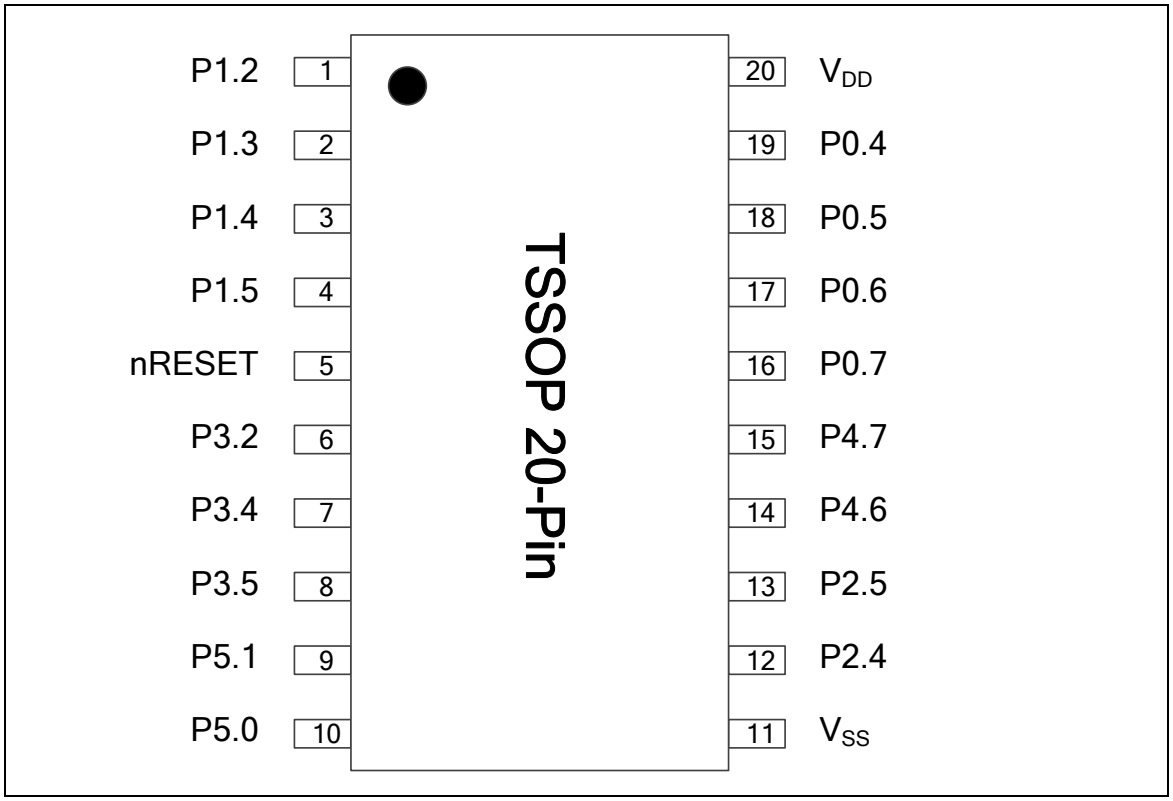


Figure 3.3-5 NuMicro® Mini58 Series TSSOP 20-pin Diagram

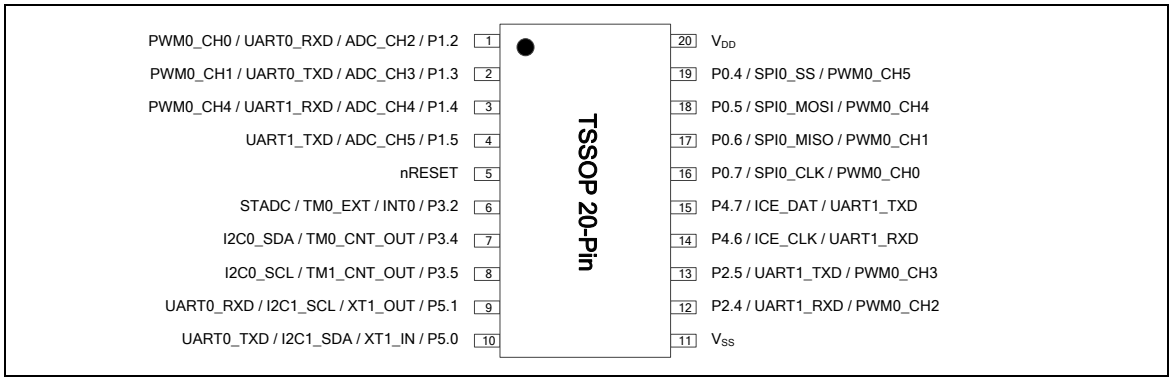


Figure 3.3-6 NuMicro® Mini58 Series TSSOP 20-pin Multi-function Diagram

4 BLOCK DIAGRAM

4.1 NuMicro® Mini58 Block Diagram

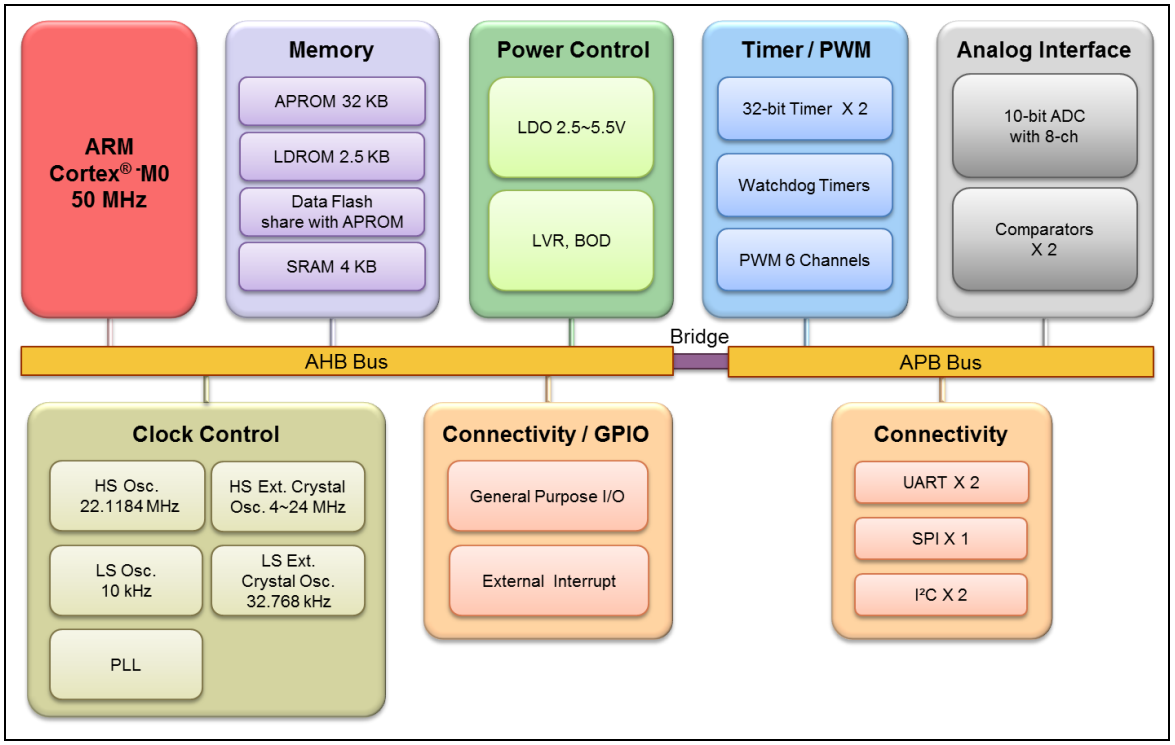
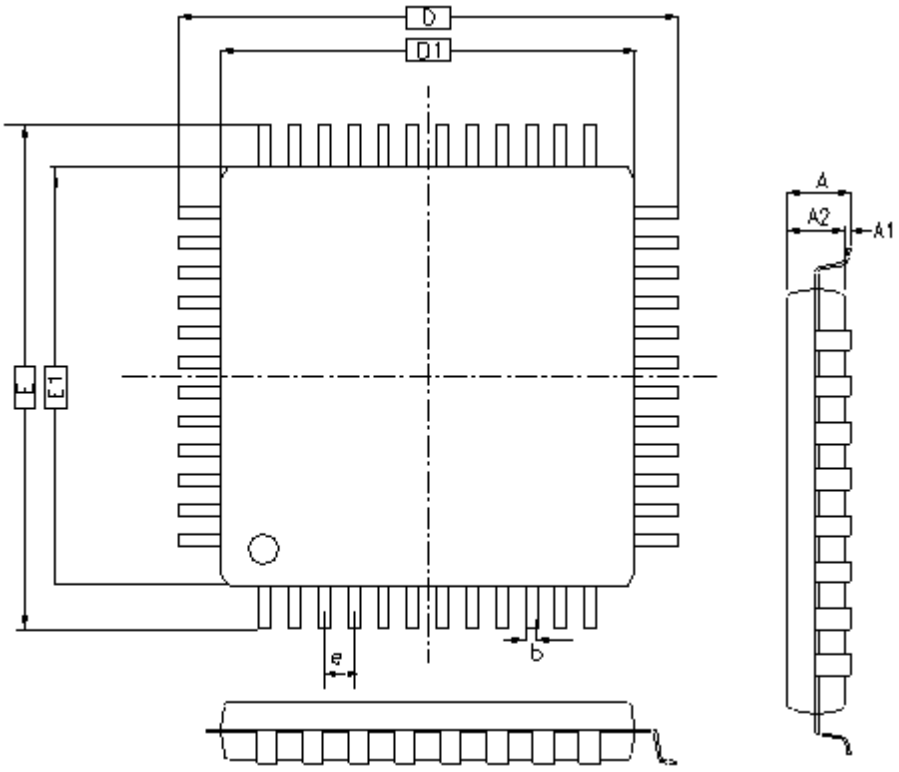


Figure 4.1-1 NuMicro® Mini58 Series Block Diagram

5 PACKAGE DIMENSIONS

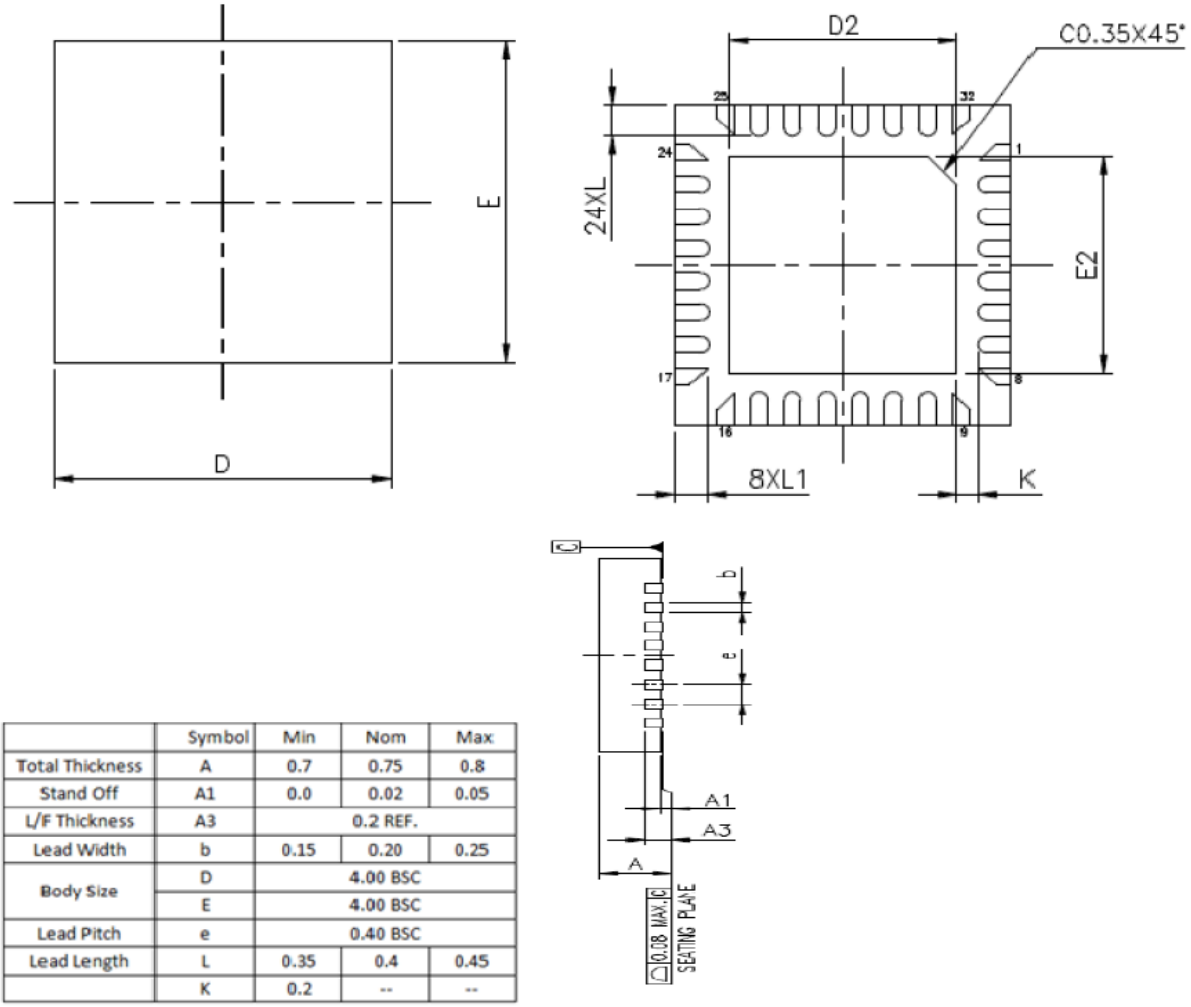
5.1 48-pin LQFP



CONTROL DIMENSIONS ARE IN MILLIMETERS

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.026
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.004	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

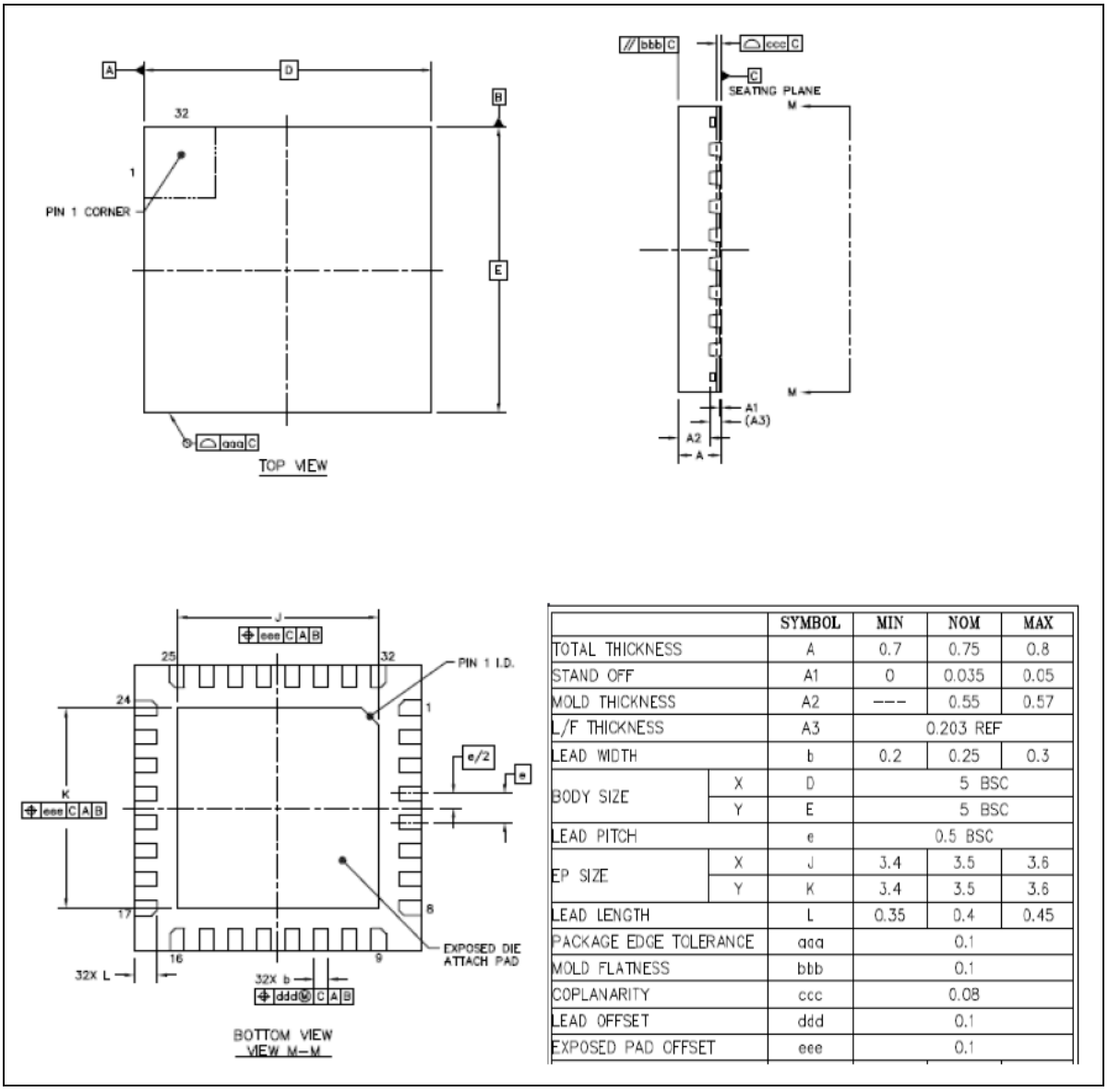
5.2 33-pin QFN (4 mm x 4 mm)



	Symbol	Min	Nom	Max
Total Thickness	A	0.7	0.75	0.8
Stand Off	A1	0.0	0.02	0.05
L/F Thickness	A3		0.2 REF.	
Lead Width	b	0.15	0.20	0.25
Body Size	D		4.00 BSC	
	E		4.00 BSC	
Lead Pitch	e		0.40 BSC	
Lead Length	L	0.35	0.4	0.45
	K	0.2	--	--

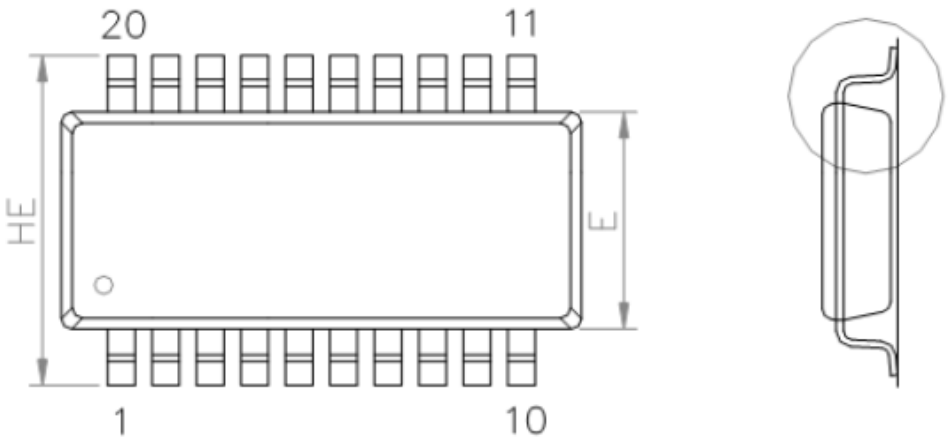
Symbol	L/F SIZE	Dimension in mm		
		MIN.	NOR.	MAX.
D2	114X114 mm	2.6	2.7	2.75
E2		2.6	2.7	2.75

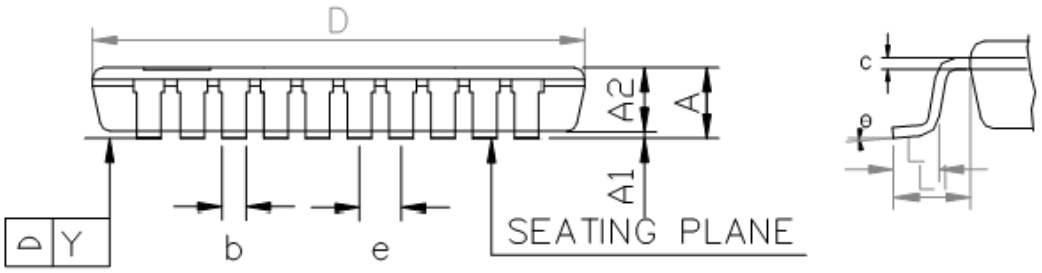
5.3 33-pin QFN (5 mm x 5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

5.4 20-pin TSSOP





SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

6 REVISION HISTORY

Date	Revision	Description
2015.06.11	1.00	Preliminary version.
2015.10.12	1.01	Updated LDROM size from 2 Kbytes to 2.5 Kbytes.

Important Notice

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