DATA SHEET

(DOC No. HX6537-A-DS)

HX6537-A

WE-I Plus ASIC

Preliminary version 01 February, 2020

Himax Technology, Inc.
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Revision History

February, 2020

Version	Date	Description of changes
01	2020/02/03	New setup.

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1. General Description

The HX6537-A is an ultra-low power, high performance microcontroller designed for battery-powered TinyML applications.

The HX6537-A is embedded with a powerful 400MHz ARC EM9D DSP core with Floating Point Unit and XY local data memory architecture to accelerate convolution operation of neural network algorithm. There are internal 2 MB ultra-low-leakage SRAMs for system and program usage. With the benefit of DSP instruction and XY memory architecture, HX6537-A can operate at lower clock speed to achieve the same application performance for lower power consumption.

Besides traditional interrupt-based trigger wakeup mechanism from deep-sleep or shutdown mode, HX6537-A provides a new multi-layer power management scheme to wakeup CMOS sensor periodically for ultra-low power applications. The multi-layer power management is controlled by hardware state machine, and the trigger condition of power layer change is the result of "Vision" detection. The EM9D core is placed in 2nd power layer to save main power consumption. Normally, EM9D core is in power shut-off state until 1st layer detection completed. There are hardware image accelerators in 1st layer to provide pre-processing of vision tasks and provide a wake-up trigger when event is detected. It can lower power consumption and maintain required response time and accuracy in "always-on" Computer Vision applications.

Security is a key consideration in Internet of Things and other embedded applications. HX6537-A provides hardware secure engine for secure boot, secure OTA firmware update, and secure meta data output with minimum processing latency.
HX6537-A also provides rich peripheral interfaces for application need, including CMOS sensor interface, audio I^2S and PDM interface, and peripheral interfaces of UART, I^2C, SPI, GPIO and ADC.

2. Features

- Ultra-low power and high-performance ARC EM9D DSP with FPU
  - 320 kB program ICCM local memory
  - 320 kB data DCCM/XCCM/YCCM local memory
  - 1472 kB system memory
  - 64 kB boot ROM
  - SIP 1MB/2MB Flash (LQFP/QFN packages only)
  - Frequency up to 400MHz
- Image hardware accelerators
  - Motion detection – Change Detection Module
  - 2x2 sub-sampler and filter
  - 5x5 de-mosaic and filter
  - JPEG codec
  - HOG extraction
  - Programmable re-sampler
- Security
  - True random number generator
  - Secure boot, secure OTA, secure meta data output
- Sensor input interface
  - 1/4/8-bit sensor interface
  - Up to 60fps@VGA
- Audio interface
  - PDM Rx for mono and stereo audio microphone input
  - I²S Rx/Tx for audio input and output
- Peripheral interfaces
  - 2x 1/2/4-bit SPI master, up to 50MHz
  - 1x SPI slave, up to 50MHz
  - 3x I²C master, up to 1MHz
  - 1x I²C slave, up to 1MHz
  - 2x UART interface with Tx and Rx FIFO
  - 3x PWM
  - GPIOs
- ADC interface
  - Up to 4-channels
  - 1x 12-bit 1 MSPS ADC
- Power management
  - Low power modes – Active, Standby, Sleep and Shutdown
  - Hardware Power Management Unit
  - SRAM retention to reduce EM9D startup time
- Debug mode
  - Two-wire JTAG interface
- Clock, reset and supply management
  - 1.8 V supply for core
  - 1.8 V to 3.3 V supply for I/Os
  - POR and BOR
  - 24 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Internal 36 MHz factory-trimmed RC oscillator
  - Internal 32 kHz RC oscillator with calibration

- Package
  - WLCSP-38: 4.695 mm x 1.604 mm
  - LQFP-128: 16 mm x 16 mm
  - QFN-72: 8 mm x 8 mm

3. Block Diagram

Below diagram shows the functional modules in HX6537-A.

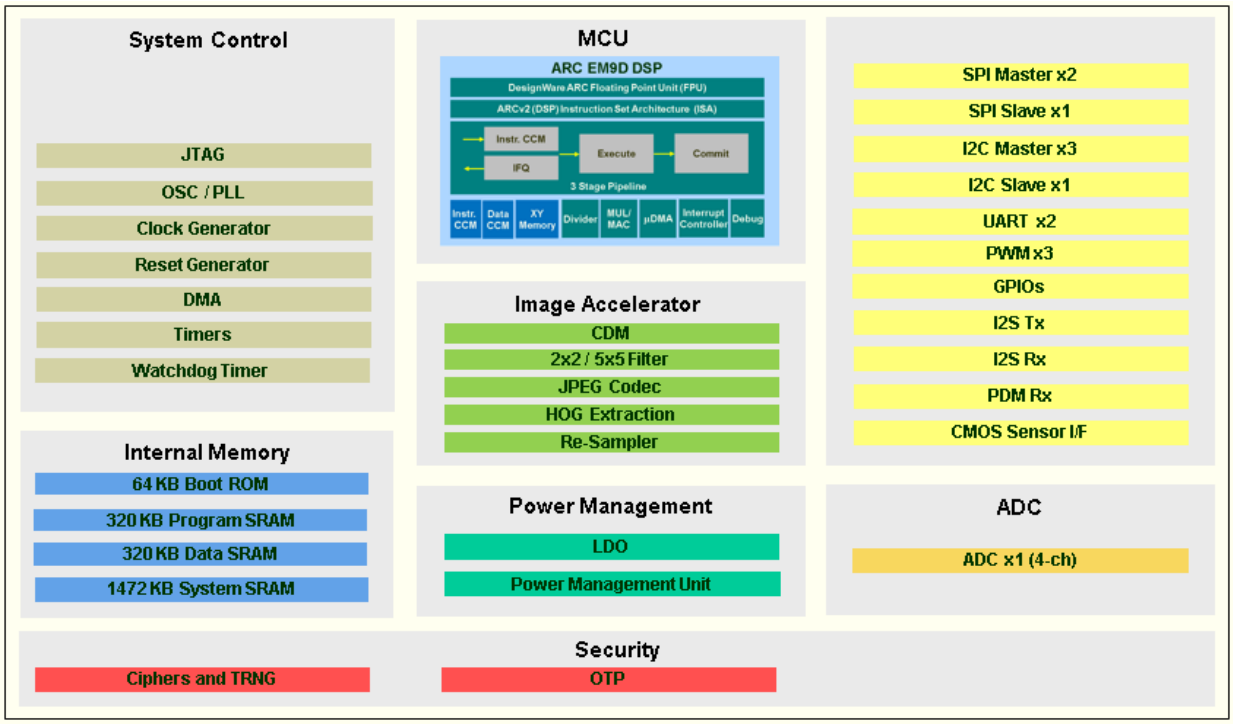


Figure 3.1: HX6537-A block diagram

4. Pin Assignment

Pin Types: **A**=Analog, **I**=Input, **O**=Output, **P**=Power, **G**=Ground

Pin name	LQFP-128 Pin no.	QFN-72 Pin no.	WLCSP-38 Pin no.	Type	Pad	Description
ADC_IP3	1	-	-	AI	-	ADC Input Ch3_P.
ADC_IP2	2	-	-	AI	-	ADC Input Ch2_P.
ADC_IN3	3	-	-	AI	-	ADC Input Ch3_N.
ADC_IN2	4	-	-	AI	-	ADC Input Ch2_N.
ADC_VREFN_IN	5	-	-	AI	-	ADC VREFN input.
ADC_AVSS18	6	1	-	G	Ground	ADC GND.
ADC_IN1	7	-	-	AI	-	ADC Input Ch1_N.
ADC_AVDD18	8	2	-	P	1.8V	ADC PWR.
ADC_IN0	9	3	-	AI	-	ADC Input Ch0_N.
ADC_IP1	10	-	-	AI	-	ADC Input Ch1_P.
ADC_IP0	11	4	-	AI	-	ADC Input Ch0_P.
ADC_VREFP_IN	12	5	-	AI	-	ADC VREFP input.
ADC_VREFP_OUT	13	-	-	AO	-	ADC VREFP output.
PLL_VDD18	14	6	B14	P	1.8V	PLL PWR.
PLL_VSS18	15	7	-	P	Ground	PLL GND.
CLDO_OUT	16	8	C15	AO	-	CLDO 0.9V output.
CLDO_AVSS18	17	-	-	G	Ground	CLDO GND.
POR_AVSS18	18	-	-	G	Ground	POR GND.
CLDO_AVDD18	19	9	C13	P	1.8V	CLDO PWR.
POR_AVDD18	20	-	-	P	1.8V	POR PWR.
XA_32K	21	-	-	I	-	XTAL32K input A.
XB_32K	22	-	-	O	-	XTAL32K input B.
XTALOUT_24M	23	11	D14	O	-	XTAL24M output.
XTALIN_24M	24	10	E15	I	-	XTAL24M input.
PGPIO0	25	12	-	I/O	-	PIF GPIO0 **(AON)**.
PGPIO1	26	13	-	I/O	-	PIF GPIO1 **(AON)**.
BOOT_OPT0	27	14	C11	I/O	-	1. Boot option selection pin0. 2. PDM clock.
BOOT_OPT1	28	15	D10	I/O	-	1. Boot option selection pin1. 2. PDM data in.
TESTMODE	29	16	D12	I/O	-	Test Mode enable pin.
BOOT_OPT3	30	-	-	I/O	-	Boot option selection pin3.
RESETN	31	17	E13	I	-	Reset pin.
BOOT_OPT2	32	18	E11	I/O	-	Boot option selection pin2.
PIF_IOVDD	33	19	C9	P	1.8V~3.3V	PIF IO Power.
PGPIO2	34	20	-	I/O	-	PIF GPIO2 **(AON)**.
PGPIO3	35	21	D8	I/O	-	PIF GPIO3 **(AON)**.
PGPIO4	36	22	E9	I/O	-	PIF GPIO4 **(AON)**.
PGPIO5	37	23	-	I/O	-	PIF GPIO5 **(AON)**.
PGPIO6	38	24	-	I/O	-	PIF GPIO6 **(AON)**.
PIF_IOGND	39	-	C5	G	Ground	PIF IO GND.
DGND	40	-	-	G	Ground	Core GND.
PI2C_SLV_SCK	41	25	D6	I/O	-	PIF I2C slave clock.
PI2C_SLV_SDA	42	26	E7	I/O	-	PIF I2C slave data.
DCDC_SW	43	27	-	I/O	-	DCDC switch control.
PI2C_M1_SCK	44	-	-	I/O	-	PIF I2C master1 clock.
PI2C_M1_SDA	45	-	-	I/O	-	PIF I2C master1 data.
PI2C_M0_SCK	46	28	-	I/O	-	PIF I2C master0 clock.
PI2C_M0_SDA	47	29	-	I/O	-	PIF I2C master0 data.

Pin name	LQFP-128 Pin no.	QFN-72 Pin no.	WLCSP-38 Pin no.	Type	Pad	Description
I2S_WS	48	30	-	I/O	-	I2S word select.
PDM_SDI	49	31	-	I/O	-	PDM data in.
I2S_SCLK	50	32	-	I/O	-	I2S clock.
I2S_SDO	51	33	-	I/O	-	I2S data out.
PDM_CLK	52	-	-	I/O	-	PDM clock.
SLDO_AVSS18	53	-	-	G	Ground	SLDO GND.
SLDO_AVDD18	54	34	E5	P	1.8V	SLDO PWR.
SLDO_OUT	55	35	D4	AO	-	SLDO 0.9V output.
UART0_RX	56	-	-	I/O	-	UART0 RX pin.
UART0_TX	57	-	-	I/O	-	UART0 TX pin.
DGND	58	-	-	G	Ground	Core GND.
PSPI_SLV_SCLK	59	-	-	I/O	-	PIF SPI slave clock.
PSPI_SLV_CS	60	-	-	I/O	-	PIF SPI slave chip select.
PSPI_SLV_SDI	61	-	-	I/O	-	PIF SPI slave data in.
PSPI_SLV_SDO	62	-	-	I/O	-	PIF SPI slave data out.
UART1_RX	63	36	E3	I/O	-	UART1 RX pin.
UART1_TX	64	37	E1	I/O	-	UART1 TX pin.
PSPI_CS0	65	38	-	I/O	-	PIF SPI master chip select0.
PSPI_CS1	66	-	-	I/O	-	PIF SPI master chip select1.
PSPI_CS2	67	-	-	I/O	-	PIF SPI master chip select2.
PSPI_CS3	68	-	-	I/O	-	PIF SPI master chip select3.
PSPI_SDIO0	69	39	-	I/O	-	PIF SPI master data0.
PSPI_SDIO1	70	40	-	I/O	-	PIF SPI master data1.
PSPI_SCLK	71	41	-	I/O	-	PIF SPI master clock.
PSPI_SDIO2	72	42	-	I/O	-	1. PIF SPI master data2. 2. PIF I2C master1 clock.
PSPI_SDIO3	73	43	-	I/O	-	1. PIF SPI master data3. 2. PIF I2C master1 data.
DGND	74	-	-	G	Ground	Core GND.
PGPIO7	75	-	-	I/O	-	PIF GPIO7.
PGPIO8	76	44	D2	I/O	-	PIF GPIO8.
PIF_IOVDD	77	45	C9	P	1.8V~3.3V	PIF IO PWR.
PGPIO9	78	46	C1	I/O	-	PIF GPIO9.
PGPIO10	79	-	-	I/O	-	PIF GPIO10.
PGPIO11	80	-	-	I/O	-	PIF GPIO11.
PGPIO12	81	-	-	I/O	-	PIF GPIO12.
PGPIO13	82	-	-	I/O	-	PIF GPIO13.
PGPIO14	83	-	-	I/O	-	PIF GPIO14.
SGPIO1	84	47	C3	I/O	-	SIF GPIO1 **(AON)**.
CLDO_OUT	85	48	C7	AO	-	CLDO 0.9V output.
SEN_INT	86	49	A1	I/O	-	Sensor Interrupt.
SGPIO0	87	-	-	I/O	-	SIF GPIO0 **(AON)**.
SI2C_M_SDA	88	50	B2	I/O	-	SIF I2C master data.
SI2C_M_SCK	89	51	B4	I/O	-	SIF I2C master clock.
SEN_XSLEEP	90	52	A3	I/O	-	Sensor XSLEEP.
SEN_D7	91	53	-	I/O	-	Sensor Data Bit7.
SEN_D6	92	54	-	I/O	-	Sensor Data Bit6.
SEN_D5	93	55	-	I/O	-	Sensor Data Bit5.
DGND	94	-	-	G	Ground	Core GND.
SIF_IOGND	95	-	-	G	Ground	SIF IO GND.
SIF_IOVDD	96	56	B8	P	1.8V	SIF IO PWR.
SEN_D4	97	57	-	I/O	-	Sensor Data Bit4.
SEN_D3	98	58	-	I/O	-	Sensor Data Bit3.

Pin name	LQFP-128 Pin no.	QFN-72 Pin no.	WLCSP-38 Pin no.	Type	Pad	Description
SEN_D2	99	59	-	I/O	-	Sensor Data Bit2.
SEN_D1	100	60	-	I/O	-	Sensor Data Bit1.
SEN_D0	101	61	A5	I/O	-	Sensor Data Bit0.
SEN_LVALID	102	62	-	I/O	-	Sensor Line Valid.
SEN_FVALID	103	63	-	I/O	-	Sensor Frame Valid.
SEN_MCLK	104	64	B6	I/O	-	Sensor MCLK.
SEN_TRIG	105	65	-	I/O	-	Sensor Trigger.
SEN_CSW1	106	-	-	I/O	-	Sensor Content Switch1.
SEN_CSW0	107	66	-	I/O	-	Sensor Content Switch0.
SEN_FAE	108	67	-	I/O	-	Sensor Frame Auto Exposure.
SEN_PCLKO	109	68	A7	I/O	-	Sensor PCLK output.
SIF_IOVDD	110	69	B8	P	1.8V	SIF IO PWR.
SLDO_OUT	111	70	-	AO	-	SLDO 0.9V output.
DGND	112	-	-	G	Ground	Core GND.
FLASH_SI	113	-	A9	I/O	-	Flash SPI data in.
SIF_IOGND	114	-	B10	G	Ground	SIF IO GND.
FLASH_SCLK	115	-	A11	I/O	-	Flash SPI clock.
FLASH_HOLDN	116	-	-	I/O	-	Flash Data Hold.
SIF_IOGND	117	-	-	G	Ground	SIF IO GND.
FLASH_WPN	118	-	-	I/O	-	Flash Write Protect.
FLASH_VDD	119	71	-	P	1.8V	Flash PWR.
FLASH_SO	122	-	B12	I/O	-	Flash SPI data out.
FLASH_CSN	123	-	A13	I/O	-	Flash SPI chip select.
DGND	124	-	-	G	Ground	Core GND.
OTP_AVDD33	125	72	A15	P	3.3V	OTP 3.3V PWR.
DUMMY	120,121 126,127 128	-	-	-	DUMMY	Please let it floating. Don't connect any power or signal to dummy pin.

Table 4.1: Pin assignment

WLCSP-38 Ball Map

	A	B	C	D	E
1	SEN_INT	-	PGPIO9	-	UART1_TX
2	-	SI2C_M_SDA	-	PGPIO8	-
3	SEN_XSLEEP	-	SGPIO1	-	UART1_RX
4	-	SI2C_M_SCK	-	SLDO_OUT	-
5	SEN_D0	-	PIF_IOGND	-	SLDO_AVDD18
6	-	SEN_MCLK	-	PI2C_SLV_SCK	-
7	SEN_PCLKO	-	CLDO_OUT	-	PI2C_SLV_SDA
8	-	SIF_IOVDD	-	PGPIO3	-
9	FLASH_SI	-	PIF_IOVDD	-	PGPIO4
10	-	SIF_IOGND	-	BOOT_OPT1	-
11	FLASH_SCLK	-	BOOT_OPT0	-	BOOT_OPT2
12	-	FLASH_SO	-	TESTMODE	-
13	FLASH_CSN	-	CLDO_AVDD18	-	RESETN
14	-	PLL_VDD18	-	XTALOUT_24M	-
15	OTP_AVDD33	-	CLDO_OUT	-	XTALIN_24M

Table 4.2: WLCSP-38 ball map (Bottom view)

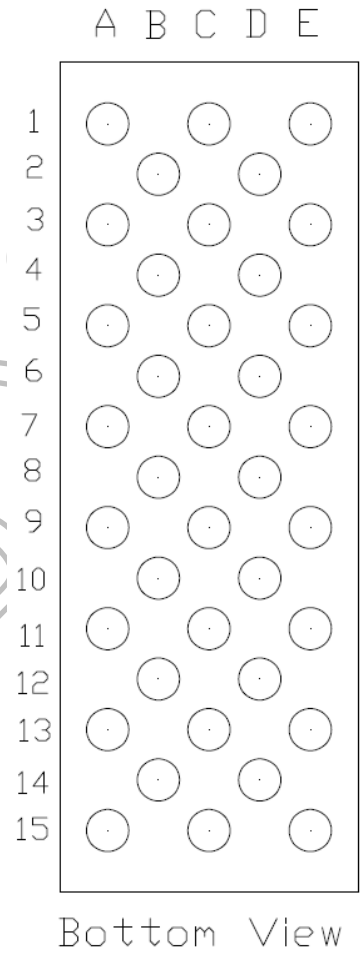


Figure 4.1: WLCSP-38 ball map (Bottom view)

5. Function Description

5.1 ARC EM9D DSP with FPU

5.1.1 Features

- XY multi-banked memory to improve MAC/cycle performance
- ARCv2DSP ISA adds over 100 DSP Instructions
- Support fixed point, vector and SIMD DSP processing
- Power-efficient unified 32x32 MUL/MAC unit
- 1.81 DMIPS/MHz and 4.02 CoreMark/MHz
- Includes Floating-Point Unit

5.1.2 Function description

The ARC EM9D DSP with FPU processor is optimized for DSP-intensive functions such as sensor fusion, object detection, voice detection, speech recognition and audio processing that are common in IoT and other embedded applications. Typical “always-on” applications such as those in the IoT market need low power consumption, optimized device performance and extended battery life.

The Floating-Point Unit provides hardware accelerated floating point calculation. The FPU becomes an integrated part of ARC EM9D execution pipeline with fully dependency checking and operand bypass capabilities. It supports single-precision operations only.

5.2 Image accelerators

5.2.1 Features

- Motion detection with de-noise pre-processing
- Crop function to select Region of Interest
- 2x2 down-scaling in vertical and horizontal
- 5x5 low pass filter or demosaic for Bayer image
- RGB to YUV converter
- JPEG encode and decode
- Histogram of Oriented Gradients extraction
- Programmable down-scaling

5.2.2 Function description

The image hardware accelerators provide image pre-processing function, and most used functions in feature extraction of Computer Vision algorithm. It can off-load ARC EM9D DSP and achieve higher “Vision” performance with low power consumption.

The Datapath flow control provides individual accelerator enable/disable control and various Datapath routing setting by programming. It includes DMA engines to transfer processed image data into system memory or get system memory data for hardware processing.

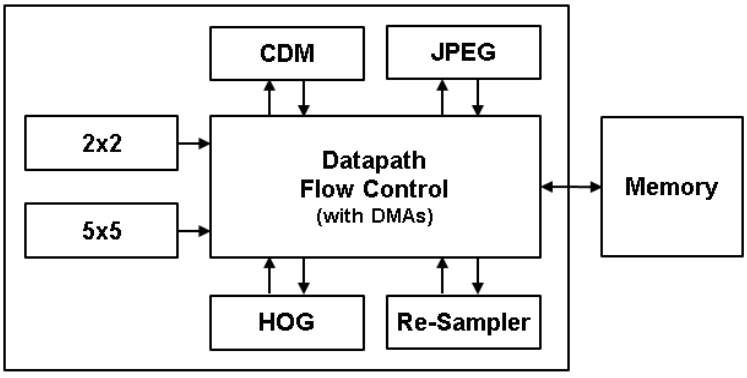


Figure 5.1: Image accelerators block diagram

5.3 Security

5.3.1 Features

- Secure boot
- Secure On-The-Air firmware update
- Secure meta data output over Transport Layer Security
- Secure key storage in OTP
- Support AES-128, SHA-256

5.3.2 Function description

HX6537-A provides complete security solution including signature authentication for the running firmware, firmware update and encrypted meta data output over TLS.

Secure boot is to prevent the loading of malicious or unauthorized firmware on the HX6537-A. Secure OTA provides the basis for secure firmware update, and validate by digital signature. Secure meta data output is to encrypt the output data over TLS to avoid eavesdropping.

5.3.3 Secure boot

The secure boot provides a secure foundation for customer firmware. HX6537-A embedded a secure boot rom to provides authentication, decryption, integrity validation, version and project-id checking and code protection for customer firmware on installation and boot/reset. Secure boot is configurable leveraging OTP to direct the secure boot loader based on the customer security requirements.

The secure boot flow chart is as below:

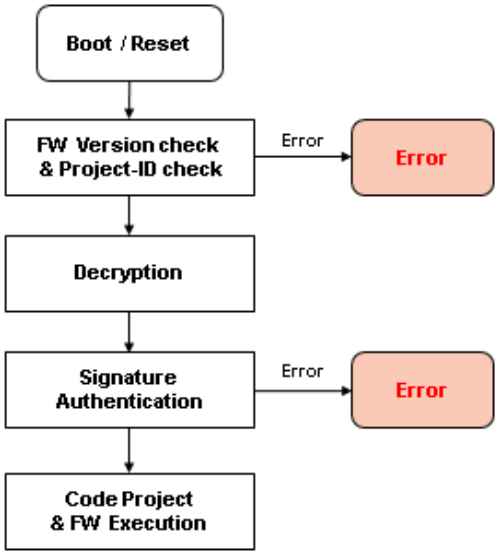


Figure 5.2: Secure boot flow

5.3.4 Secure OTA

The secure OTA is executed in HX6537-A firmware and loader. The secure OTA uploader provides the authentication, decryption, integrity validation, firmware version and project-id checking for customer firmware before upgrade firmware to flash memory. Customers can update firmware securely as directed via the security policy configuration in OTP.

The secure OTA flow chart is as below:

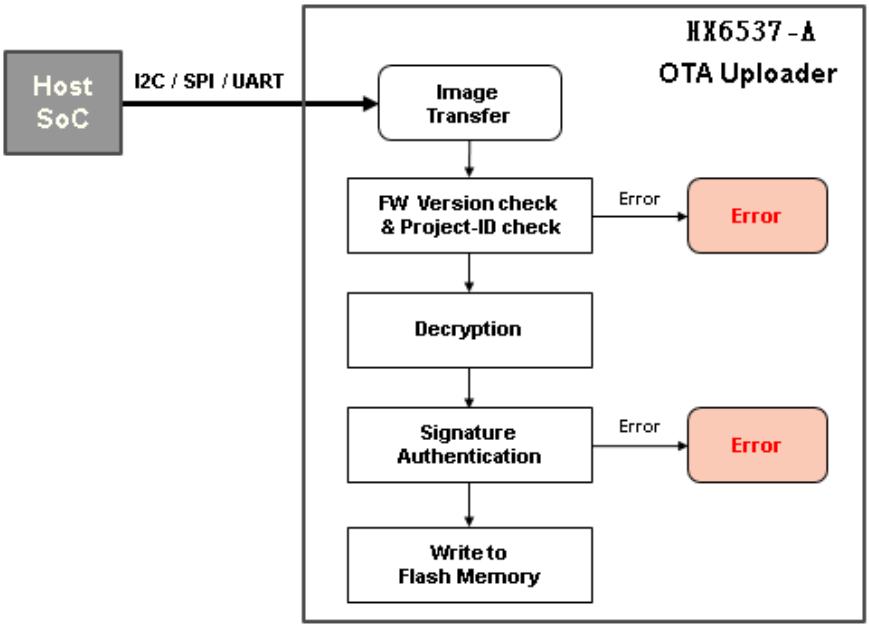


Figure 5.3: Secure OTA flow

5.3.5 Secure meta data output

The secure meta data output is using dynamic key communicating with Host processor over TLS. HX6537-A provides three TLS cipher suites which are:

- TLS_RSA_WITH_AES_128_GCM_SHA256
- TLS_ECDHE_ECDSA_WITH_AES_128_GCM_SHA256
- TLS_ECDHE_RSA_WITH_AES_128_GCM_SHA256

5.4 Power management

5.4.1 Features

- Power management – Active, Standby, Sleep and Shutdown modes
- Hardware power management when EM9D DSP is power is not active

5.4.2 Function description

HX6537-A supports a variety of power control features to achieve the best compromise between low-power consumption, short startup time and available wakeup sources.

The Power Management Unit is a hardware state machine that controls HX6537-A internal power domain switches on/off for power modes transitions. PMU supports various wake-up sources including external interrupts or internal timers interrupt for periodic wake-up in “always-on” applications.

5.4.3 Active mode

In active mode, the EM9D and all peripherals are powered up, clocks are active. EM9D can execute instructions to access selected peripherals for applications.

5.4.4 Standby mode

In standby mode, the EM9D is powered up, but clocks to EM9D are not active. Once system interrupt happens, the gated EM9D clock will be released immediately. EM9D become active and begin instruction execution process. For further information, see the *ARCv2 ISA Programmer’s Reference*.

5.4.5 Sleep mode

In sleep mode, EM9D is powered off, but EM9D local memories are in power retention state. When an interrupt triggers wake-up event, PMU will transit power mode to active mode. The startup time is short because all instruction and data is kept in local memory in sleep mode. There is no re-load programming and re-booting latency.

5.4.6 Shutdown mode

In shutdown mode, the main power is removed except PMU block. When an interrupt triggers wake-up event, PMU will transit power mode to active mode. EM9D will re-load program from Flash memory and re-booting before execute instruction.

6. Electrical Characteristics

6.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	ADC_AVDD18 PLL_VDD18 CLDO_AVDD18 POR_AVDD18 SLDO_AVDD18 SIF_IOVDD FLASH_VDD	-0.5	-	2.16	V
	PIF_IOVDD	-0.5	-	3.96	V
	OTP_AVDD33	-0.5	-	3.96	V
CMOS/TTL input voltage	V_{IN}	-0.5	-	IOVDD	V
CMOS/TTL output voltage	V_{OUT}	-0.5	-	IOVDD	V
Storage temperature	T_{STG}	-40	-	125	℃

Note: (1) Device will probably be damaged permanently in case that the stresses are over the absolute maximum ratings listed above.

6.2 Recommended operating conditions

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Supply voltage	ADC_AVDD18 PLL_VDD18 CLDO_AVDD18 POR_AVDD18 SLDO_AVDD18 SIF_IOVDD FLASH_VDD	1.7	1.8	1.9	V
	PIF_IOVDD	1.7	1.8 3.3	3.5	V
	OTP_AVDD33	3.1	3.3	3.5	V
Operating temperature	T_A	-10	25	85	℃
Junction temperature	T_J	-	-	90	℃

6.3 DC electrical characteristics

6.3.1 GPIO

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
High level input voltage	V_{IH}	-	0.7IOVDD	-	-	V
Low level input voltage	V_{IL}	-	-	-	0.3IOVDD	V
High level output voltage	V_{OH}	I_{OH}=-2mA	0.8IOVDD	-	-	V
Low level output voltage	V_{OL}	I_{OL}=2mA	-	-	0.3IOVDD	V

6.4 AC electrical characteristics

6.4.1 I²C Interface

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
SCL clock frequency(1)	f_{SCL}	Standard mode	0	-	100	kHz
		Fast mode	0	-	400	kHz
		Fast mode plus	0	-	1	MHz
Fall time(2)	t_f	Standard mode	-	-	300	ns
		Fast mode	-	-	300	ns
		Fast mode plus	-	-	120	ns
LOW period of SCL clock(2)	t_{LOW}	Standard mode	4.7	-	-	µs
		Fast mode	1.3	-	-	µs
		Fast mode plus	0.5	-	-	µs
HIGH period of SCL clock(2)	t_{HIGH}	Standard mode	4.0	-	-	µs
		Fast mode	0.6	-	-	µs
		Fast mode plus	0.26	-	-	µs
Data hold time(2)	$t_{HD;DAT}$	Standard mode	0	-	-	µs
		Fast mode	0	-	-	µs
		Fast mode plus	0	-	-	µs
Data setup time(2)	$T_{SU;DAT}$	Standard mode	250	-	-	ns
		Fast mode	100	-	-	ns
		Fast mode plus	50	-	-	ns

Note: (1) Guaranteed by characterization results. Not tested in production.
(2) Based on simulated values. Not tested in production.

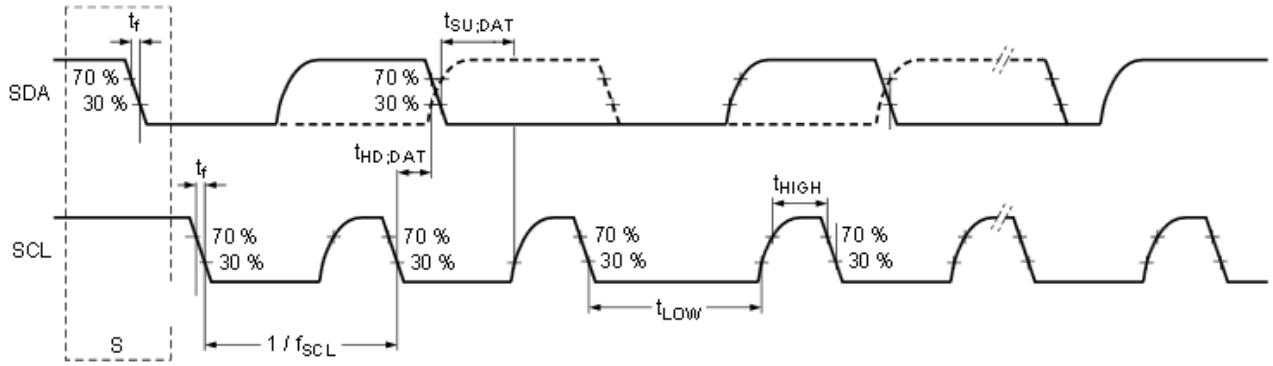


Figure 6.1: I²C timing

6.4.2 SPI interface

SPI master

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
SCK Clock cycle time(1)	$T_{cy(clk)}$	-	20	-	-	ns
Data setup time(2)	t_{DS}	-	0	-	-	ns
Data hold time(2)	t_{DH}	-	0	-	-	ns
Data output valid time(2)	$t_{v(Q)}$	-	0	-	5	ns

Note: (1) Guaranteed by characterization results. Not tested in production.
(2) Based on simulated values. Not tested in production.

SPI slave

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
SCK clock cycle time(1)	$T_{cy(clk)}$	-	20	-	-	ns
Data setup time(2)	t_{DS}	-	7	-	-	ns
Data hold time(2)	t_{DH}	-	0	-	-	ns
Data output valid time(2)	$t_{v(Q)}$	-	5	-	12	ns

Note: (1) Guaranteed by characterization results. Not tested in production.
(2) Based on simulated values. Not tested in production.

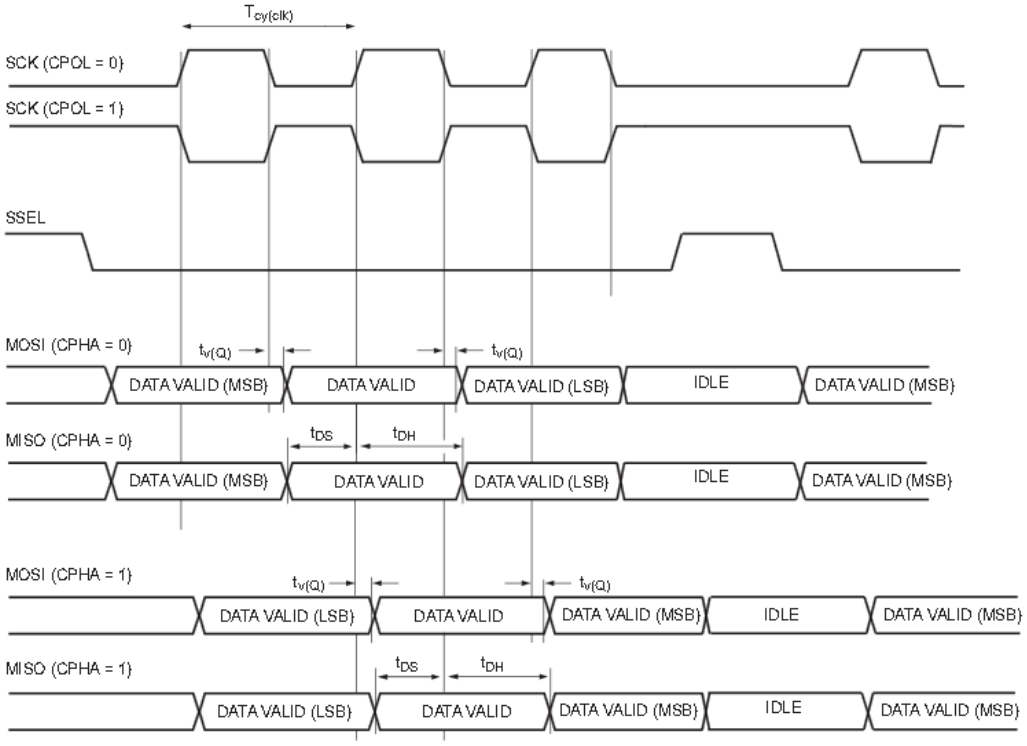


Figure 6.2: SPI master timing

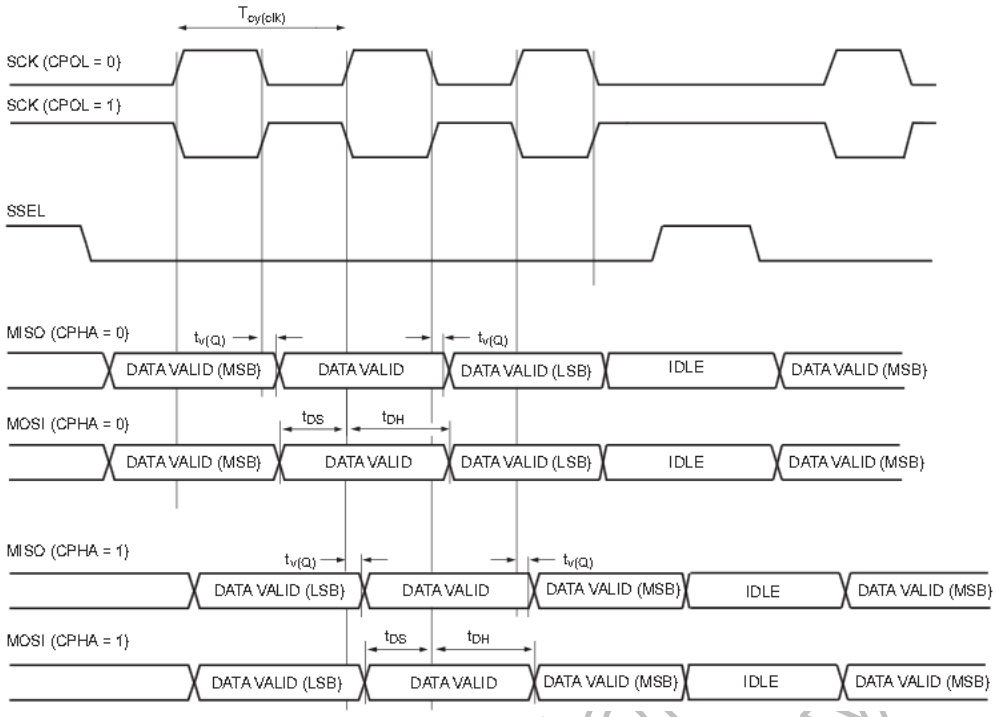


Figure 6.3: SPI slave timing

6.4.3 I²S RX/TX master interface AC characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Pulse width HIGH(1)	t_{WH}	-	163	-	1302	ns
Pulse width LOW(1)	t_{WL}	-	163	-	1302	ns
Data output valid time(2)	$t_{v(Q)}$	-	-	-	10	ns
Data input setup time(2)	$t_{su(D)}$	-	30	-	-	ns
Data input hold time(2)	$t_{h(D)}$	-	0	-	-	ns

Note: (1) Guaranteed by characterization results. Not tested in production.
(2) Based on simulated values. Not tested in production.

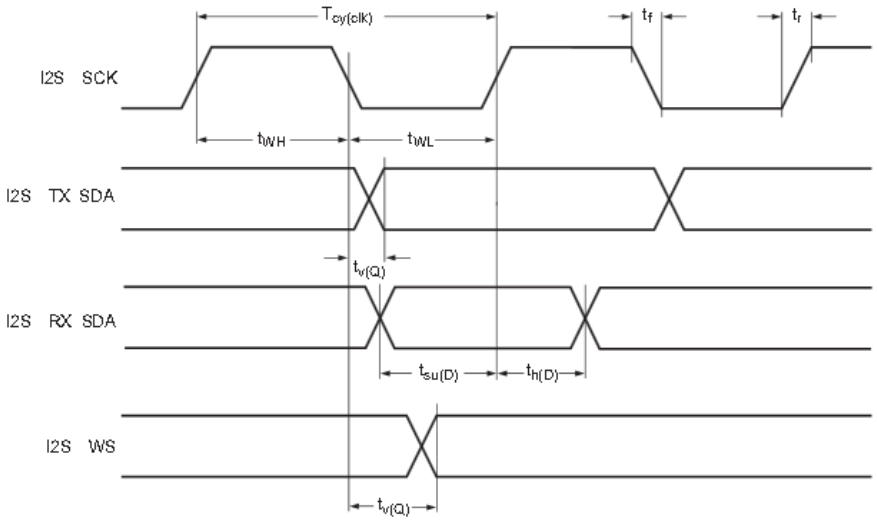


Figure 6.4: I²S RX/TX master timing

6.4.4 PDM RX Interface AC characteristics(1)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
PDM clock(1)	T_{CLK}	-	326	-	2604	ns
Data input setup time (R)(2)	T_{REN}	-	30	-	-	ns
Data input hold time (R)(2)	T_{RDIS}	-	5	-	23	ns
Data input setup time (L)(2)	T_{LEN}	-	30	-	-	ns
Data input hold time (L)(2)	T_{LDIS}	-	5	-	23	ns

Note: (1) Guaranteed by characterization results. Not tested in production.
(2) Based on simulated values. Not tested in production.

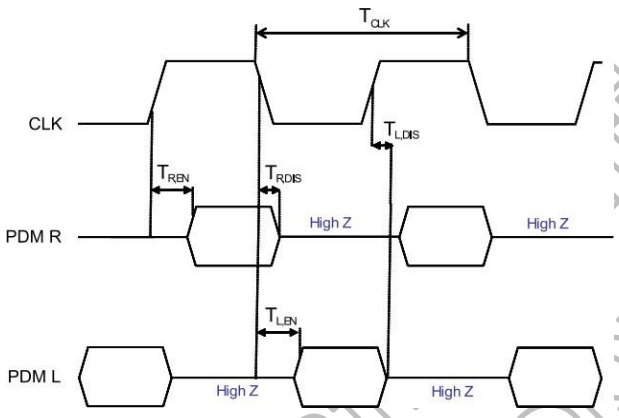


Figure 6.5: PDM Rx timing

6.4.5 Image sensor interface AC characteristics(1)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
PCLKO clock frequency(1)	F_{CLK}	-	-	-	75	MHz
Data input setup time(2)	T_{SU}	-	2	-	-	ns
Data input hold time(2)	T_{HD}	-	4	-	-	ns

Note: (1) Guaranteed by characterization results. Not tested in production.
(2) Based on simulated values. Not tested in production.

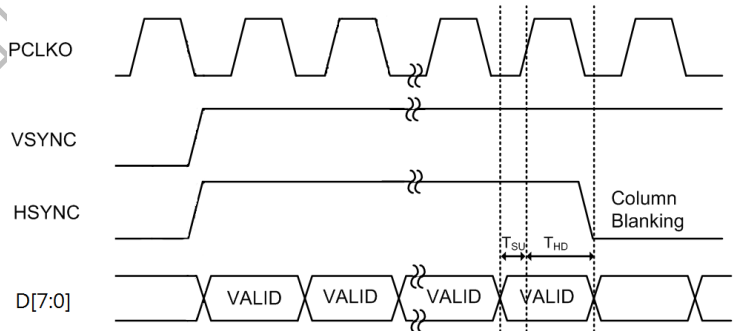


Figure 6.6: Image sensor interface timing

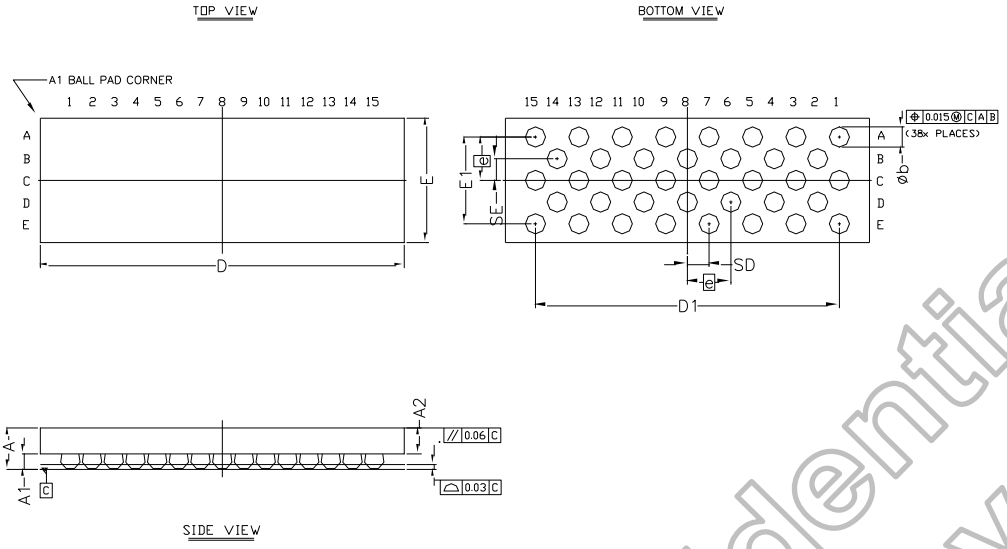
6.4.6 12-bit ADC characteristics(1)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Analog power supply	V_{DDA}	-	1.7	-	1.9	V
Positive reference voltage	V_{REF+}	-	0.95	-	1.05	V
Negative reference voltage	V_{REF-}	-	V_{ADC_AVSS18}			V
Analog input voltage	V_{ADCIN}	-	0	-	1	V
ADC clock frequency	F_{ADC}	-	-	-	1	MHz
Sampling rate	F_S	-	-	-	1	MSPS

Note: (1) Guaranteed by characterization results. Not tested in production.

7. Package Outline Dimension

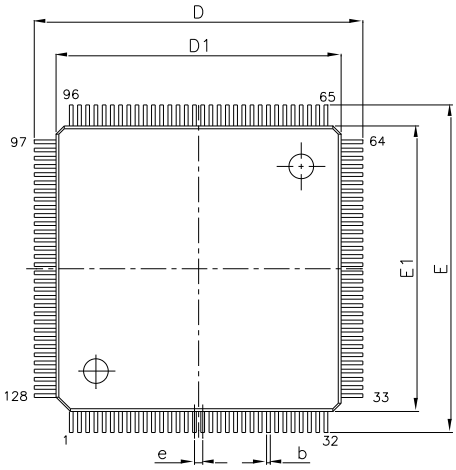
7.1 WLCSP-38

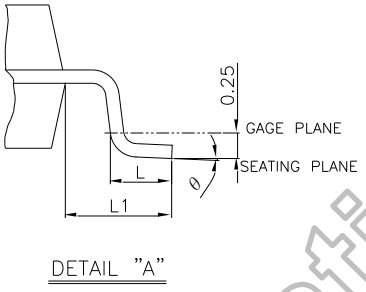


SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	0.505	0.535	0.565
A1	0.180	0.200	0.220
A2	0.315	0.335	0.355
Øb	0.240	0.260	0.280
D	4.675	4.695	4.750
D1	3.905	3.920	3.935
E	1.584	1.604	1.659
E1	1.105	1.120	1.135
e	0.545	0.560	0.575
SE	0.265	0.280	0.295
SD	0.265	0.280	0.295

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.

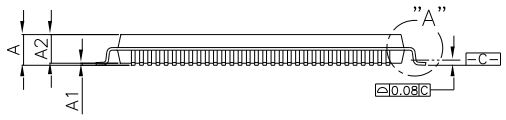
7.2 LQFP-128





Symbol	Min	Nom	Max
A	–	–	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
D	15.85	16.00	16.15
D1	13.90	14.00	14.10
E	15.85	16.00	16.15
E1	13.90	14.00	14.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

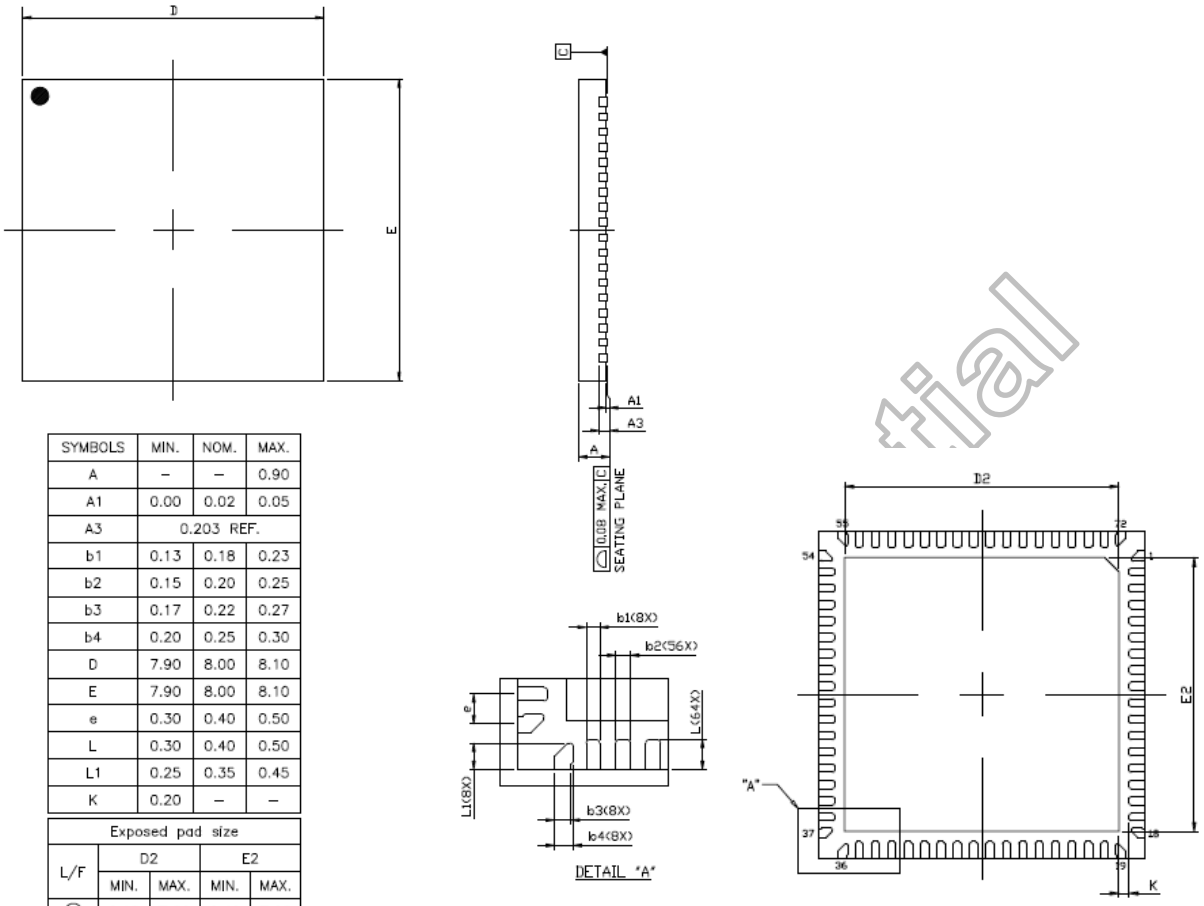
UNIT: MM



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS
   INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE
   TO THE LOWEST POINT OF THE PACKAGE BODY.
6. REFERENCE DOCUMENT : JEDEC MS-026.

7.3 QFN-72



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b1	0.13	0.18	0.23
b2	0.15	0.20	0.25
b3	0.17	0.22	0.27
b4	0.20	0.25	0.30
D	7.90	8.00	8.10
E	7.90	8.00	8.10
e	0.30	0.40	0.50
L	0.30	0.40	0.50
L1	0.25	0.35	0.45
K	0.20	–	–

Exposed pad size				
L/F	D2		E2	
	MIN.	MAX.	MIN.	MAX.
①	6.40	7.00	6.40	7.00

8. Ordering Information

Part no.	Package	Application	Description
HX6537-A01TWA	WLCSP-38	NB	No Flash
HX6537-A02TLBG	LQFP-128	AIoT	1 MB Flash
HX6537-A04TLDG	LQFP-128	AIoT	2 MB Flash
HX6537-A08TDHG	QFN-72	AIoT	1 MB Flash
HX6537-A09TDIG	QFN-72	AIoT	2 MB Flash