9-channel LED Driver

Bi−CMOS IC

LV5237JA

Overview

The LV5237JA is a 9−channel LED driver IC that is capable of switching between constant−current output and open drain output. Peak output current is I_O max = 100 mA. It enables 2−wire/3−wire serial bus control (address designation) to be set arbitrarily using an external pin. Also possible are 9−channel LED ON/OFF control and the setting of the PWM luminance in 256 steps.

Up to 81 driver ICs can be connected using the slave address setting pins.

Function

- 9−channel Output Constant−current LED Driver/Open Drain Output LED Driver (Selected by Using an External Pin) Supports Separate ON/OFF Setting for Each LED Output, High Withstand Voltage (VOUT < 42 V)
- In the Constant−current Mode (OUTSCT: L), the Reference Current is Set by the Value of Resistor Connected to the External Pin (RT1). Built−in D/A (5 Bits) for Switching Current Level …0.86 mA to 31.24 mA (RGB Drive) Constant Current (I_O max = 100 mA) for Full−color LEDs x 9 Channels
- In the Open Drain Mode (OUTSCT: H), High Current Drive (I_O max = 100 mA) x 9 Channels
- In the Constant−current Mode (OUTSCT: M) Only RGB3 is Open Drain (I_O max = 100 mA)
- Luminance Adjustment Using Internal PWM Control (256 Steps), It Copes with Independent PWM Control for Each LED Output
  - 8−bit PWM Luminance Dimming (0% to 99.6%)
  - 3−phase PWM
- Selection of 2−wire/3−wire Serial Bus Control Signals Enabled (Switching Using an External Pin)
  - Schmitt Trigger Input (3.3 V/5 V)
- Slave Addressing (4 Bits, Connection of Up to 81 Driver ICs Possible)
- Input Power Supply Supports 12 V
  - Internal Reference Output Terminal (5 V)
- Low Current Consumption
- Output Malfunction Protection Circuits (Thermal Protection Function, UVLO Detection Protection Function, Power on RESET)

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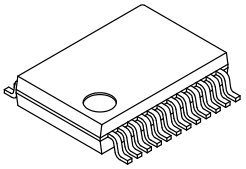
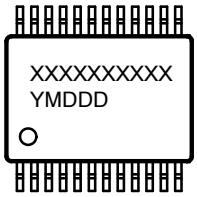


SSOP24 (225 mil)
CASE 565AR

MARKING DIAGRAM



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

ORDERING INFORMATION

Device	Package	Shipping
LV5237JAZ−AH	SSOP24 (225 mil) (Pb−Free / Halogen Free)	2000 / Tape & Reel

*For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Maximum Supply Voltage	V_{CC} max	SVCC	13.6	V
	VLED	VLED	42	V
	VREF	VREF	5.8	V
Output Voltage	V_O max	LED off	42	V
Output Current	I_O max	Open drain	100	mA
Allowable Power Dissipation	Pd max	Ta ≤ 25°C *	1.22	W
Operating Temperature	Topr		−25 to +85	°C
Storage Temperature	Tstg		−40 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Specified board: 114.3 mm x 76.1 mm x 1.6 mm, glass epoxy board. Exposed Die−pad area is not a substrate mounting.

WARNING: If you should intend to use this IC continuously under high temperature, high current, high voltage, or drastic temperature change, even if it is used within the range of absolute maximum ratings or operating conditions, there is a possibility of decrease reliability. Please contact us for a confirmation

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Operating Supply Voltage Range	V_{CC} op	SVCC	3.1 to 12.8	V
	V_{LED} op	VLED	3.1 to 42	V
	V_{REF} op	VREF	3.1 to 5.5	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

WARNING: The VLED terminal becomes the terminal for protection of the LED drive output. Please be connected to the power supply same as LED drive. When IC power supply (SVCC) and power supply of the LED or two kinds of power supply is more than it, please connect VLED to the highest potential and the power supply that it is.

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 5 V (= VREF))

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Consumption Current	$I_{CC}1$	LED off	1.0	1.8	2.9	mA
Reference Current Pin Voltage	VRT	RT1 = 20 kΩ	1.14	1.22	1.30	V
MAX Output Current	ΔIL	V_O = 0.7 to 4.0 V (Same channel line regulation)	−10	–	–	%
Between Bits Output Current	$\Delta I_O L$	I_O = 31.24 mA (Between bits pairing characteristics)	–	–	5	%
Maximum LED Driver Output Current 1	IMAX1	RT1 = 20 kΩ OUTSCT= L	29.36	31.24	33.12	mA
LED Output on Resistance 1	Ron1	I_O = 10 mA	–	10	20	Ω
OFF Leak Current	Ileak	LED OFF	–	–	10	μA
Power on RESET Voltage	VPOR	The voltage that is canceled	–	2.5	–	V
Reset Voltage	VRST	UVLO voltage	–	2.3	–	V
VREF Voltage	VREF	VREF = open	–	4.9	–	V
VREF Voltage	VREF1	V_{CC} = 6.0 V, I_O = 10 mA	4.7	5.1	5.4	V
Oscillator Frequency	Fosc		–	1.0	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Power on RESET

Reset all the data in the IC at the time of power activation. And it becomes the default setting.

**UVLO detection protection function

When SVCC decreases, it turns off LED output terminal.

***Thermal protection function

When a temperature in the IC rises, it turns off output terminal. When temperature falls, it returns by oneself.

CONTROL CIRCUIT (Ta = 25°C, V_{CC} = 5.0 V (= VREF))

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H Level 1	VH1	Input H level OUTSCT	4.5	–	5.0	V
M Level 1	VM1	Input M level OUTSCT	1.8	–	3.0	V
L Level 1	VL1	Input L level OUTSCT	−0.2	–	0.5	V
H Level 2	VH2	Input H level CTLSCT	3.5	–	5.0	V
L Level 2	VL2	Input L level CTLSCT	−0.2	–	0.5	V
H Level 3	VH3	Input H level SCLK, SDATA, SDEN	4.0	–	5.0	V
L Level 3	VL3	Input L level SCLK, SDATA, SDEN	−0.2	–	1.0	V
H Level 4	VH4	Input H level A0 to A3	4.5	–	5.0	V
M Level 4	VM4	Input M level A0 to A3	1.8	–	3.0	V
L Level 4	VL4	Input L level A0 to A3	−0.2	–	0.5	V

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 3.3 V (= VREF))

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Consumption Current	$I_{CC}2$	LED off	–	1.6	–	mA
Reference Current Pin Voltage	VRT	RT1 = 20 kΩ	1.14	1.22	1.30	V
MAX Output Current	ΔIL	V_O = 0.7 to 4.0 V (Same channel line regulation)	−10	–	–	%
Between Bits Output Current	$\Delta I_O L$	I_O = 31.24 mA (Between bits pairing characteristics)	–	–	5	%
Maximum LED Driver Output Current 1	IMAX1	RT1 = 20 kΩ OUTSCT= L	–	31.24	–	mA
LED Output on Resistance 1	Ron1	I_O = 10 mA	–	10	20	Ω
OFF Leak Current	Ileak	LED OFF	–	–	10	μA
Power on RESET Voltage	VPOR	The voltage that is canceled	–	2.5	–	V
Reset Voltage	VRST	UVLO voltage	–	2.3	–	V
VREF Voltage	VREF	VREF = open	–	3.2	–	V
Oscillator Frequency	Fosc		–	1.0	–	MHz

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

CONTROL CIRCUIT (Ta = 25°C, V_{CC} = 3.3 V (= VREF))

Parameter	Symbol	Condition	Min	Typ	Max	Unit
H Level 1	VH1	Input H level OUTSCT	2.8	–	3.3	V
M Level 1	VM1	Input M level OUTSCT	1.2	–	1.7	V
L Level 1	VL1	Input L level OUTSCT	−0.2	–	0.5	V
H Level 2	VH2	Input H level CTLSCT	2.3	–	3.3	V
L Level 2	VL2	Input L level CTLSCT	−0.2	–	0.5	V
H Level 3	VH3	Input H level SCLK, SDATA, SDEN	2.7	–	3.3	V
L Level 3	VL3	Input L level SCLK, SDATA, SDEN	−0.2	–	0.6	V
H Level 4	VH4	Input H level A0 to A3	2.8	–	3.3	V
M Level 4	VM4	Input M level A0 to A3	1.35	–	1.8	V
L Level 4	VL4	Input L level A0 to A3	−0.2	–	0.5	V

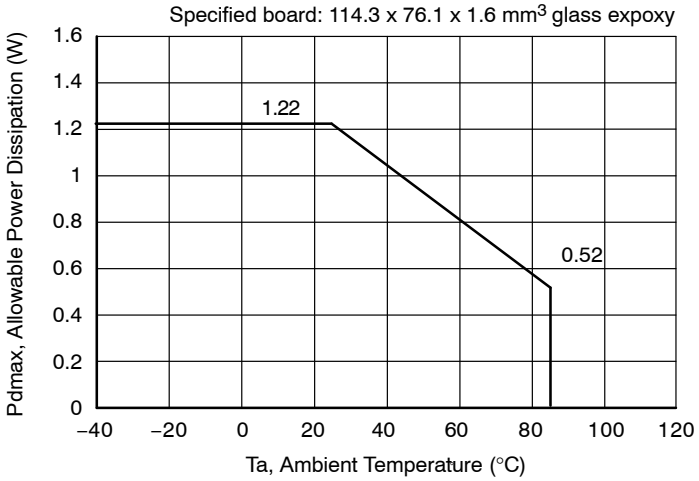
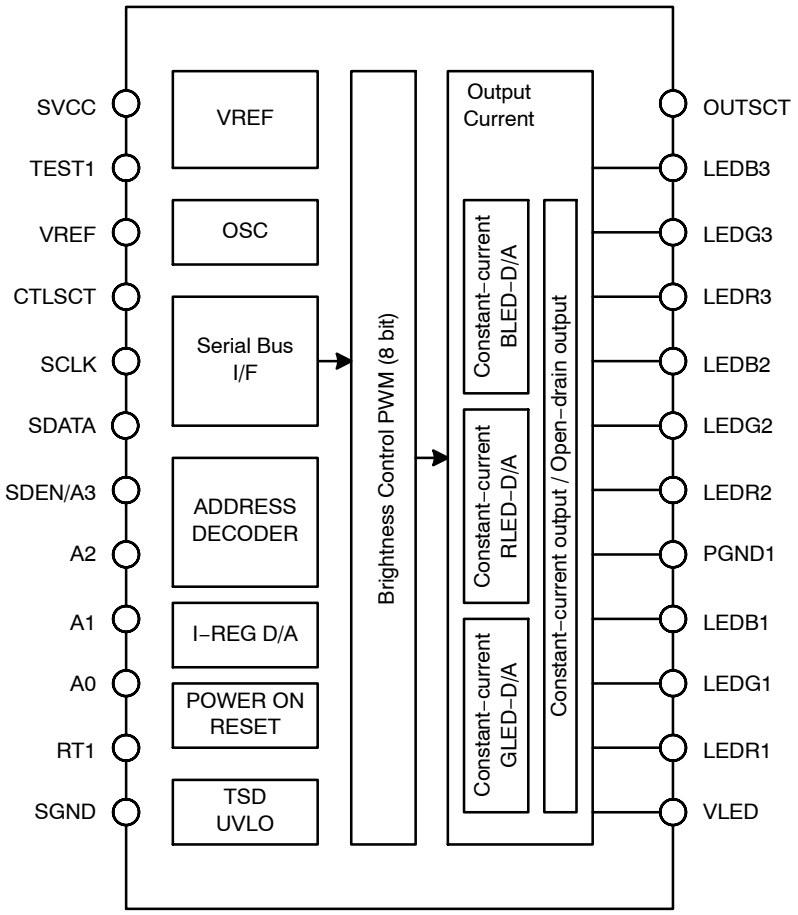


Figure 1. Pdmax – Ta

BLOCK DIAGRAM



WARNING: The VLED terminal becomes the terminal for protection of the LED drive output. Please be connected to the power supply same as LED drive.
When IC power supply (SVCC) and power supply of the LED or two kinds of power supply is more than it, please connect VLED to the highest potential and the power supply that it is.

Figure 2. Block Diagram

PIN ASSIGNMENT

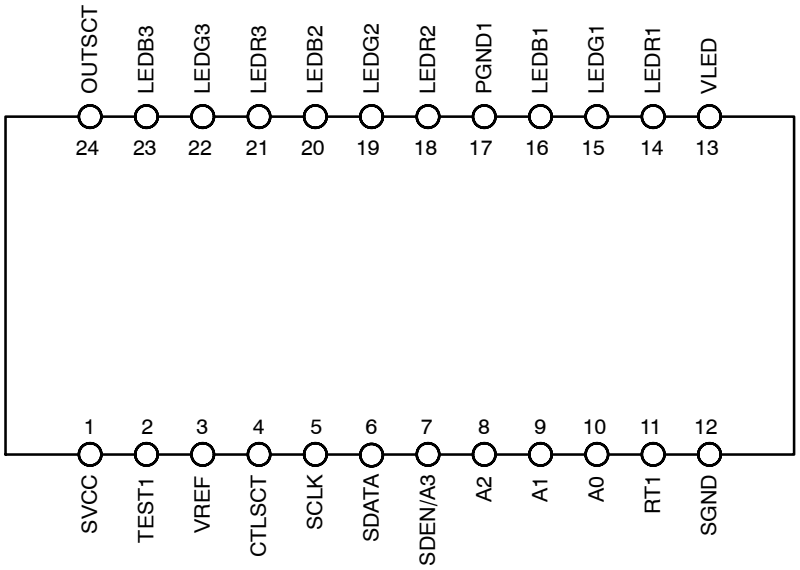


Figure 3. Pin Assignment

PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Description
1	SVCC	–	Power supply pin
2	TEST1	I	Test1 pin (connected to GND)
3	VREF	O	5 V reference output pin
4	CTLSCT	I	2−wire serial bus/3−wire serial bus selecting control pin (L: 3−wire serial, H: 2−wire serial)
5	SCLK	I	Serial clock signal input pin
6	SDATA	I	Serial data signal input pin
7	SDEN/A3	I	Serial enable signal input pin / Slave address input pin A3
8	A2	I	Slave address input pin A2
9	A1	I	Slave address input pin A1
10	A0	I	Slave address input pin A0
11	RT1	O	LED current setting resistor connection pin
12	SGND	–	Analog circuit GND pin
13	VLED	–	Output protection pin
14	LEDR1	O	LEDR1 output pin
15	LEDG1	O	LEDG1 output pin
16	LEDB1	O	LEDB1 output pin
17	PGND1	–	GND pin dedicated for LED driver
18	LEDR2	O	LEDR2 output pin
19	LEDG2	O	LEDG2 output pin
20	LEDB2	O	LEDB2 output pin
21	LEDR3	O	LEDR3 output pin
22	LEDG3	O	LEDG3 output pin
23	LEDB3	O	LEDB3 output pin
24	OUTSCT	I	Output type switching control pin L: Constant−current output M: Constant output, only RGB3 is open drain output H: Open drain output

OUTSCT SETTINGS

	LED Driver Output Pin	
OUTSCT Pin	LEDR1 / LEDR2 LEDG1 / LEDG2 LEDB1 / LEDB2	LEDR3 LEDG3 LEDB3
L	Constant current output Built−in current value switching D/A (5 bits) 0.86 mA to 31.24 mA, RT1 = 20 kΩ (f = 1 MHz)	Constant current output Built−in current value switching D/A (5 bits) 0.86 mA to 31.24 mA, RT1 = 20 kΩ (f = 1 MHz)
H	Open drain output Current value is determined by external limiting resistor. R_{ON} = 10 Ω	Open drain output Current value is determined by external limiting resistor. R_{ON} = 10 Ω
M	Constant current output Built−in current value switching D/A (5 bits) 0.86 mA to 31.24 mA, RT1 = 20 kΩ (f = 1 MHz)	Open drain output Current value is determined by external limiting resistor. R_{ON} = 10 Ω

Power on RESET Settings

It has power−on reset circuit built−in, and, at the time of power activation, the air register data of the IC is reset. It prevents malfunction of the LED lighting by letting you reset it.

When voltage rises from state of SVCC = 0 V, the power−on reset becomes effective. Please start to reboot it after making SVCC = 0 V.

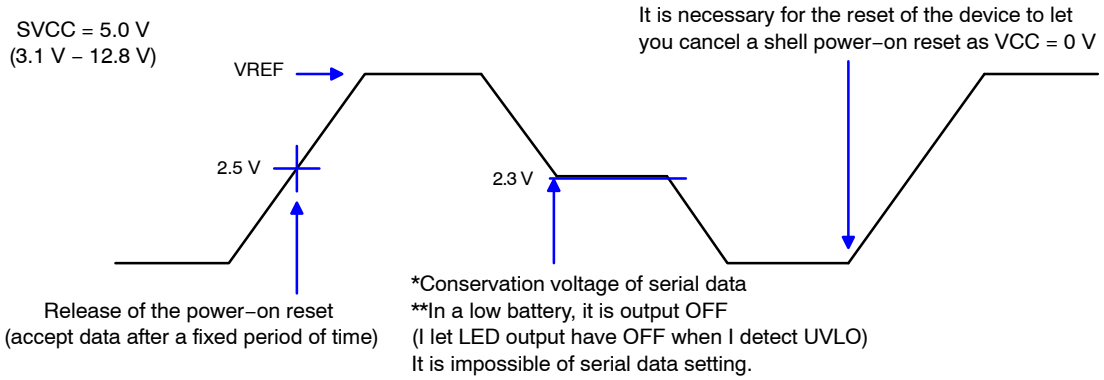
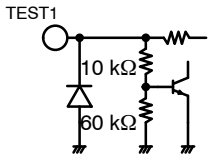
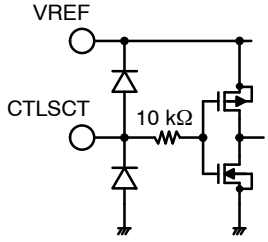
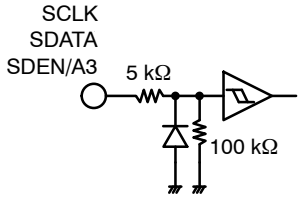
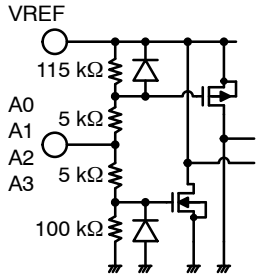
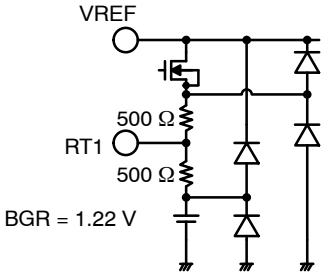
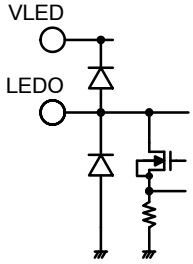
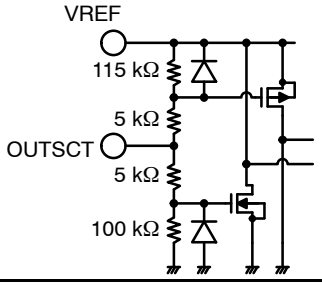


Figure 4.

PIN FUNCTIONS

Pin No.	Pin Name	Pin Function	Equivalent Circuit
1	SVCC	Power supply pin	
2	TEST1	Test1 pin This pin must always be connected to GND.	
3	VREF	Reference output pin (5 V)	
4	CTLSCT	Serial bus communication setting pin When set to low: The 3−wire serial bus signals are set as the input signals. When set to high: The 2−wire serial bus signals are set as the input signals.	

PIN FUNCTIONS (continued)

Pin No.	Pin Name	Pin Function	Equivalent Circuit
5 6 7	SCLK SDATA SDEN/A3	Serial clock signal input pin Serial data signal input pin Serial enable signal input pin / Slave address setting pin A3	
8 9 10	A2 A1 A0	Slave address setting pin A2 Slave address setting pin A1 Slave address setting pin A0	
11	RT1	Reference current setting resistor connection pin. By connecting the external register between this pin and GND, the reference current is generated. The pin voltage is approximately 1.22 V. By changing the current level, it is possible to change the LED driver current value (in the constant−current mode).	
12	SGND	GND pin	
13	VLED	Output protection pin	
14 15 16 18 19 20 21 22 23	LEDR1 LEDG1 LEDB1 LEDR2 LEDG2 LEDB2 LEDR3 LEDG3 LEDB3	LEDR1 output pin LEDG1 output pin LEDB1 output pin LEDR2 output pin LEDG2 output pin LEDB2 output pin LEDR3 output pin LEDG3 output pin LEDB3 output pin If these pins are not going to be used, they must always be connected to GND.	
17	PGND1	GND pin dedicate for LED output	
24	OUTSCT	LED driver output type setting pin When set to low: Constant−current output is set for the LED driver. When set to high: Open drain output is set for the LED driver. When set to middle: Constant−current output is set for the LED driver. However, open drain output is set for the only LED3 driver (LEDR3/G3/B3).	

SERIAL BUS COMMUNICATION SPECIFICATIONS

Serial Bus Transfer Timing Conditions

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Cycle Time	tcy1	SCLK clock period	200	–	–	ns
Data Setup Time	ts0	SDEN setup time relative to the rise of SCLK	90	–	–	ns
	ts1	SDATA setup time relative to the rise of SCLK	60	–	–	ns
Data Hold Time	th0	SDEN hold time relative to the rise of SCLK	200	–	–	ns
	th1	SDATA hold time relative to the rise of SCLK	60	–	–	ns
Pulse Width	tw1L	Low period pulse width of SCLK	90	–	–	ns
	tw1H	High period pulse width of SCLK	90	–	–	ns
	tw2L	Low period pulse width of SDEN	1	–	–	μs

3−wire Serial Bus Transfer Formats

LV5237JA receives the command by communication format by 3 line type serial communication of SCLK, SDATA, and SDEN.

When SCLK stops in “L” level

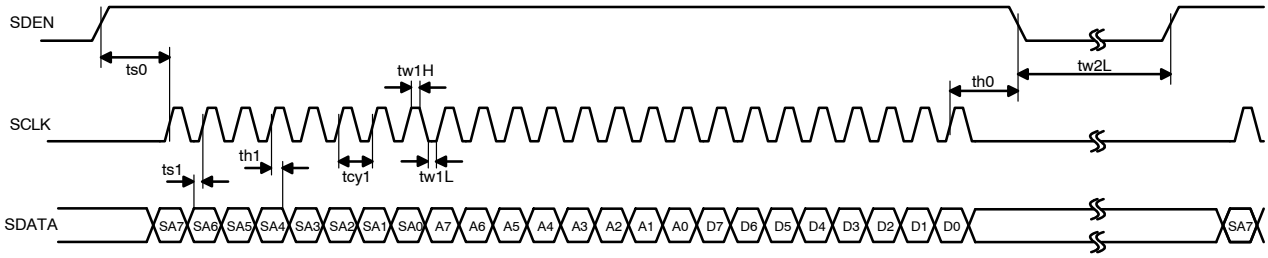


Figure 5.

When SCLK stops in “H” level

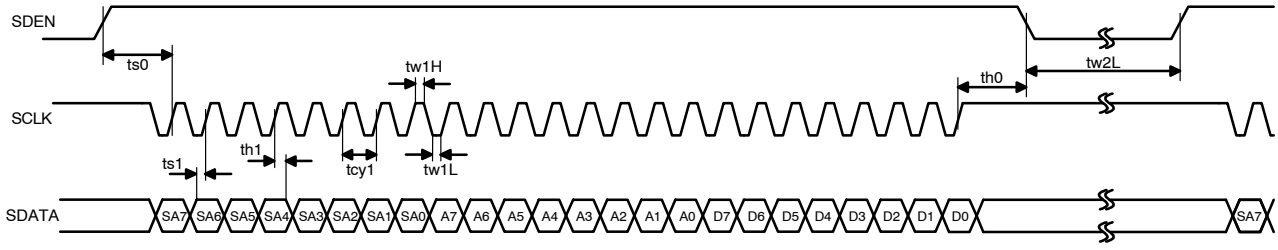


Figure 6.

Data length: 24 bits

Slave address (8 bits) + Register address (8 bits) + Data (8 bits)

Clock frequency: 5 MHz or less

When 24 SCLK clock signals have been input during the high period of SDEN, the SDATA is taken in at the rising edge of SCLK.

NOTE: If the number of SCLK clock signals during the high period of SDEN is 23 or less, SDATA is not taken in. If it is 25 or more, the register address is automatically incremented every time 1 byte is taken in.

Data Organization

The slave address is assigned by the first byte, and the register address on the serial map is specified by the next byte. The third byte transfers the data to the address specified by the register address that was written by the second byte and if the data subsequently continues even after this, the register address is automatically incremented for the fourth and subsequent bytes. As a result, it is possible to send the data continuously from the specified addresses. Data of less than one byte is ignored. However, when the address reaches 0fh, the next byte to be transferred becomes 00h.

Serial Data Transfer Example (Slave Address = 0000 001−)

When I set register address 02h and write in data (the smallest data length)

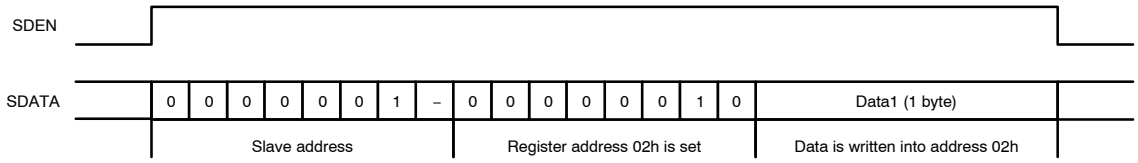


Figure 7.

When I set register address 02h and write in data for 3 bytes

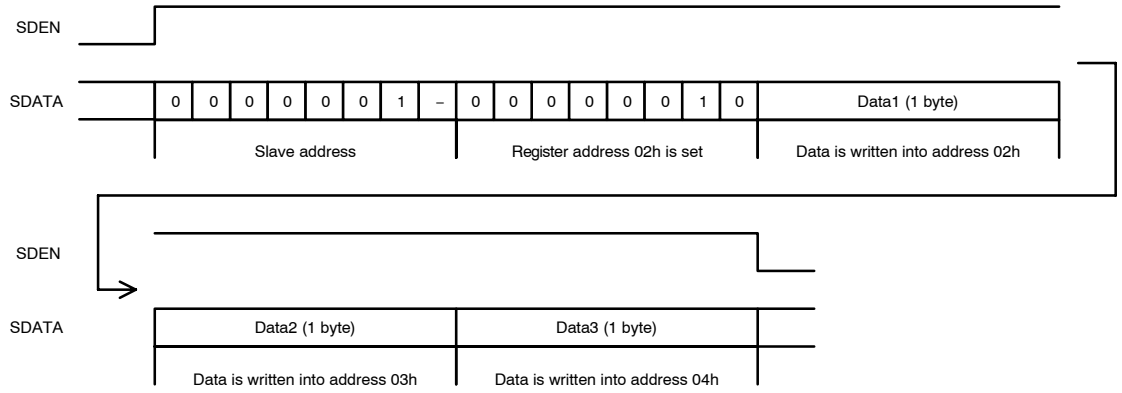


Figure 8.

When I set register address 02h and write in data for 3 byte, and following data is less than a signal byte

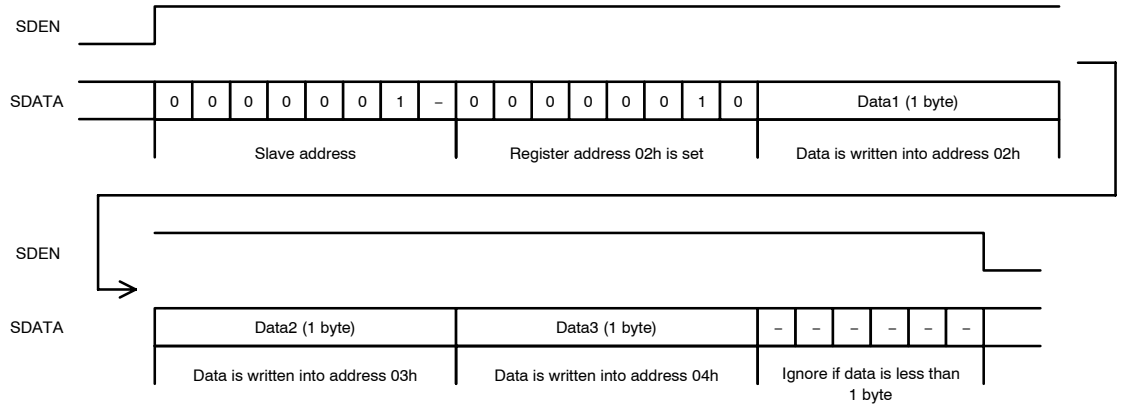


Figure 9.

When slave address does not accord

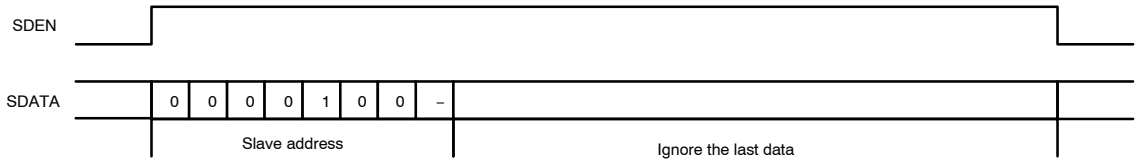


Figure 10.

2−wire Serial Bus Transfer Formats

LV5237JA receives the command by communication format by 2 line type serial communication of SCLK, SDATA.

When SCLK stops in “L” level

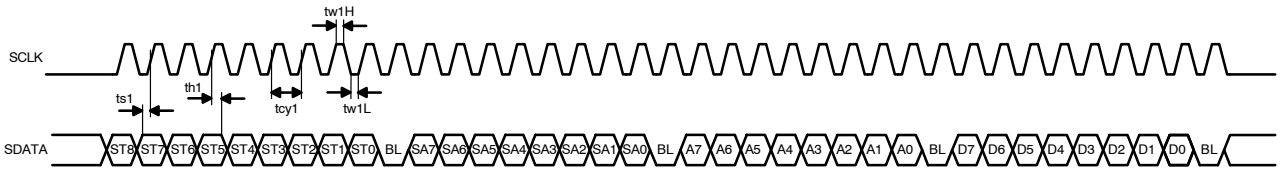


Figure 11.

When SCLK stops in “H” level

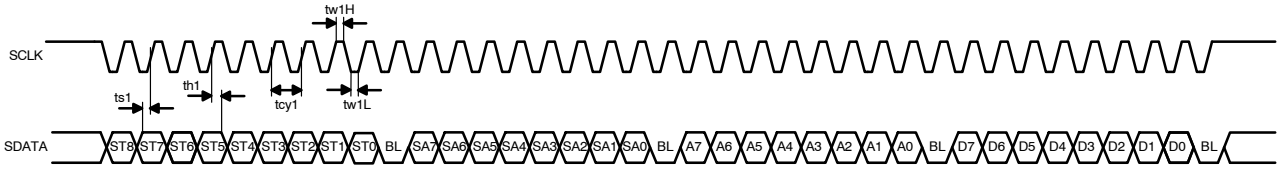


Figure 12.

Data length: 37 bits

Start condition (“111111111”) + BLANK (“0”) + Slave address (8 bits) + BLANK (“0”) + Register address (8 bits) + BLANK (“0”) + Data (8 bits) + BLANK (“0”)

Clock frequency: 5 MHz or less

After start detection, it takes SDATA in the timing when the 27th clock track of SCLK stands up when sign according to communication format is input into SCLK and SDATA.

NOTE: When SCLK is less than 27th clock track, and BLANK is different from communication format such as “1”, after start detection, do not take in SDATA.

When SCLK is higher than 28th clock track, start detection is confirmed, or it is automatic, and register address is incremented every 1 byte (8 bit) + BLANK (“0”) unless BLANL is “1”.

Data Organization

Table 2.

bit	ST8	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	BL	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	BL	A7	A6	A5	A4	A3	A2	A1	A0	BL	D7	D6	D5	D4	D3	D2	D1	D0	BL
SDATA	1	1	1	1	1	1	1	1	1	0	0	0						–	0									0									0
Parameter	Start condition									BLANK	Slave address								BLANK	Register address								BLANK	Data								BLANK

Even if SCLK and SDATA are state such as among standby or serial data inward correspondences, “111111111” start assumption and BLANK“0” start the uptake atomic act of new serial data after detection (start detection) was considered to be it.

After start detection, the first single byte (8 bit) is assigned to slave address, and a write store of the slave address completes it in BLANK“0”.

The next single byte appoints register address in the serial manufacturing auto protocol, and a write of the register address is completed in BLANK“0”.

The third byte performs a data transfer to the address which it appointed in the register address which it wrote in at the second byte and it complete data transfer in BLANK“0” and write in it. When data continues after this, register address is automatically incremented after the fourth byte and a data transfer is completed each time and, in BLANK“0”, writes in it.

Data Forward continuous from designated register address is enabled, but, as for the redirecting address of the next byte, it is in this way with for “00h” when register address becomes “0fh”.

In addition, when serial data uptake BLANK is “1”, including slave address selection and register address assignment, the single byte data just before it is ignored without being written in, and the subsequent data is ignored until it is detected a start.

Serial Data Transfer Example (Slave Address = 0000 001−)

When I set register address 02h and write in data (the smallest data length)

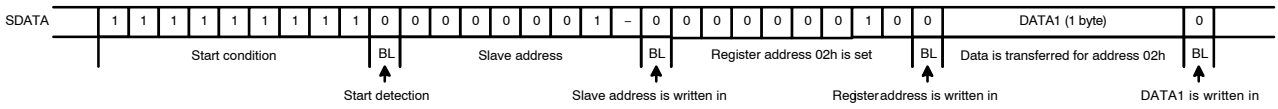


Figure 13.

When I set register address 02h and write in data for 3 bytes

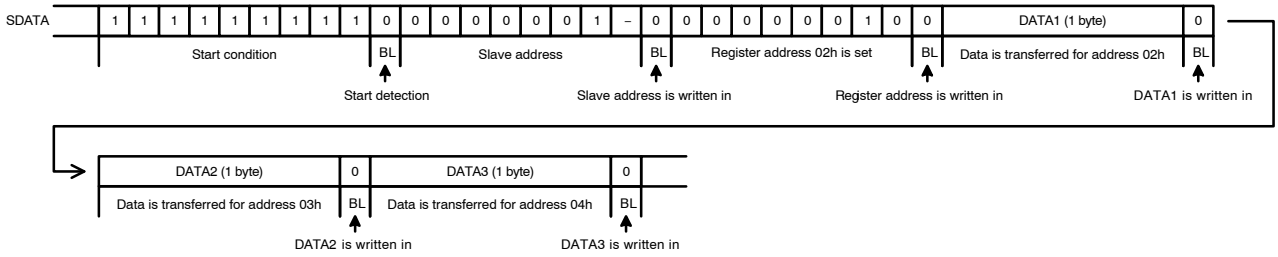


Figure 14.

When I set register address 02h and write in data for 1 byte, and BLANK after the following byte in the case of “1”

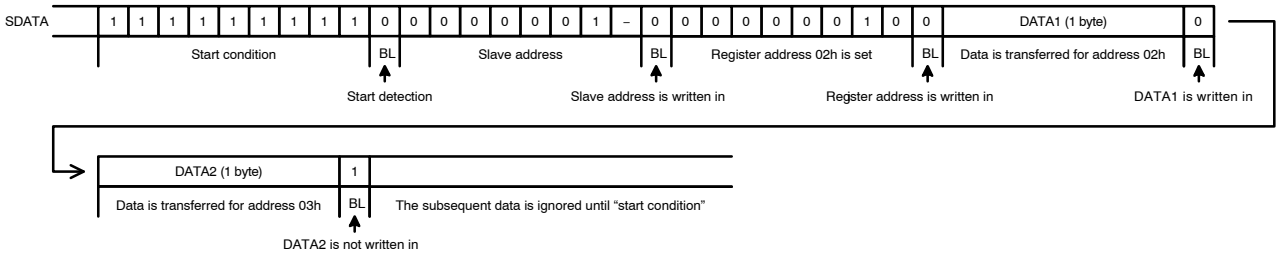


Figure 15.

When I set register address 02h, but BLANK after the byte in the case of “1”

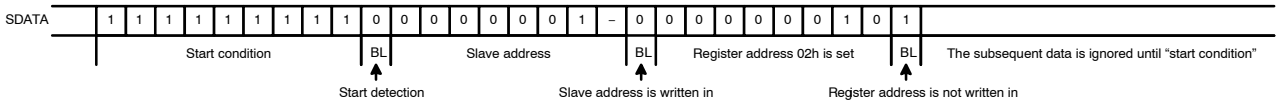


Figure 16.

When slave address does not accord

Figure 17.

SDATA continues more than 10 bit; and in the case of “1” (start detection of this case)

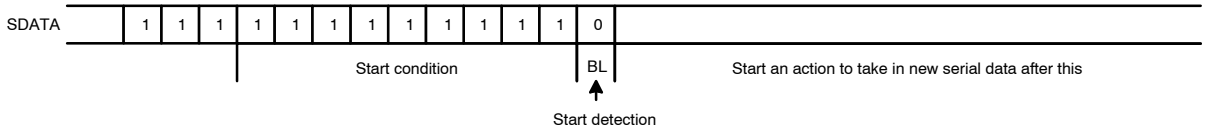


Figure 18.

Slave Address Condition

SLAVE ADDRESS CONDITION

	SLAVE ADDRESS							
	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Register Name	–	–	–	A3	A2	A1	A0	–
Default	0	0	0	0	0	0	0	–

Table 3.

Terminal PIN														LV5237
	A3	A2	A1	A0		SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
	L	L	L	L		0	0	0	0	0	0	0	–	1
	L	L	L	M		0	0	0	0	0	0	1	–	2
	L	L	L	H		0	0	0	0	0	1	0	–	3
	L	L	M	L		0	0	0	0	0	1	1	–	4
	L	L	M	M		0	0	0	0	1	0	0	–	5
	L	L	M	H		0	0	0	0	1	0	1	–	6
	L	L	H	L		0	0	0	0	1	1	0	–	7
	L	L	H	M		0	0	0	0	1	1	1	–	8
	L	L	H	H		0	0	0	1	0	0	0	–	9
	L	M	L	L		0	0	0	1	0	0	1	–	10
	L	M	L	M		0	0	0	1	0	1	0	–	11
	L	M	L	H		0	0	0	1	0	1	1	–	12
	L	M	M	L		0	0	0	1	1	0	0	–	13
	L	M	M	M		0	0	0	1	1	0	1	–	14
	L	M	M	H		0	0	0	1	1	1	0	–	15
	L	M	H	L		0	0	0	1	1	1	1	–	16
	L	M	H	M		0	0	1	0	0	0	0	–	17
	L	M	H	H		0	0	1	0	0	0	1	–	18
	L	H	L	L		0	0	1	0	0	1	0	–	19
	L	H	L	M		0	0	1	0	0	1	1	–	20
	L	H	L	H		0	0	1	0	1	0	0	–	21
	L	H	M	L		0	0	1	0	1	0	1	–	22
	L	H	M	M		0	0	1	0	1	1	0	–	23
	L	H	M	H		0	0	1	0	1	1	1	–	24
	L	H	H	L		0	0	1	1	0	0	0	–	25
	L	H	H	M		0	0	1	1	0	0	1	–	26
	L	H	H	H		0	0	1	1	0	1	0	–	27
	M	L	L	L		0	0	1	1	0	1	1	–	28
	M	L	L	M		0	0	1	1	1	0	0	–	29
	M	L	L	H		0	0	1	1	1	0	1	–	30
	M	L	M	L		0	0	1	1	1	1	0	–	31
	M	L	M	M		0	0	1	1	1	1	1	–	32
	M	L	M	H		0	1	0	0	0	0	0	–	33

Table 3. (continued)

Terminal PIN													LV5237
	A3	A2	A1	A0		SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
	M	L	H	L		0	1	0	0	0	0	1	–	34
	M	L	H	M		0	1	0	0	0	1	0	–	35
	M	L	H	H		0	1	0	0	0	1	1	–	36
	M	M	L	L		0	1	0	0	1	0	0	–	37
	M	M	L	M		0	1	0	0	1	0	1	–	38
	M	M	L	H		0	1	0	0	1	1	0	–	39
	M	M	M	L		0	1	0	0	1	1	1	–	40
	M	M	M	M		0	1	0	1	0	0	0	–	41
	M	M	M	H		0	1	0	1	0	0	1	–	42
	M	M	H	L		0	1	0	1	0	1	0	–	43
	M	M	H	M		0	1	0	1	0	1	1	–	44
	M	M	H	H		0	1	0	1	1	0	0	–	45
	M	H	L	L		0	1	0	1	1	0	1	–	46
	M	H	L	M		0	1	0	1	1	1	0	–	47
	M	H	L	H		0	1	0	1	1	1	1	–	48
	M	H	M	L		0	1	1	0	0	0	0	–	49
	M	H	M	M		0	1	1	0	0	0	1	–	50
	M	H	M	H		0	1	1	0	0	1	0	–	51
	M	H	H	L		0	1	1	0	0	1	1	–	52
	M	H	H	M		0	1	1	0	1	0	0	–	53
	M	H	H	H		0	1	1	0	1	0	1	–	54
	H	L	L	L		0	1	1	0	1	1	0	–	55
	H	L	L	M		0	1	1	0	1	1	1	–	56
	H	L	L	H		0	1	1	1	0	0	0	–	57
	H	L	M	L		0	1	1	1	0	0	1	–	58
	H	L	M	M		0	1	1	1	0	1	0	–	59
	H	L	M	H		0	1	1	1	0	1	1	–	60
	H	L	H	L		0	1	1	1	1	0	0	–	61
	H	L	H	M		0	1	1	1	1	0	1	–	62
	H	L	H	H		0	1	1	1	1	1	0	–	63
	H	M	L	L		0	1	1	1	1	1	1	–	64
	H	M	L	M		1	1	0	0	0	0	0	–	65
	H	M	L	H		1	1	0	0	0	0	1	–	66
	H	M	M	L		1	1	0	0	0	1	0	–	67
	H	M	M	M		1	1	0	0	0	1	1	–	68
	H	M	M	H		1	1	0	0	1	0	0	–	69
	H	M	H	L		1	1	0	0	1	0	1	–	70
	H	M	H	M		1	1	0	0	1	1	0	–	71
	H	M	H	H		1	1	0	0	1	1	1	–	72
	H	H	L	L		1	1	0	1	0	0	0	–	73
	H	H	L	M		1	1	0	1	0	0	1	–	74

Table 3. (continued)

Terminal PIN													LV5237
	A3	A2	A1	A0		SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
	H	H	L	H		1	1	0	1	0	1	0	–	75
	H	H	M	L		1	1	0	1	0	1	1	–	76
	H	H	M	M		1	1	0	1	1	0	0	–	77
	H	H	M	H		1	1	0	1	1	0	1	–	78
	H	H	H	L		1	1	0	1	1	1	0	–	79
	H	H	H	M		1	1	0	1	1	1	1	–	80
	H	H	H	H		1	1	1	0	0	0	0	–	81

Slave Address Condition

SLAVE ADDRESS CONDITION

	SLAVE ADDRESS							
	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Register Name	–	–	–	–	A2	A1	A0	–
Default	0	0	0	0	0	0	0	–

Table 4.

Terminal PIN														LV5237
		A2	A1	A0		SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0	
		L	L	L		0	0	0	0	0	0	0	–	1
		L	L	M		0	0	0	0	0	0	1	–	2
		L	L	H		0	0	0	0	0	1	0	–	3
		L	M	L		0	0	0	0	0	1	1	–	4
		L	M	M		0	0	0	0	1	0	0	–	5
		L	M	H		0	0	0	0	1	0	1	–	6
		L	H	L		0	0	0	0	1	1	0	–	7
		L	H	M		0	0	0	0	1	1	1	–	8
		L	H	H		0	0	0	1	0	0	0	–	9
		M	L	L		0	0	0	1	0	0	1	–	10
		M	L	M		0	0	0	1	0	1	0	–	11
		M	L	H		0	0	0	1	0	1	1	–	12
		M	M	L		0	0	0	1	1	0	0	–	13
		M	M	M		0	0	0	1	1	0	1	–	14
		M	M	H		0	0	0	1	1	1	0	–	15
		M	H	L		0	0	0	1	1	1	1	–	16
		M	H	M		0	0	1	0	0	0	0	–	17
		M	H	H		0	0	1	0	0	0	1	–	18
		H	L	L		0	0	1	0	0	1	0	–	19
		H	L	M		0	0	1	0	0	1	1	–	20
		H	L	H		0	0	1	0	1	0	0	–	21
		H	M	L		0	0	1	0	1	0	1	–	22
		H	M	M		0	0	1	0	1	1	0	–	23
		H	M	H		0	0	1	0	1	1	1	–	24
		H	H	L		0	0	1	1	0	0	0	–	25
		H	H	M		0	0	1	1	0	0	1	–	26
		H	H	H		0	0	1	1	0	1	0	–	27

Serial Each Mode Setting

ADDRESS: 00h

	ADDRESS: 00h							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Register Name	–	–	–	–	–	PWM[2]	PWM[1]	PWM[0]
Default	0	0	0	0	0	0	0	0

Table 5. PWM CYCLE SETTING (*Default)

D2	D1	D0	Time (ms)
0	0	0	0.5 *
0	0	1	1.0
0	1	0	2.0
0	1	1	4.0
1	0	0	8.0
–	–	–	–
–	–	–	–
–	–	–	–
–	–	–	–

ADDRESS: 01h

	ADDRESS: 01h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	R3OUT	R2OUT	R1OUT	RLED[4]	RLED[3]	RLED[2]	RLED[1]	RLED[0]
Default	0	0	0	0	0	0	0	0

Table 6. LEDR3 OUTPUT DUTY SETTING (*Default)

D7	R3OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 7. LEDR2 OUTPUT DUTY SETTING (*Default)

D6	R2OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 8. LEDR1 OUTPUT DUTY SETTING (*Default)

D5	R1OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 9. RLED CURRENT VALUE SETTING (* Default)

D4	D3	D2	D1	D0	Current Value (mA)
0	0	0	0	0	0.86 *
0	0	0	0	1	1.84
0	0	0	1	0	2.82
0	0	0	1	1	3.80
0	0	1	0	0	4.78
0	0	1	0	1	5.76
0	0	1	1	0	6.74
0	0	1	1	1	7.72
0	1	0	0	0	8.70
0	1	0	0	1	9.68
0	1	0	1	0	10.66
0	1	0	1	1	11.64
0	1	1	0	0	12.62
0	1	1	0	1	13.60
0	1	1	1	0	14.58
0	1	1	1	1	15.56
1	0	0	0	0	16.54
1	0	0	0	1	17.52
1	0	0	1	0	18.50
1	0	0	1	1	19.48
1	0	1	0	0	20.46
1	0	1	0	1	21.44
1	0	1	1	0	22.42
1	0	1	1	1	23.40
1	1	0	0	0	24.38
1	1	0	0	1	25.36
1	1	0	1	0	26.34
1	1	0	1	1	27.32
1	1	1	0	0	28.30
1	1	1	0	1	29.28
1	1	1	1	0	30.26
1	1	1	1	1	31.24

ADDRESS: 02h

	ADDRESS: 02h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	G3OUT	G2OUT	G1OUT	GLED[4]	GLED[3]	GLED[2]	GLED[1]	GLED[0]
Default	0	0	0	0	0	0	0	0

Table 10. LEDG3 OUTPUT DUTY SETTING (*Default)

D7	G3OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 11. LEDG2 OUTPUT DUTY SETTING (*Default)

D6	G2OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 12. LEDG1 OUTPUT DUTY SETTING (*Default)

D5	G1OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 13. GLED CURRENT VALUE SETTING (* Default)

D4	D3	D2	D1	D0	Current Value (mA)
0	0	0	0	0	0.86 *
0	0	0	0	1	1.84
0	0	0	1	0	2.82
0	0	0	1	1	3.80
0	0	1	0	0	4.78
0	0	1	0	1	5.76
0	0	1	1	0	6.74
0	0	1	1	1	7.72
0	1	0	0	0	8.70
0	1	0	0	1	9.68
0	1	0	1	0	10.66
0	1	0	1	1	11.64
0	1	1	0	0	12.62
0	1	1	0	1	13.60
0	1	1	1	0	14.58
0	1	1	1	1	15.56
1	0	0	0	0	16.54
1	0	0	0	1	17.52
1	0	0	1	0	18.50
1	0	0	1	1	19.48
1	0	1	0	0	20.46
1	0	1	0	1	21.44
1	0	1	1	0	22.42
1	0	1	1	1	23.40
1	1	0	0	0	24.38
1	1	0	0	1	25.36
1	1	0	1	0	26.34
1	1	0	1	1	27.32
1	1	1	0	0	28.30
1	1	1	0	1	29.28
1	1	1	1	0	30.26
1	1	1	1	1	31.24

ADDRESS: 03h

	ADDRESS: 03h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	B3OUT	B2OUT	B1OUT	BLED[4]	BLED[3]	BLED[2]	BLED[1]	BLED[0]
Default	0	0	0	0	0	0	0	0

Table 14. LEDB3 OUTPUT DUTY SETTING (*Default)

D7	B3OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 15. LEDB2 OUTPUT DUTY SETTING (*Default)

D6	B2OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 16. LEDB1 OUTPUT DUTY SETTING (*Default)

D5	B1OUT
0	PWM mode−Duty setting *
1	100%−Duty setting

Table 17. BLED CURRENT VALUE SETTING (* Default)

D4	D3	D2	D1	D0	Current Value (mA)
0	0	0	0	0	0.86 *
0	0	0	0	1	1.84
0	0	0	1	0	2.82
0	0	0	1	1	3.80
0	0	1	0	0	4.78
0	0	1	0	1	5.76
0	0	1	1	0	6.74
0	0	1	1	1	7.72
0	1	0	0	0	8.70
0	1	0	0	1	9.68
0	1	0	1	0	10.66
0	1	0	1	1	11.64
0	1	1	0	0	12.62
0	1	1	0	1	13.60
0	1	1	1	0	14.58
0	1	1	1	1	15.56
1	0	0	0	0	16.54
1	0	0	0	1	17.52
1	0	0	1	0	18.50
1	0	0	1	1	19.48
1	0	1	0	0	20.46
1	0	1	0	1	21.44
1	0	1	1	0	22.42
1	0	1	1	1	23.40
1	1	0	0	0	24.38
1	1	0	0	1	25.36
1	1	0	1	0	26.34
1	1	0	1	1	27.32
1	1	1	0	0	28.30
1	1	1	0	1	29.28
1	1	1	1	0	30.26
1	1	1	1	1	31.24

ADDRESS: 04h

	ADDRESS: 04h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	R1PWM[7]	R1PWM[6]	R1PWM[5]	R1PWM[4]	R1PWM[3]	R1PWM[2]	R1PWM[1]	R1PWM[0]
Default	0	0	0	0	0	0	0	0

Table 18. LEDR1 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{R1PWM[7 : 0]}}{256} \quad \text{(eq. 1)}$$

ADDRESS: 05h

	ADDRESS: 05h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	G1PWM[7]	G1PWM[6]	G1PWM[5]	G1PWM[4]	G1PWM[3]	G1PWM[2]	G1PWM[1]	G1PWM[0]
Default	0	0	0	0	0	0	0	0

Table 19. LEDG1 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{G1PWM[7 : 0]}}{256} \quad \text{(eq. 2)}$$

ADDRESS: 06h

	ADDRESS: 06h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	B1PWM[7]	B1PWM[6]	B1PWM[5]	B1PWM[4]	B1PWM[3]	B1PWM[2]	B1PWM[1]	B1PWM[0]
Default	0	0	0	0	0	0	0	0

Table 20. LEDB1 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{B1PWM[7 : 0]}}{256} \quad \text{(eq. 3)}$$

ADDRESS: 07h

	ADDRESS: 07h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	R2PWM[7]	R2PWM[6]	R2PWM[5]	R2PWM[4]	R2PWM[3]	R2PWM[2]	R2PWM[1]	R2PWM[0]
Default	0	0	0	0	0	0	0	0

Table 21. LEDR2 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{R2PWM[7 : 0]}}{256} \quad \text{(eq. 4)}$$

ADDRESS: 08h

	ADDRESS: 08h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	G2PWM[7]	G2PWM[6]	G2PWM[5]	G2PWM[4]	G2PWM[3]	G2PWM[2]	G2PWM[1]	G2PWM[0]
Default	0	0	0	0	0	0	0	0

Table 22. LEDG2 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{G2PWM[7 : 0]}}{256} \quad \text{(eq. 5)}$$

ADDRESS: 09h

	ADDRESS: 09h							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	B2PWM[7]	B2PWM[6]	B2PWM[5]	B2PWM[4]	B2PWM[3]	B2PWM[2]	B2PWM[1]	B2PWM[0]
Default	0	0	0	0	0	0	0	0

Table 23. LEDB2 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{B2PWM[7 : 0]}}{256} \quad \text{(eq. 6)}$$

ADDRESS: 0ah

	ADDRESS: 0ah							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	R3PWM[7]	R3PWM[6]	R3PWM[5]	R3PWM[4]	R3PWM[3]	R3PWM[2]	R3PWM[1]	R3PWM[0]
Default	0	0	0	0	0	0	0	0

Table 24. LEDR3 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{R3PWM[7 : 0]}}{256} \quad \text{(eq. 7)}$$

ADDRESS: 0bh

	ADDRESS: 0bh							
	D7	D6	D5	D4	D3	D2	D1	D0
Register Name	G3PWM[7]	G3PWM[6]	G3PWM[5]	G3PWM[4]	G3PWM[3]	G3PWM[2]	G3PWM[1]	G3PWM[0]
Default	0	0	0	0	0	0	0	0

Table 25. LEDG3 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{G3PWM[7 : 0]}}{256} \quad \text{(eq. 8)}$$

ADDRESS: 0ch

	ADDRESS: 0ch							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Register Name	B3PWM[7]	B3PWM[6]	B3PWM[5]	B3PWM[4]	B3PWM[3]	B3PWM[2]	B3PWM[1]	B3PWM[0]
Default	0	0	0	0	0	0	0	0

Table 26. LEDB3 PWM DUTY SETTING (Default ALL0)

D	Duty (%)
00h	0.0
ffh	99.6

$$\text{Duty (\%)} = \frac{\text{B3PWM[7 : 0]}}{256} \quad \text{(eq. 9)}$$

LV5237JA Serial Map

- Table upper row: Register name
  Table the lower: Default value

Table 27. LV5237JA SERIAL MAP

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
00h	0	0	0	0	0	0	0	0	x	x	x	x	x	PWM[2:0]		
									–	–	–	–	–	0	0	0
01h	0	0	0	0	0	0	0	1	R3OUT	R2OUT	R1OUT	RLED[4:0]				
									0	0	0	0	0	0	0	0
02h	0	0	0	0	0	0	1	0	G3OUT	G2OUT	G1OUT	GLED[4:0]				
									0	0	0	0	0	0	0	0
03h	0	0	0	0	0	0	1	1	B3OUT	B2OUT	B1OUT	BLED[4:0]				
									0	0	0	0	0	0	0	0
04h	0	0	0	0	0	1	0	0	R1PWM[7:0]							
									0	0	0	0	0	0	0	0
05h	0	0	0	0	0	1	0	1	G1PWM[7:0]							
									0	0	0	0	0	0	0	0
06h	0	0	0	0	0	1	1	0	B1PWM[7:0]							
									0	0	0	0	0	0	0	0
07h	0	0	0	0	0	1	1	1	R2PWM[7:0]							
									0	0	0	0	0	0	0	0
08h	0	0	0	0	1	0	0	0	G2PWM[7:0]							
									0	0	0	0	0	0	0	0
09h	0	0	0	0	1	0	0	1	B2PWM[7:0]							
									0	0	0	0	0	0	0	0
0ah	0	0	0	0	1	0	1	0	R3PWM[7:0]							
									0	0	0	0	0	0	0	0
0bh	0	0	0	0	1	0	1	1	G3PWM[7:0]							
									0	0	0	0	0	0	0	0
0ch	0	0	0	0	1	1	0	0	B3PWM[7:0]							
									0	0	0	0	0	0	0	0

MECHANICAL CASE OUTLINE
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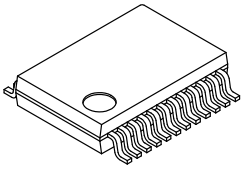
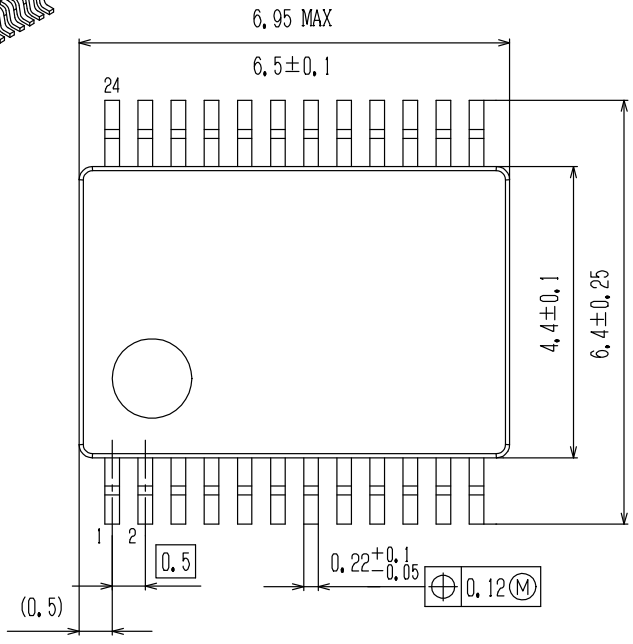
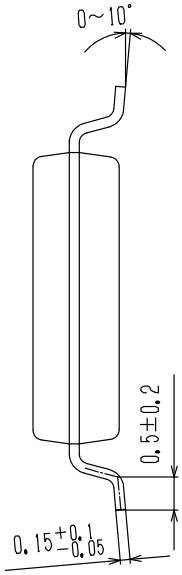
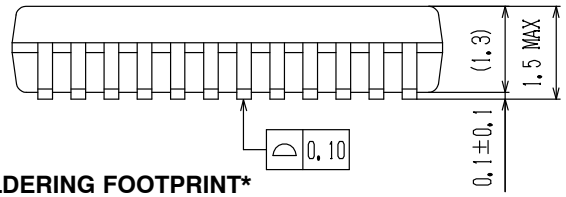
SSOP24 (225mil)
CASE 565AR
ISSUE A

DATE 23 OCT 2013

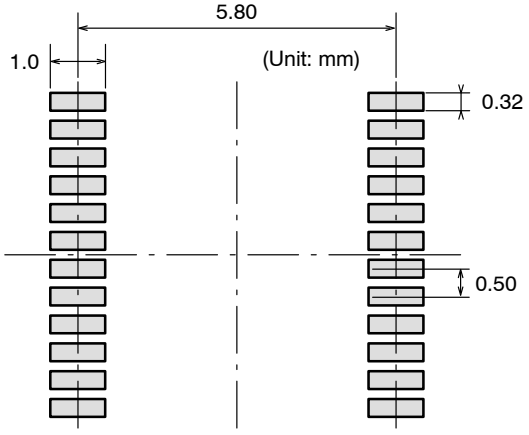








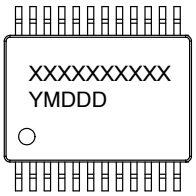
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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