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CY90F952JDS/F952MDS
CY90V950AJAS/V950AMAS

F²MC-16LX CY90950 Series 16-bit Microcontrollers

The CY90950-series with 2 FULL-CAN interfaces and Flash ROM is especially designed for automotive and other industrial applications. Its main feature are the on-board CAN Interfaces, which conform to V2.0 Part A and Part B, while supporting a very flexible message buffer scheme and so offering more functions than a normal FULL-CAN approach. With the new 0.18 µm CMOS technology, Cypress now offers on-chip Flash ROM program memory 256 Kbytes.

The power to the MCU core (1.8 V) is supplied by a built-in regulator circuit, giving these microcontrollers superior performance in terms of power consumption and tolerance to EMI.

Features

CPU

- Instruction system best suited to controller
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced functionality with signed multiply and divide instructions and the RETI instruction
  - Enhanced high-precision computing with 32-bit accumulator
- Instruction system compatible with high-level language (C language) and multitask
  - Employing system stack pointer
  - Various enhanced pointer indirect instructions
  - Barrel shift instructions
- Increased processing speed
  4-byte instruction queue

Serial interface

- UART (LIN/SCI): 7 channels
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available
- I²C interface: 2 channels
  Up to 400 kbps transfer rate

Interrupt controller

- Powerful 8-level, 34-condition interrupt feature
- Up to 16 external interrupts are supported
- Automatic data transfer function independent of CPU
  Expanded intelligent I/O service function (EI²OS): up to 16 channels
  DMA function: up to 16 channels

I/O ports

- General-purpose input/output port (CMOS output) : 82 ports

8/10-bit A/D converter: 24 channels

- Resolution is selectable between 8-bit and 10-bit.
- Activation by external trigger input is allowed.
- Conversion time: 3 µs (at 32-MHz machine clock, including sampling time)

8-bit D/A converter: 2 channels

Program patch function

Detects address matches against 6 address pointers

Timer

- Time-base timer, watch timer, watchdog timer: 1 channel
- 8/16-bit PPG timer: 8-bit×16 channels, or 16-bit×8 channels
- 16-bit reload timer: 4 channels
- 16-bit input/output timer
  - 16-bit free-run timer: 2 channels
  (FRT0: ICU 0/1/2/3, OCU 0/1/2/3, FRT1: ICU 4/5/6/7, OCU 4/5/6/7)
  - 16-bit input capture: (ICU): 8 channels
  - 16-bit output compare: (OCU): 8 channels

FULL-CAN controller

- 2 channels
- Compliant with Ver2.0A and Ver2.0B CAN specifications
- 16 built-in message buffers
- CAN wake-up function

Low power consumption (standby) mode

- Sleep mode (a mode that halts CPU operating clock)
- Timebase timer mode (a mode where only the oscillation clock, sub clock, timebase timer and watch timer operate)
- Watch mode (a mode that operates sub clock and clock timer only)
- Stop mode (a mode that stops oscillation clock and sub clock)
- CPU intermittent operation mode

Technology

0.18 µm CMOS technology

Contents

1. Product Lineup

Part Number / Parameter	CY90V950AJAS	CY90V950AMAS	CY90F952JDS	CY90F952MDS
Type	Evaluation products		Flash memory products	
CPU	F^2MC-16LX CPU			
System clock	On-chip PLL clock multiplier (×1, ×2, ×3, ×4, ×6, ×8, 1/2 when PLL stops) Minimum instruction execution time : 31.25 ns (4 MHz osc. PLL×8)			
ROM	External		Main 256 Kbytes Satellite 32 Kbytes	
RAM	30 Kbytes		16 Kbytes	
Emulator-specific power supply*1	Yes		—	
FPGA data*2	Rev 050617		—	
Adaptor board*2	CY2147-20 Rev.04C or later		—	
Clock supervisor	Yes	No	Yes	No
Clock calibration unit	Yes	No	Yes	No
Low-voltage/CPU operation detection reset	No (CPU operation detection reset only)	No	Yes	No
Technology	0.35 μm CMOS with built-in power supply regulator		0.18 μm CMOS with built-in power supply regulator + Flash memory with Charge pump for programming voltage	
Operating voltage range	5 V ± 10%		3.0 V to 5.5 V : When normal operating 4.0 V to 5.5 V : When Flash programming 4.5 V to 5.5 V : When using the external bus	
Operating ambient temperature	—		−40°C to +105°C	
Package	PGA-299		QFP-100, LQFP-100	
UART	7 channels			
	Wide range of baud rate settings using a dedicated reload timer Special synchronous options for adapting to different synchronous serial protocols LIN functionality working either as master or slave LIN device			
I^2C (400 kbps)	2 channels			
A/D Converter	24 input channels			
	10-bit or 8-bit resolution Conversion time : Min 3 μs include sample time (per one channel)			
16-bit Reload Timer (4 channels)	Operation clock frequency : fsys/2^1, fsys/2^3, fsys/2^5 (fsys = Machine clock frequency) Supports External Event Count function			
16-bit I/O Timer (2 channels)	Generates an interrupt signal on overflow Supports Timer Clear when the output compare finds a match Operation clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4, fsys/2^5, fsys/2^6, fsys/2^7 (fsys = Machine clock freq.) I/O Timer 0 (clock input FRCK0) corresponds to ICU0/1/2/3, OCU 0/1/2/3 I/O Timer 1 (clock input FRCK1) corresponds to ICU4/5/6/7, OCU 4/5/6/7			
16-bit Output Compare (8 channels)	Generates an interrupt signal when one of the 16-bit I/O timer matches the output compare register A pair of compare registers can be used to generate an output signal.			
16-bit Input Capture (8 channels)	Holds free-run timer on rising edge, falling edge or rising & falling edge Signals an interrupt upon external event			

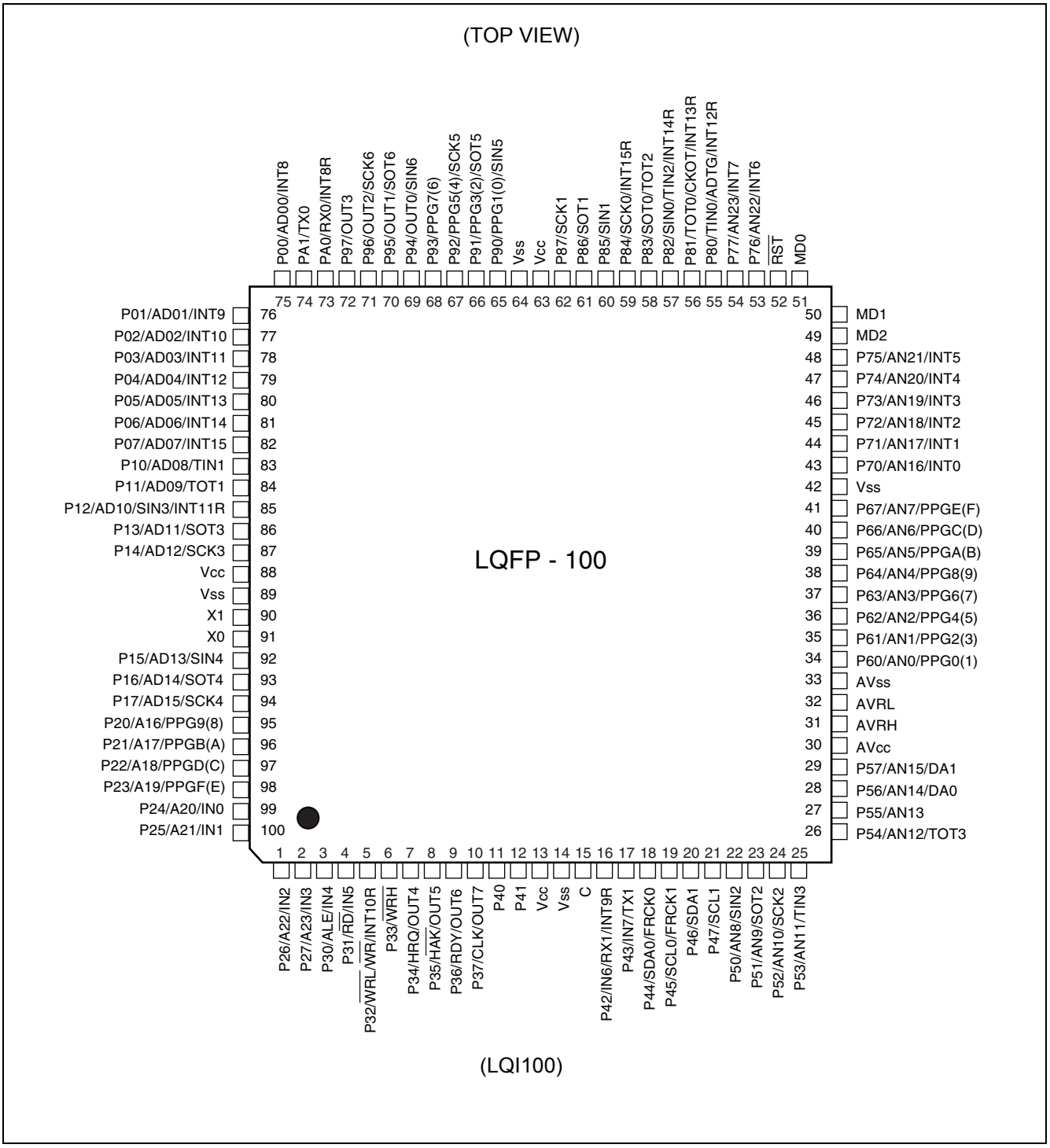
Part Number / Parameter	CY90V950AJAS	CY90V950AMAS	CY90F952JDS	CY90F952MDS
8/16-bit Programmable Pulse Generator	8 channels (16-bit) /16 channels (8-bit) Sixteen 8-bit reload counters Sixteen 8-bit reload registers for L pulse width Sixteen 8-bit reload registers for H pulse width Supports 8-bit and 16-bit operation modes A pair of 8-bit reload counters can be configured as one 16-bit reload counter or as 8-bit prescaler plus 8-bit reload counter Operating clock freq. : fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 or 128 μs@fosc = 4 MHz (fsys = Machine clock frequency, fosc = Oscillation clock frequency)			
CAN Interface	3 channels		2 channels	
	Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission in response to Remote Frames Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering : Full bit compare/Full bit mask/Two partial bit masks Supports up to 1 Mbps			
External Interrupt (16 channels)	Can be used rising edge, falling edge, starting up by H/L level input, external interrupt, expanded intelligent I/O services (EI^{2}OS) and DMA			
D/A converter	2 channels			
Sub clock	Yes	No	Yes	No
I/O Ports	Virtually all external pins can be used as general purpose I/O port All ports are push-pull outputs Bit-wise settable as input/output or peripheral signal Can be configured 8 as CMOS schmitt trigger/ automotive inputs (in blocks of 8 pins) TTL input level settable for external bus (32-pin only for external bus)			
Flash Memory	–		Supports automatic programming, Embedded Algorithm Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Security Feature for protecting the content of the Flash	

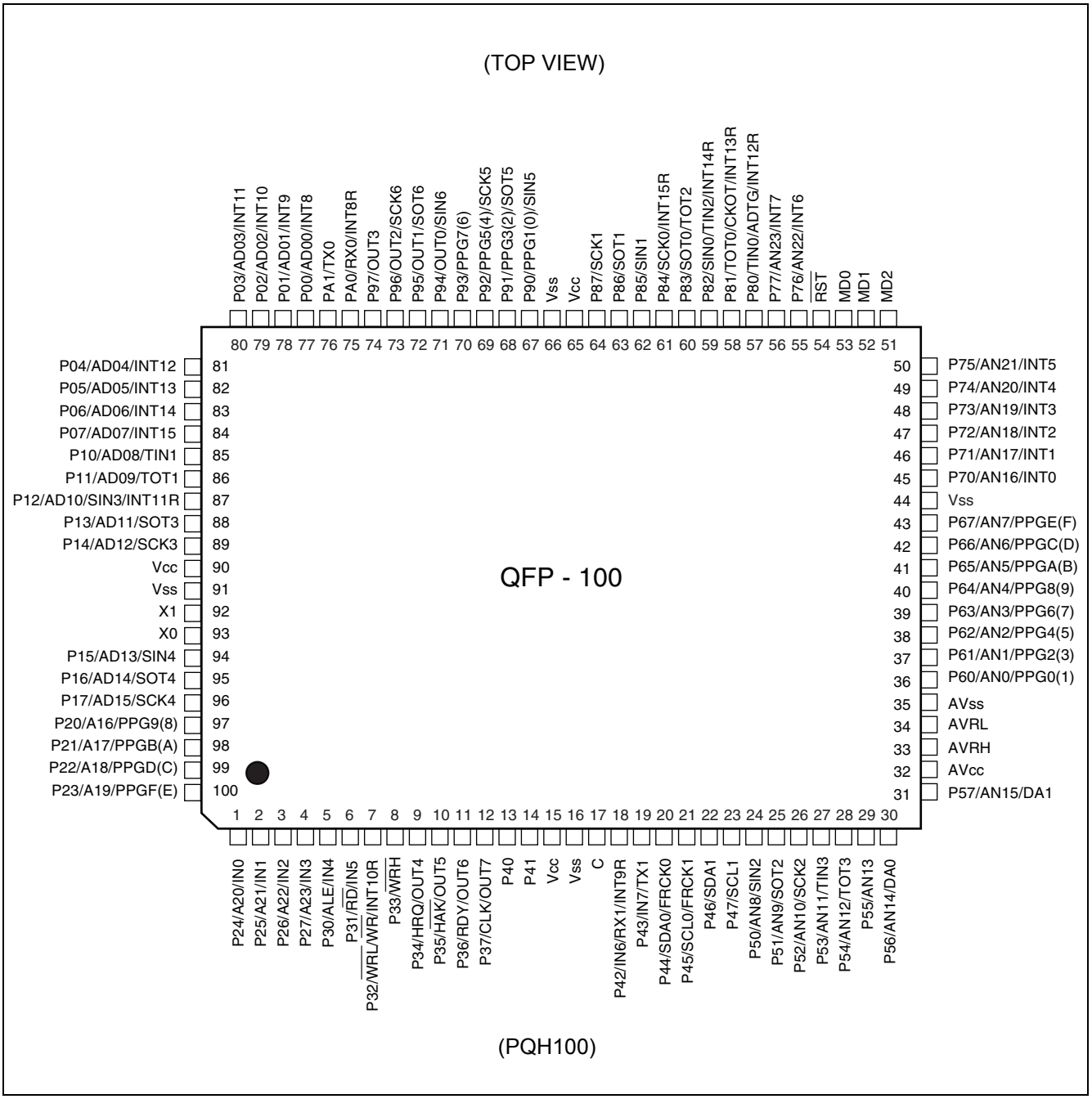
*1 : It is setting of Jumper switch (TOOL VCC) when Emulator (CY2147-01) is used.
Please refer to the Emulator hardware manual for details.

*2 : Customers considering the use of other FPGA data and the adaptor boards should consult with sales representatives.

2. Pin Assignments

■ CY90F952JDS, CY90F952MDS




(TOP VIEW)
P03/AD03/INT11 80
P02/AD02/INT10 79
P01/AD01/INT9 78
P00/AD00/INT8 77
PA1/TX0 76
PA0/RX0/INT8R 75
P97/OUT3 74
P96/OUT2/SCK6 73
P95/OUT1/SOT6 72
P94/OUT0/SIN6 71
P93/PPG7(6) 70
P92/PPG5(4)/SCK5 69
P91/PPG3(2)/SOT5 68
P90/PPG1(0)/SIN5 67
Vss 66
Vcc 65
P87/SCK1 64
P86/SOT1 63
P85/SIN1 62
P84/SCK0/INT15R 61
P83/SOT0/TOT2 60
P82/SIN0/TIN2/INT14R 59
P81/TOT0/CKOT/INT13R 58
P80/TIN0/ADTG/INT12R 57
P77/AN23/INT7 56
P76/AN22/INT6 55
RST 54
MD0 53
MD1 52
MD2 51
P04/AD04/INT12 81
P05/AD05/INT13 82
P06/AD06/INT14 83
P07/AD07/INT15 84
P10/AD08/TIN1 85
P11/AD09/TOT1 86
P12/AD10/SIN3/INT11R 87
P13/AD11/SOT3 88
P14/AD12/SCK3 89
Vcc 90
Vss 91
X1 92
X0 93
P15/AD13/SIN4 94
P16/AD14/SOT4 95
P17/AD15/SCK4 96
P20/A16/PPG9(8) 97
P21/A17/PPGB(A) 98
P22/A18/PPGD(C) 99
P23/A19/PPGF(E) 100
QFP - 100
50 P75/AN21/INT5
49 P74/AN20/INT4
48 P73/AN19/INT3
47 P72/AN18/INT2
46 P71/AN17/INT1
45 P70/AN16/INT0
44 Vss
43 P67/AN7/PPGE(F)
42 P66/AN6/PPGC(D)
41 P65/AN5/PPGA(B)
40 P64/AN4/PPG8(9)
39 P63/AN3/PPG6(7)
38 P62/AN2/PPG4(5)
37 P61/AN1/PPG2(3)
36 P60/AN0/PPG0(1)
35 AVss
34 AVRL
33 AVRH
32 AVcc
31 P57/AN15/DA1
1 P24/A20/IN0
2 P25/A21/IN1
3 P26/A22/IN2
4 P27/A23/IN3
5 P30/ALE/IN4
6 P31/RD/IN5
7 P32/WRL/WR/INT10R
8 P33/WRH
9 P34/HRQ/OUT4
10 P35/HAK/OUT5
11 P36/RDY/OUT6
12 P37/CLK/OUT7
13 P40
14 P41
15 Vcc
16 Vss
17 C
18 P42/IN6/RX1/INT9R
19 P43/IN7/TX1
20 P44/SDA0/FRCK0
21 P45/SCL0/FRCK1
22 P46/SDA1
23 P47/SCL1
24 P50/AN8/SIN2
25 P51/AN9/SOT2
26 P52/AN10/SCK2
27 P53/AN11/TIN3
28 P54/AN12/TOT3
29 P55/AN13
30 P56/AN14/DA0
(PQH100)

3. Pin Description

Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
90	92	X1	A	Oscillation output pin
91	93	X0		Oscillation input pin
52	54	$\overline{RST}$	E	Reset input pin
75 to 82	77 to 84	P00 to P07	G	General purpose I/O ports The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD00 to AD07		I/O pins for 8 lower bits of the external address/data bus. This function is enabled when the external bus is enabled.
		INT8 to INT15		External interrupt request input pins for INT8 to INT15.
83	85	P10	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD08		I/O pin of the external address/data bus (AD08). This function is enabled when the external bus is enabled.
		TIN1		Event input pin for the reload timer 1
84	86	P11	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD09		I/O pin of the external address/data bus (AD09). This function is enabled when the external bus is enabled.
		TOT1		Output pin for the reload timer 1
85	87	P12	N	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD10		I/O pin of the external address/data bus (AD10). This function is enabled when the external bus is enabled.
		SIN3		Serial data input pin for UART3
		INT11R		External interrupt request input pin for INT11R
86	88	P13	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD11		I/O pin of the external address/data bus (AD11). This function is enabled when the external bus is enabled.
		SOT3		Serial data output pin for UART3
87	89	P14	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD12		I/O pin of the external address/data bus (AD12). This function is enabled when the external bus is enabled.
		SCK3		Clock I/O pin for UART3

Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
92	94	P15	N	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD13		I/O pin of the external address/data bus (AD13). This function is enabled when the external bus is enabled.
		SIN4		Serial data input pin for UART4
93	95	P16	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD14		I/O pin of the external address/data bus (AD14). This function is enabled when the external bus is enabled.
		SOT4		Serial data output pin for UART4
94	96	P17	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		AD15		I/O pin of the external address/data bus (AD15). This function is enabled when the external bus is enabled.
		SCK4		Clock I/O pin for UART4
95 to 98	97 to 100	P20 to P23	G	General purpose I/O ports The register can be set to select whether to use a pull-up resistor.In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A16 to A19		A16 to A19 for output pins of the external address/data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A16 to A19).
		PPG9, PPGB, PPGD, PPGF		Output pins for PPGs
99, 100, 1, 2	1 to 4	P24 to P27	G	General purpose I/O ports The register can be set to select whether to use a pull-up resistor. In external bus mode, the pin is enabled as a general-purpose I/O port when the corresponding bit in the external address output control register (HACR) is 1.
		A20 to A23		A20 to A23 for output pins of the external address/data bus. When the corresponding bit in the external address output control register (HACR) is 0, the pins are enabled as high address output pins (A20 to A23).
		IN0 to IN3		Data sample input pins for input capture ICU0 to ICU3.
3	5	P30	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		ALE		Address latch enable output pin. This function is enabled when the external bus is enabled.
		IN4		Data sample input pin for input capture ICU4.

Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
4	6	P31	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled in single-chip mode.
		$\overline{RD}$		External read strobe output pin for data bus. This function is enabled when the external bus is enabled.
		IN5		Data sample input pin for input capture ICU5.
5	7	P32	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WR}$/$\overline{WRL}$ pin output is disabled.
		$\overline{WRL}$/ $\overline{WR}$		Write strobe output pin for the external data bus. This function is enabled when both the external bus and the $\overline{WR}$/$\overline{WRL}$ pin output are enabled. $\overline{WRL}$ is used to write-strobe 8 lower bits of the data bus in 16-bit access while $\overline{WR}$ is used to write-strobe 8 bits of the data bus in 8-bit access.
		INT10R		External interrupt request input pin for INT10R.
6	8	P33	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the $\overline{WRH}$ pin output is disabled.
		$\overline{WRH}$		Write strobe output pin for the upper 8 bits of the external data bus. This function is enabled when the external bus is enabled, when the external bus 16-bit mode is selected, and when the $\overline{WRH}$ output pin is enabled.
7	9	P34	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the hold function is disabled.
		HRQ		Hold request input pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT4		Waveform output pin for output compare OCU4.
8	10	P35	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the hold function is disabled.
		$\overline{HAK}$		Hold acknowledge output pin. This function is enabled when both the external bus and the hold function are enabled.
		OUT5		Waveform output pin for output compare OCU5.
9	11	P36	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor. This function is enabled either in single-chip mode or when the external ready function is disabled.
		RDY		Ready input pin. This function is enabled when both the external bus and the external ready function are enabled.
		OUT6		Waveform output pin for output compare OCU6.

Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
10	12	P37	G	General purpose I/O port The register can be set to select whether to use a pull-up resistor.This function is enabled either in single-chip mode or when the clock output is disabled.
		CLK		Clock output pin. This function is enabled when both the external bus and clock output are enabled.
		OUT7		Waveform output pin for output compare OCU7.
11, 12	13, 14	P40, P41	F	General purpose I/O ports
16	18	P42	F	General purpose I/O port
		IN6		Data sample input pin for input capture ICU6.
		RX1		RX input pin for CAN1 Interface
		INT9R		External interrupt request input pin for INT9R.
17	19	P43	F	General purpose I/O port
		IN7		Data sample input pin for input capture ICU7.
		TX1		TX Output pin for CAN1
18	20	P44	H	General purpose I/O port
		SDA0		Serial data I/O pin for I^2C 0
		FRCK0		Input pin for the 16-bit I/O Timer 0
19	21	P45	H	General purpose I/O port
		SCL0		Serial clock I/O pin for I^2C 0
		FRCK1		Input pin for the 16-bit I/O Timer1
20	22	P46	H	General purpose I/O port
		SDA1		Serial data I/O pin for I^2C 1
21	23	P47	H	General purpose I/O port
		SCL1		Serial clock I/O pin for I^2C 1
22	24	P50	O	General purpose I/O port
		AN8		Analog input pin for the A/D converter
		SIN2		Serial data input pin for UART2
23	25	P51	I	General purpose I/O port
		AN9		Analog input pin for the A/D converter
		SOT2		Serial data output pin for UART2
24	26	P52	I	General purpose I/O port
		AN10		Analog input pin for the A/D converter
		SCK2		Clock I/O pin for UART2
25	27	P53	I	General purpose I/O port
		AN11		Analog input pin for the A/D converter
		TIN3		Event input pin for the reload timer 3
26	28	P54	I	General purpose I/O port
		AN12		Analog input pin for the A/D converter
		TOT3		Output pin for the reload timer 3

Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
27	29	P55	I	General purpose I/O port
		AN13		Analog input pin for the A/D converter
28, 29	30, 31	P56, P57	J	General purpose I/O ports
		AN14, AN15		Analog input pins for the A/D converter
		DA0,DA1		Analog output pins for the D/A converter
34 to 41	36 to 43	P60 to P67	I	General purpose I/O ports
		AN0 to AN7		Analog input pins for the A/D converter
		PPG0, PPG2, PPG4, PPG6, PPG8, PPGA, PPGC, PPGE		Output pins for PPGs
43 to 48, 53, 54	45 to 50, 55, 56	P70 to P77	I	General purpose I/O ports
		AN16 to AN23		Analog input pins for the A/D converter
		INT0 to INT7		External interrupt request input pins for INT0 to INT7
55	57	P80	F	General purpose I/O port
		TIN0		Event input pin for the reload timer 0
		ADTG		Trigger input pin for the A/D converter
		INT12R		External interrupt request input pin for INT12R
56	58	P81	F	General purpose I/O port
		TOT0		Output pin for the reload timer 0
		CKOT		Output pin for the clock monitor
		INT13R		External interrupt request input pin for INT13R
57	59	P82	M	General purpose I/O port
		SIN0		Serial data input pin for UART0
		TIN2		Event input pin for the reload timer 2
		INT14R		External interrupt request input pin for INT14R
58	60	P83	F	General purpose I/O port
		SOT0		Serial data output pin for UART 0
		TOT2		Output pin for the reload timer 2
59	61	P84	F	General purpose I/O port
		SCK0		Clock I/O pin for UART0
		INT15R		External interrupt request input pin for INT15R
60	62	P85	M	General purpose I/O port
		SIN1		Serial data input pin for UART1
61	63	P86	F	General purpose I/O port
		SOT1		Serial data output pin for UART1

Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
62	64	P87	F	General purpose I/O port
		SCK1		Clock I/O pin for UART1
65	67	P90	M	General purpose I/O port
		PPG1		Output pin for PPGs
		SIN5		Serial data input pin for UART5
66	68	P91	F	General purpose I/O port
		PPG3		Output pin for PPGs
		SOT5		Serial data output pin for UART5
67	69	P92	F	General purpose I/O port
		PPG5		Output pin for PPGs
		SCK5		Clock I/O pin for UART5
68	70	P93	F	General purpose I/O port
		PPG7		Output pin for PPGs
69	71	P94	M	General purpose I/O port
		OUT0		Waveform output pin for output compare for OCU0. This function is enabled when the waveform output is enabled.
		SIN6		Serial data input pin for UART6
70	72	P95	F	General purpose I/O port
		OUT1		Waveform output pin for output compare for OCU1.This function is enabled when the waveform output is enabled.
		SOT6		Serial data output pin for UART6
71	73	P96	F	General purpose I/O port
		OUT2		Waveform output pin for output compare for OCU2. This function is enabled when the waveform output is enabled.
		SCK6		Clock I/O pin for UART6
72	74	P97	F	General purpose I/O port
		OUT3		Waveform output pin for output compare for OCU3. This function is enabled when the waveform output is enabled.
73	75	PA0	F	General purpose I/O port
		RX0		RX input pin for CAN0 Interface. Outputs generated by other functions must be stopped when using the CAN functions.
		INT8R		External interrupt request input pin for INT8R
74	76	PA1	F	General purpose I/O port
		TX0		TX Output pin for CAN0
30	32	AV_{CC}	K	V_{CC} power input pin for the Analog circuit
31	33	AVRH	L	Reference voltage input pin for the A/D Converter. This power supply must be turned on or off while a voltage higher than or equal to AVRH is applied to AV_{CC}.
32	34	AVRL	K	Lower reference voltage input pin for the A/D Converter
33	35	AV_{SS}	K	V_{SS} power input pin for the Analog circuit
50, 51	52, 53	MD1, MD0	C	Input pins for specifying the operating mode

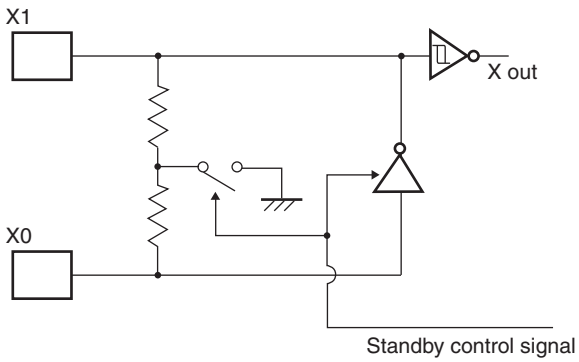
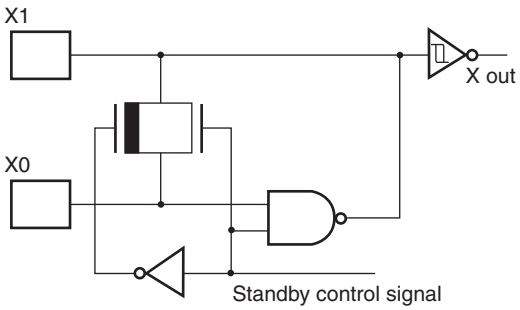
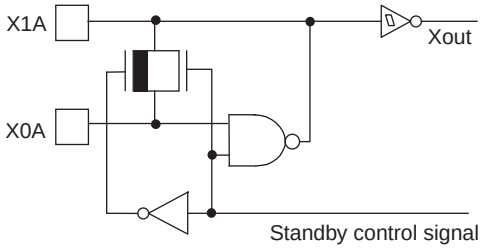
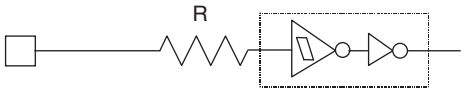
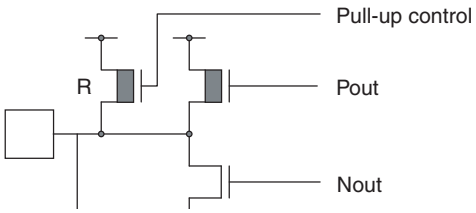
Pin No.		Pin Name	I/O Circuit Type*3	Function
LQFP100*1	QFP100*2			
49	51	MD2	D	Input pin for specifying the operating mode
13, 63, 88	15, 65, 90	V_{CC}	—	Power (3.5 V to 5.5 V) input pins
14, 42, 64, 89	16, 44, 66, 91	V_{SS}	—	Power (0 V) input pins
15	17	C	K	This is the power supply stabilization capacitor. This pin should be connected to a ceramic capacitor with a capacitance greater than or equal to 0.1 μF.

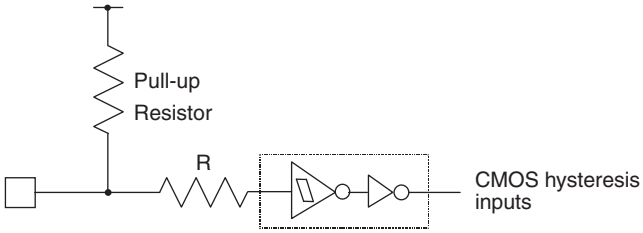
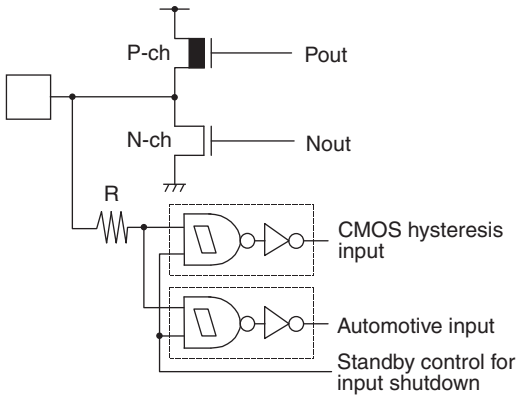
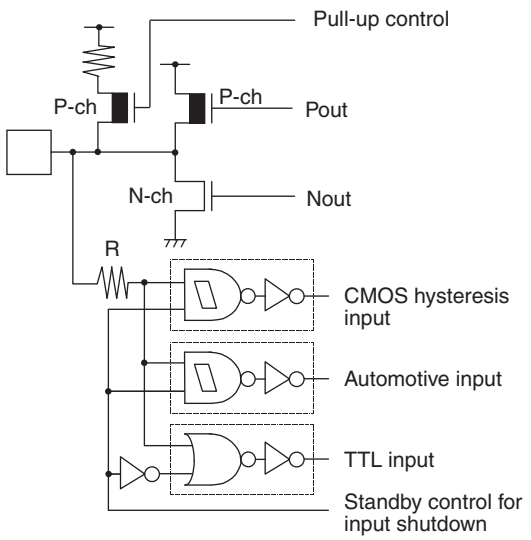
*1 : LQI100

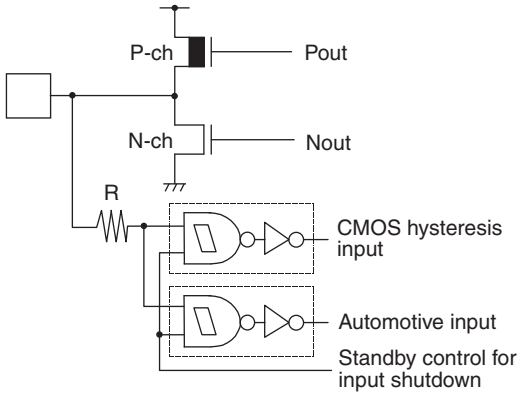
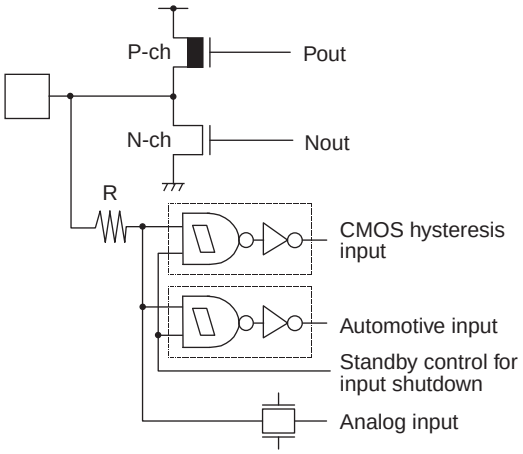
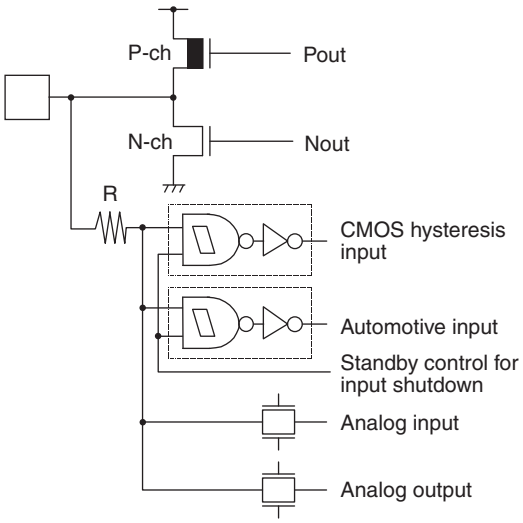
*2 : PQH100

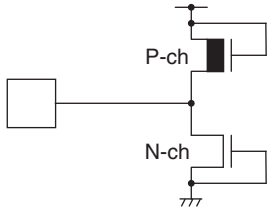
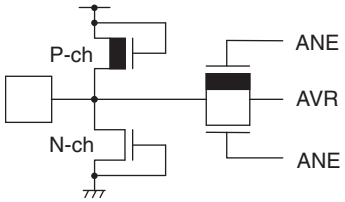
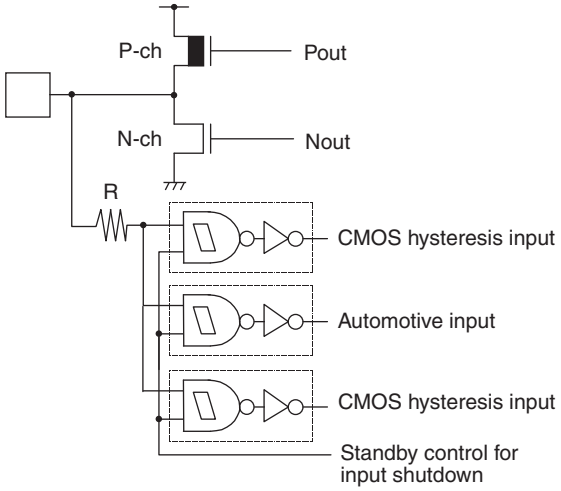
*3 : For I/O circuit type, refer to “I/O Circuit Types”.

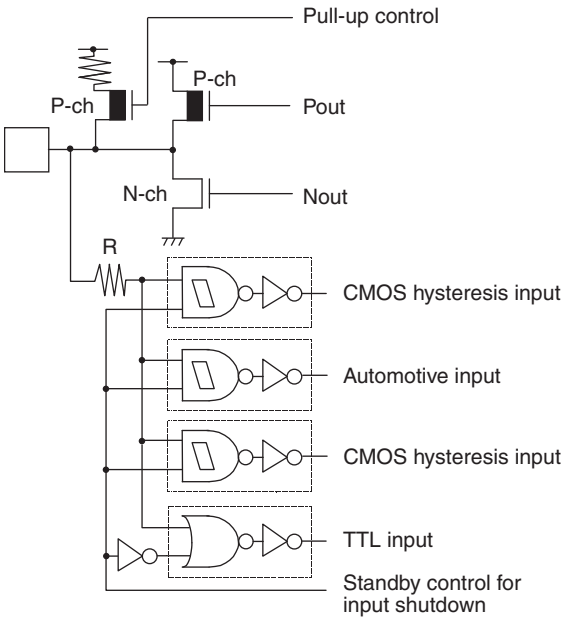
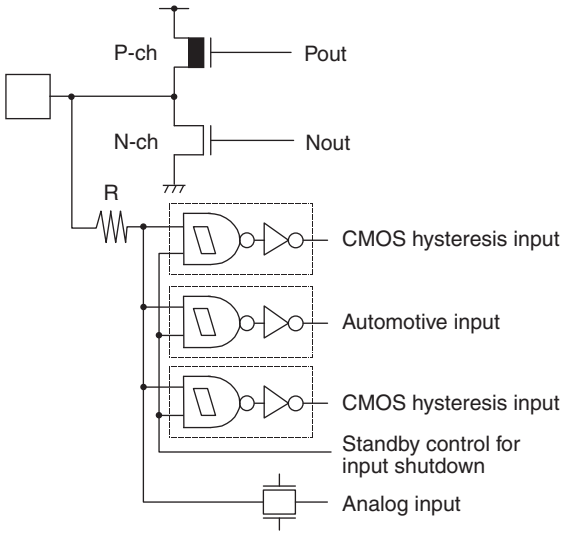
4. I/O Circuit Types

Type	Circuit	Remarks
A		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ (Flash memory product)
		Oscillation circuit High-speed oscillation feedback resistor = approx. 1 MΩ (Evaluation product)
B		Oscillation circuit Low-speed oscillation feedback resistor = approx. 10 MΩ
C		Evaluation products: CMOS hysteresis input Flash memory products: CMOS input pin
D		Evaluation products: • CMOS hysteresis input • Pull-down resistor value: approx. 50 kΩ Flash memory products: • CMOS input • No pull-down

Type	Circuit	Remarks
E		• CMOS hysteresis input • Pull-up resistor value: approx. 50 kΩ
F		• CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby)
G		• CMOS level output (I_{OL} = 4 mA, I_{OH} = −4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) • Programmable pull-up resistor: 50 kΩ approx.

Type	Circuit	Remarks
H		• CMOS level output (I_{OL} = 3 mA, I_{OH} = –3 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby)
I		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input
J		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • D/A analog output • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • A/D converter analog input • D/A converter analog output

Type	Circuit	Remarks
K		Power supply input protection circuit
L		A/D converter reference voltage power supply input pin, with the protection circuit Flash memory devices do not have a protection circuit against V_{CC} for pin AVRH
M		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby)

Type	Circuit	Remarks
N		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • TTL input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby) • Programmable pull-up resistor: 50 kΩ approx
O		• CMOS level output (I_{OL} = 4 mA, I_{OH} = –4 mA) • CMOS hysteresis input (V_{IH} 0.8 V_{CC} V_{IL} 0.2 V_{CC}) (with function to disconnect input during standby) • Automotive input (with function to disconnect input during standby) • CMOS hysteresis input (V_{IH} 0.7 V_{CC} V_{IL} 0.3 V_{CC}) (with function to disconnect input during standby) • A/D converter analog input

5. Handling Devices

■ Preventing Latch-up

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, also be careful not to let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

■ Handling Unused Pins

Leaving unused input pins open may result in misbehavior or latch-up and possible permanent damage to the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

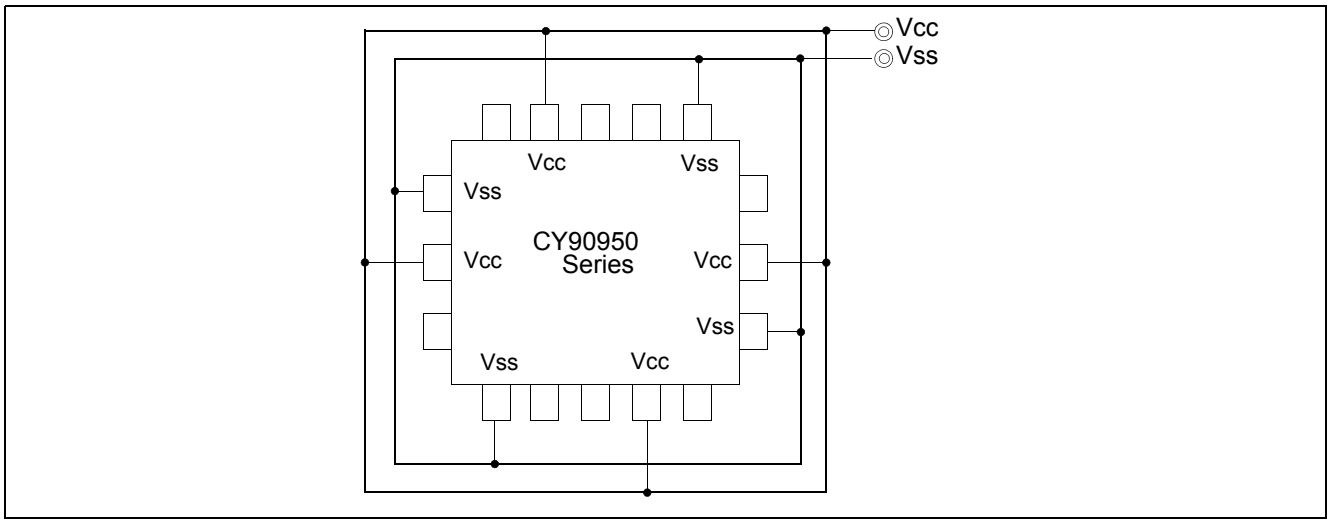
Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

■ Power Supply Pins (V_{CC}/V_{SS})

- If there are multiple V_{CC} and V_{SS} pins, that are designed to be set to the same potential are connected the inside of the device to prevent malfunctions such as latch-up.

To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the V_{CC} and V_{SS} pins to the power supply and ground externally. Connect V_{CC} and V_{SS} pins to the device from the current supply source at a low impedance.

- As a measure against power supply noise, connect a capacitor of about 0.1 μF as a bypass capacitor between V_{CC} and V_{SS} pins in the vicinity of V_{CC} and V_{SS} pins of the device



■ Mode Pins (MD0 to MD2)

Connect the mode pins directly to V_{CC} or V_{SS} pins. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{CC} or V_{SS} pins and to provide a low-impedance connection.

■ Sequence for Turning On the Power Supply to the A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN23) after turning-on the digital power supply (V_{CC}).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

■ Pin connection when A/D Converter is Not Used

Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = AVRL = V_{SS}$.

■ Crystal Oscillator Circuit

The X0, X1 pins may be possible causes of abnormal operation. Make sure to provide bypass capacitors via the shortest distance from X0, X1 pins and crystal oscillator (or ceramic oscillator) and ground lines, and make sure, to the utmost effort, that the oscillation circuit lines do not cross the lines of other circuits. It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins with a ground area for stabilizing the operation.

For each of the mass-production products, request an oscillator evaluation from the manufacturer of the oscillator you are using.

■ Pull-up/down Resistors

The CY90950 Series does not support internal pull-up/down resistors (except for the pull-up resistors built into ports 0 to 3). Use external components where needed.

■ Using External Clock

The external clock inputs can not be used.

■ Notes on Operation in PLL Clock Mode

If PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or the external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ Notes on Power-On

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during power-on to 50 μs or more (0.2 V to 2.7 V) .

■ Stabilization of Power Supply Voltage

A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.

Stabilize the power supply voltage as follows as a standard level of stabilization.

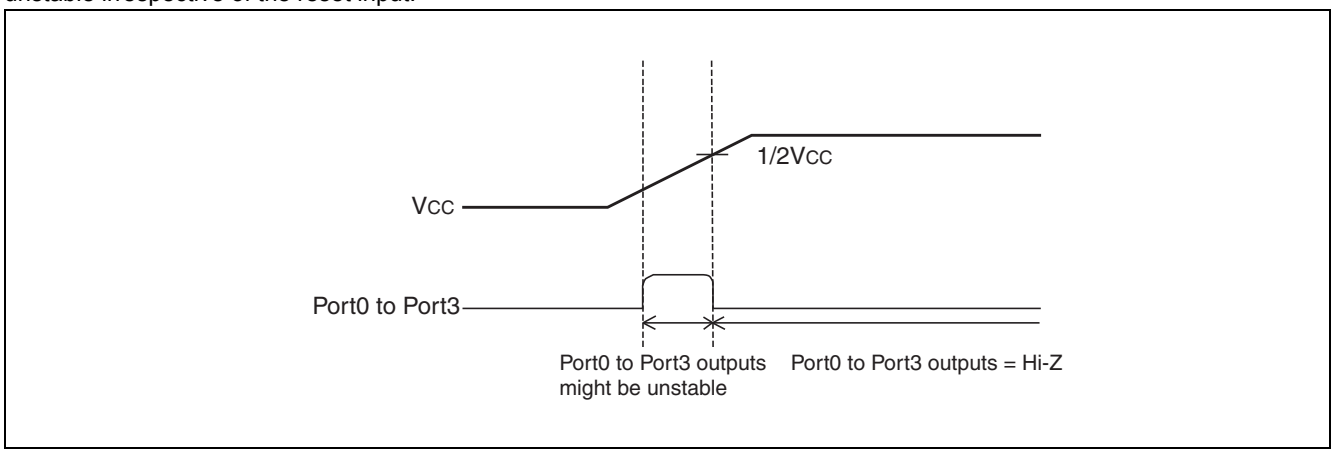
- V_{CC} ripple variations (peak-to-peak value) at commercial frequencies (50 Hz/60 Hz) fall below 10% of the standard V_{CC} supply voltage
- The coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.

■ Initialization

In the device, there are internal registers which are initialized only by a power-on reset. To initialize these registers, turn on the power again.

■ Port 0 to Port 3 Output During Power-on (External-bus Mode)

As shown below, when the power is turned on in External-Bus mode, there is a possibility that output signal of Port 0 to Port 3 might be unstable irrespective of the reset input.



■ Notes on Using the CAN Function

To use the CAN function, please set the DIRECT bit of the CAN Direct Mode Register (CDMR) to 1.
If the DIRECT bit is set to '0' (initial value) only CY90V950AJAS and CY90V950AMAS, wait states will be performed when accessing CAN registers.

Note : Please refer to the Hardware Manual of the CY90950 series for detail of CAN Direct Mode Register.

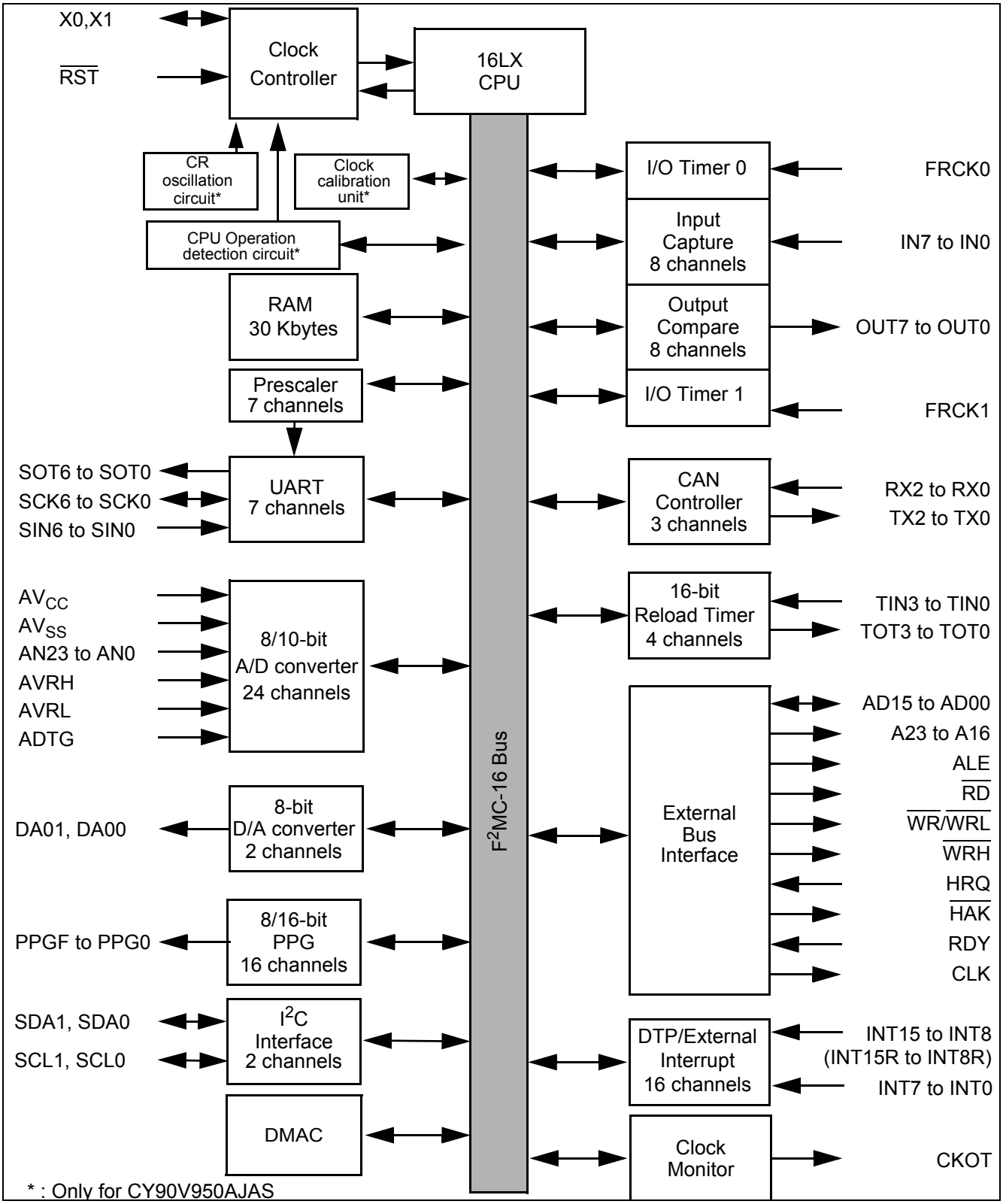
■ Flash Security Function

A security bit is located in the area of the Flash memory.
If protection code 01_H is written in the security bit, the Flash memory is in the protected state by security.
Therefore please do not write 01_H in this address if you do not use the security function.
Refer to following table for the address of the security bit.

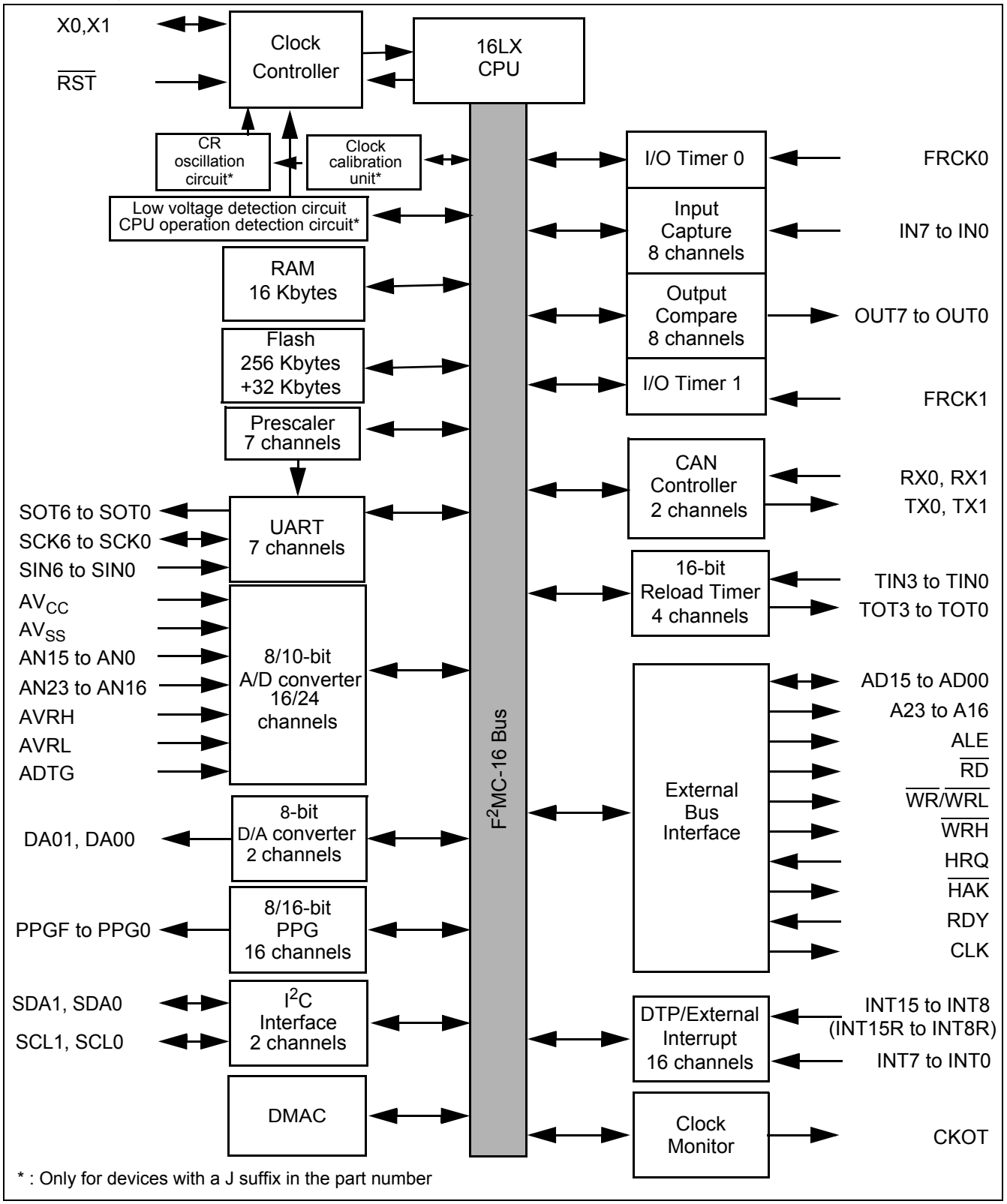
	Flash Memory Size	Address of the Security Bit
CY90F952JDS, CY90F952MDS	Embedded 2 Mbits Flash Memory	$FC0001_H$

6. Block Diagrams

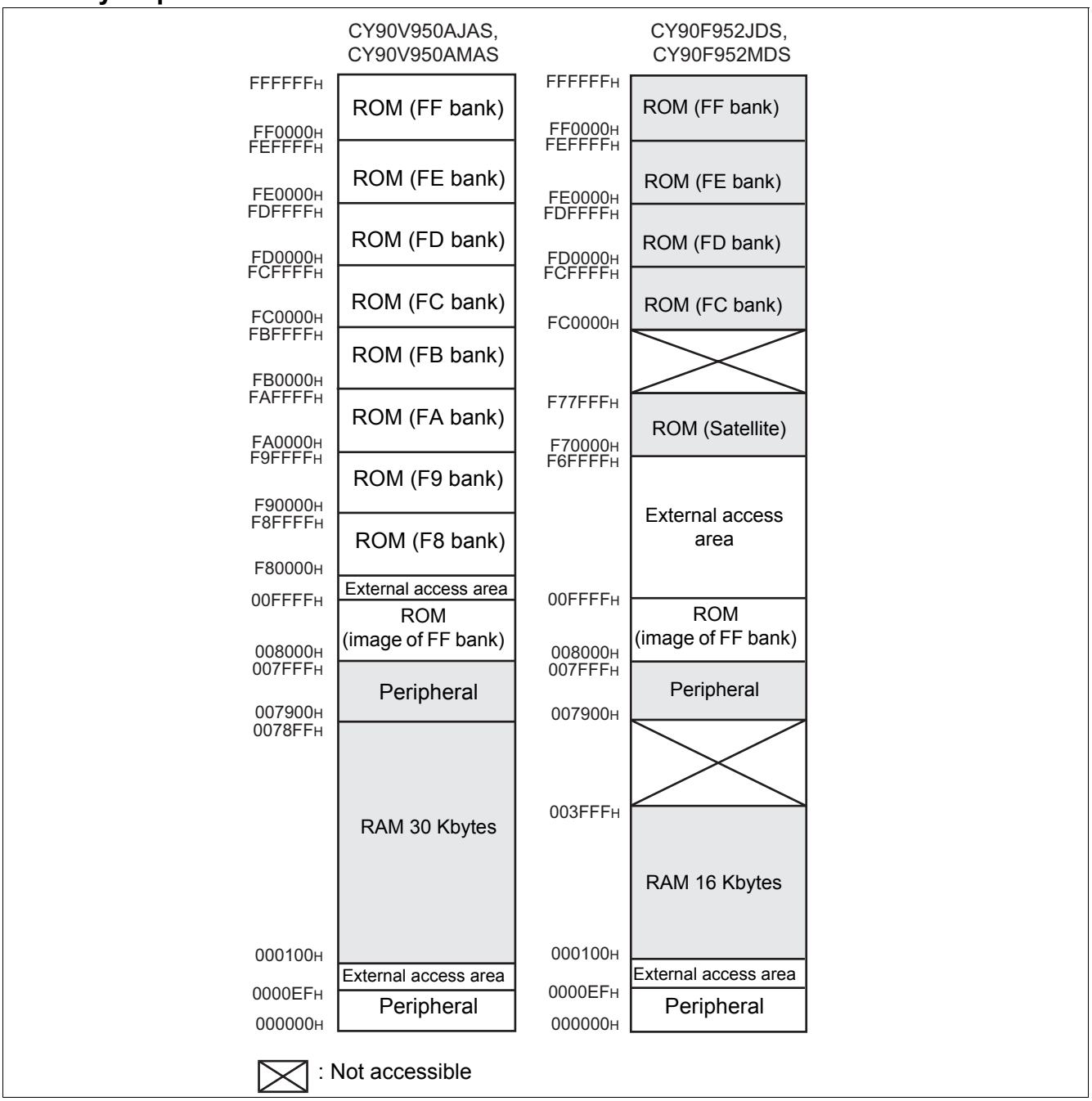
■ CY90V950AJAS,CY90V950AMAS



■ CY90F952JDS, CY90F952MDS



7. Memory Map



Note: An image of the data in the FF bank of ROM is visible in the upper part of bank 00, which makes it possible for the C compiler to use the small memory model. The lower 16 bits of addresses in the FF bank are the same as the lower 16 bits of addresses in the 00 bank so that tables stored in the ROM can be accessed without using the far specifier in the pointer declaration. For example, when the address $00C000_H$ is accessed, the data at $FFC000_H$ in ROM is actually accessed.
The ROM area in bank FF exceeds 32 Kbytes, and its entire image cannot be shown in bank 00.
As a result, the image between $FF8000_H$ and $FFFFFF_H$ is visible in bank 00, while the image between $FF0000_H$ and $FF7FFF_H$ is visible only in bank FF.

8. I/O Map

Address	Register	Abbreviation	Access	Resource Name	Initial Value
000000_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
000001_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
000002_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
000003_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
000004_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
000005_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
000006_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
000007_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
000008_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
000009_H	Port 9 Data Register	PDR9	R/W	Port 9	$XXXXXXXX_B$
$00000A_H$	Port A Data Register	PDRA	R/W	Port A	$111111XX_B$
$00000B_H$	Analog Input Enable Register 5	ADER5	R/W	Port 5, A/D	11111111_B
$00000C_H$	Analog Input Enable Register 6	ADER6	R/W	Port 6, A/D	11111111_B
$00000D_H$	Analog Input Enable Register 7	ADER7	R/W	Port 7, A/D	11111111_B
$00000E_H$	Input Level Select Register 0	ILSR0	R/W	Port 0 to 7	$XXXXXXXX_B$
$00000F_H$	Input Level Select Register 1	ILSR1	R/W	Port 0 to 3, Port 8 to A	$XXXX0XXX_B$
000010_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
000011_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
000012_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
000013_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
000014_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
000015_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
000016_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
000017_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
000018_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
000019_H	Port 9 Direction Register	DDR9	R/W	Port 9	00000000_B
$00001A_H$	Port A Direction Register	DDRA	R/W	Port A	00000100_B
$00001B_H$	Reserved				
$00001C_H$	Port 0 Pull-up Control Register	PUCR0	R/W	Port 0	00000000_B
$00001D_H$	Port 1 Pull-up Control Register	PUCR1	R/W	Port 1	00000000_B
$00001E_H$	Port 2 Pull-up Control Register	PUCR2	R/W	Port 2	00000000_B
$00001F_H$	Port 3 Pull-up Control Register	PUCR3	R/W	Port 3	00000000_B
000020_H	Serial Mode Register 0	SMR0	W, R/W	UART0	00000000_B
000021_H	Serial Control Register 0	SCR0	W, R/W		00000000_B
000022_H	Reception/Transmission Data Register 0	RDR0/TDR0	R/W		00000000_B/ 11111111_B
000023_H	Serial Status Register 0	SSR0	R, R/W		00001000_B
000024_H	Extended Communication Control Register 0	ECCR0	R, W, R/W		$000000XX_B$
000025_H	Extended Status/Control Register 0	ESCR0	R/W		$00000X00_B$
000026_H	Baud Rate Generator Register 00	BGR00	R, R/W		00000000_B
000027_H	Baud Rate Generator Register 01	BGR01	R, R/W		00000000_B

Address	Register	Abbreviation	Access	Resource Name	Initial Value
000028_H	Serial Mode Register 1	SMR1	W, R/W	UART1	00000000_B
000029_H	Serial Control Register 1	SCR1	W, R/W		00000000_B
$00002A_H$	Reception/Transmission Data Register 0	RDR1/TDR1	R/W		00000000_B/ 11111111_B
$00002B_H$	Serial Status Register 1	SSR1	R, R/W		00001000_B
$00002C_H$	Extended Communication Control Register 1	ECCR1	R, W, R/W		$000000XX_B$
$00002D_H$	Extended Status/Control Register 1	ESCR1	R/W		$00000X00_B$
$00002E_H$	Baud Rate Generator Register 10	BGR10	R, R/W		00000000_B
$00002F_H$	Baud Rate Generator Register 11	BGR11	R, R/W		00000000_B
000030_H	PPG0 Operation Mode Control Register	PPGC0	W, R/W	16-bit PPG0/PPG1	01000111_B
000031_H	PPG1 Operation Mode Control Register	PPGC1	W, R/W		01000001_B
000032_H	PPG0/PPG1 Count Clock Select Register	PPG01	R/W		00000010_B
000033_H	Reserved				
000034_H	PPG2 Operation Mode Control Register	PPGC2	W, R/W	16-bit PPG2/PPG3	01000111_B
000035_H	PPG3 Operation Mode Control Register	PPGC3	W, R/W		01000001_B
000036_H	PPG2/PPG3 Count Clock Select Register	PPG23	R/W		00000010_B
000037_H	Reserved				
000038_H	PPG4 Operation Mode Control Register	PPGC4	W, R/W	16-bit PPG4/PPG5	01000111_B
000039_H	PPG5 Operation Mode Control Register	PPGC5	W, R/W		01000001_B
$00003A_H$	PPG4/PPG5 Clock Select Register	PPG45	R/W		00000010_B
$00003B_H$	Address Detect Control Register 1	PACSR1	R/W	Address Match Detection 1	11000000_B
$00003C_H$	PPG6 Operation Mode Control Register	PPGC6	W, R/W	16-bit PPG6/PPG7	01000111_B
$00003D_H$	PPG7 Operation Mode Control Register	PPGC7	W, R/W		01000001_B
$00003E_H$	PPG6/PPG7 Count Clock Select Register	PPG67	R/W		00000010_B
$00003F_H$	Reserved				
000040_H	PPG8 Operation Mode Control Register	PPGC8	W, R/W	16-bit PPG8/PPG9	01000111_B
000041_H	PPG9 Operation Mode Control Register	PPGC9	W, R/W		01000001_B
000042_H	PPG8/PPG9 Count Clock Select Register	PPG89	R/W		00000010_B
000043_H	Reserved				
000044_H	PPGA Operation Mode Control Register	PPGCA	W, R/W	16-bit PPGA/PPGB	01000111_B
000045_H	PPGB Operation Mode Control Register	PPGCB	W, R/W		01000001_B
000046_H	PPGA/PPGB Count Clock Select Register	PPGAB	R/W		00000010_B
000047_H	Reserved				
000048_H	PPGC Operation Mode Control Register	PPGCC	W, R/W	16-bit PPGC/PPGD	01000111_B
000049_H	PPGD Operation Mode Control Register	PPGCD	W, R/W		01000001_B
$00004A_H$	PPGC/PPGD Count Clock Select Register	PPGCD	R/W		00000010_B
$00004B_H$	Reserved				
$00004C_H$	PPGE Operation Mode Control Register	PPGCE	W, R/W	16-bit PPGE/PPGF	01000111_B
$00004D_H$	PPGF Operation Mode Control Register	PPGCF	W, R/W		01000001_B
$00004E_H$	PPGE/PPGF Count Clock Select Register	PPGEF	R/W		00000010_B
$00004F_H$	Reserved				

Address	Register	Abbreviation	Access	Resource Name	Initial Value
000050_H	Input Capture Control Status 0/1	ICS01	R/W	Input Capture 0/1	00000000_B
000051_H	Input Capture Edge 0/1	ICE01	R/W, R		$111010XX_B$
000052_H	Input Capture Control Status 2/3	ICS23	R/W	Input Capture 2/3	00000000_B
000053_H	Input Capture Edge 2/3	ICE23	R		$111111XX_B$
000054_H	Input Capture Control Status 4/5	ICS45	R/W	Input Capture 4/5	00000000_B
000055_H	Input Capture Edge 4/5	ICE45	R		$111100XX_B$
000056_H	Input Capture Control Status 6/7	ICS67	R/W	Input Capture 6/7	00000000_B
000057_H	Input Capture Edge 6/7	ICE67	R/W, R		$111000XX_B$
000058_H	Output Compare Control Status 0	OCS0	R/W	Output Compare 0/1	00001100_B
000059_H	Output Compare Control Status 1	OCS1	R/W		01100000_B
$00005A_H$	Output Compare Control Status 2	OCS2	R/W	Output Compare 2/3	00001100_B
$00005B_H$	Output Compare Control Status 3	OCS3	R/W		01100000_B
$00005C_H$	Output Compare Control Status 4	OCS4	R/W	Output Compare 4/5	00001100_B
$00005D_H$	Output Compare Control Status 5	OCS5	R/W		01100000_B
$00005E_H$	Output Compare Control Status 6	OCS6	R/W	Output Compare 6/7	00001100_B
$00005F_H$	Output Compare Control Status 7	OCS7	R/W		01100000_B
000060_H	Timer Control Status 0	TMCSR0	R/W	16-bit reload timer 0	00000000_B
000061_H	Timer Control Status 0	TMCSR0	R/W		11110000_B
000062_H	Timer Control Status 1	TMCSR1	R/W	16-bit reload timer 1	00000000_B
000063_H	Timer Control Status 1	TMCSR1	R/W		11110000_B
000064_H	Timer Control Status 2	TMCSR2	R/W	16-bit reload timer 2	00000000_B
000065_H	Timer Control Status 2	TMCSR2	R/W		11110000_B
000066_H	Timer Control Status 3	TMCSR3	R/W	16-bit reload timer 3	00000000_B
000067_H	Timer Control Status 3	TMCSR3	R/W		11110000_B
000068_H	A/D Control Status 0	ADCS0	R/W	A/D Converter	00011110_B
000069_H	A/D Control Status 1	ADCS1	R/W		00000001_B
$00006A_H$	A/D Data 0	ADCR0	R		00000000_B
$00006B_H$	A/D Data 1	ADCR1	R		11111100_B
$00006C_H$	ADC Setting 0	ADSR0	R/W		00000000_B
$00006D_H$	ADC Setting 1	ADSR1	R/W		00000000_B
$00006E_H$	Low Voltage/CPU OPeration Detection Reset Control Register	LVRC	R/W	Low Voltage/CPU Operation Detection Reset	00111000_B
$00006F_H$	ROM Mirror Function Setting	ROMM	W	ROM Mirror	11111101_B
000070_H to $00008F_H$	Reserved for CAN Controller				
000090_H to $00009A_H$	Reserved				
$00009B_H$	DMA Descriptor Channel Specified Register	DCSR	R/W	DMA	00000000_B
$00009C_H$	DMA Status Register L	DSRL	R/W		00000000_B
$00009D_H$	DMA Status Register H	DSRH	R/W		00000000_B
$00009E_H$	Address Detect Control Register 0	PACSR0	R/W	Address Match Detection 0	11000000_B

Address	Register	Abbreviation	Access	Resource Name	Initial Value
$00009F_H$	Delayed Interrupt Trigger/Release Register	DIRR	R/W	Delayed Interrupt Generation Module	11111110_B
$0000A0_H$	Low-power Mode Control Register	LPMCR	W, R/W	Low Power Control Circuit	00011000_B
$0000A1_H$	Clock Selection Register	CKSCR	R, R/W	Low Power Control Circuit	11111100_B
$0000A2_H$, $0000A3_H$	Reserved				
$0000A4_H$	DMA Stop Status Register	DSSR	R/W	DMA	00000000_B
$0000A5_H$	Automatic Ready Function Select Register	ARSR	W	External Memory Access	00111100_B
$0000A6_H$	External Address Output Control Register	HACR	W		00000000_B
$0000A7_H$	Bus Control Signal Selection Register	ECSR	W		00000001_B
$0000A8_H$	Watchdog Control Register	WDTC	R, W	Watchdog Timer	$X1XXX111_B$
$0000A9_H$	Time Base Timer Control Register	TBTC	W, R/W	Time Base Timer	11100100_B
$0000AA_H$	Watch Timer Control Register	WTC	R, R/W	Watch Timer	$1X001000_B$
$0000AB_H$	Reserved				
$0000AC_H$	DMA Enable Register L	DERL	R/W	DMA	00000000_B
$0000AD_H$	DMA Enable Register H	DERH	R/W		00000000_B
$0000AE_H$	Flash Control Status Register (Flash memory devices only)	FMCS	R, R/W	Flash Memory	$000X0000_B$
$0000AF_H$	Reserved				
$0000B0_H$	Interrupt Control Register 00	ICR00	W, R/W	Interrupt Control	00000111_B
$0000B1_H$	Interrupt Control Register 01	ICR01	W, R/W		00000111_B
$0000B2_H$	Interrupt Control Register 02	ICR02	W, R/W		00000111_B
$0000B3_H$	Interrupt Control Register 03	ICR03	W, R/W		00000111_B
$0000B4_H$	Interrupt Control Register 04	ICR04	W, R/W		00000111_B
$0000B5_H$	Interrupt Control Register 05	ICR05	W, R/W		00000111_B
$0000B6_H$	Interrupt Control Register 06	ICR06	W, R/W		00000111_B
$0000B7_H$	Interrupt Control Register 07	ICR07	W, R/W		00000111_B
$0000B8_H$	Interrupt Control Register 08	ICR08	W, R/W		00000111_B
$0000B9_H$	Interrupt Control Register 09	ICR09	W, R/W		00000111_B
$0000BA_H$	Interrupt Control Register 10	ICR10	W, R/W		00000111_B
$0000BB_H$	Interrupt Control Register 11	ICR11	W, R/W		00000111_B
$0000BC_H$	Interrupt Control Register 12	ICR12	W, R/W		00000111_B
$0000BD_H$	Interrupt Control Register 13	ICR13	W, R/W		00000111_B
$0000BE_H$	Interrupt Control Register 14	ICR14	W, R/W		00000111_B
$0000BF_H$	Interrupt Control Register 15	ICR15	W, R/W		00000111_B
$0000C0_H$	D/A Converter Data 0	DAT0	R/W	D/A Converter	$XXXXXXXX_B$
$0000C1_H$	D/A Converter Data 1	DAT1	R/W		$XXXXXXXX_B$
$0000C2_H$	D/A Control 0	DACR0	R/W		00000000_B
$0000C3_H$	D/A Control 1	DACR1	R/W		00000000_B

Address	Register	Abbreviation	Access	Resource Name	Initial Value
$0000C4_H$, $0000C5_H$	Reserved				
$0000C6_H$	External Interrupt Enable 0	ENIR0	R/W	DTP/External Interrupt 0	00000000_B
$0000C7_H$	External Interrupt Source 0	EIRR0	R/W		$XXXXXXXX_B$
$0000C8_H$	Detection Level Setting 0	ELVR0	R/W		00000000_B
$0000C9_H$	Detection Level Setting 0	ELVR0	R/W		00000000_B
$0000CA_H$	External Interrupt Enable 1	ENIR1	R/W	DTP/External Interrupt 1	00000000_B
$0000CB_H$	External Interrupt Source 1	EIRR1	R/W		$XXXXXXXX_B$
$0000CC_H$	Detection Level Setting 1	ELVR1	R/W		00000000_B
$0000CD_H$	Detection Level Setting 1	ELVR1	R/W		00000000_B
$0000CE_H$	External Interrupt Source Select	EISSR	R/W		00000000_B
$0000CF_H$	PLL/Sub clock Control Register	PSCCR	W	PLL	11110000_B
$0000D0_H$	DMA Buffer Address Pointer L Register	BAPL	R/W	DMA	$XXXXXXXX_B$
$0000D1_H$	DMA Buffer Address Pointer M Register	BAPM	R/W		$XXXXXXXX_B$
$0000D2_H$	DMA Buffer Address Pointer H Register	BAPH	R/W		$XXXXXXXX_B$
$0000D3_H$	DMA Control Register	DMACS	R/W		$XXXXXXXX_B$
$0000D4_H$	I/O Register Address Pointer L Register	IOAL	R/W		$XXXXXXXX_B$
$0000D5_H$	I/O Register Address Pointer H Register	IOAH	R/W		$XXXXXXXX_B$
$0000D6_H$	Data Counter L Register	DCTL	R/W		$XXXXXXXX_B$
$0000D7_H$	Data Counter H Register	DCTH	R/W		$XXXXXXXX_B$
$0000D8_H$	Serial Mode Register 2	SMR2	W, R/W	UART2	00000000_B
$0000D9_H$	Serial Control Register 2	SCR2	W, R/W		00000000_B
$0000DA_H$	Reception/Transmission Data Register 2	RDR2/TDR2	R/W		00000000_B/ 11111111_B
$0000DB_H$	Serial Status Register 2	SSR2	R, R/W		00001000_B
$0000DC_H$	Extended Communication Control Register 2	ECCR2	R, W, R/W		$000000XX_B$
$0000DD_H$	Extended Status Control Register 2	ESCR2	R/W		$00000X00_B$
$0000DE_H$	Baud Rate Generator Register 20	BGR20	R, R/W		00000000_B
$0000DF_H$	Baud Rate Generator Register 21	BGR21	R, R/W		00000000_B
$0000E0_H$ to $0000EF_H$	Reserved for CAN Controller 2. Refer to "CAN Controllers"				
$0000F0_H$ to $0000FF_H$	External				
007900_H	Reload Register L0	PRLL0	R/W	16-bit PPG0/PPG1	$XXXXXXXX_B$
007901_H	Reload Register H0	PRLH0	R/W		$XXXXXXXX_B$
007902_H	Reload Register L1	PRLL1	R/W		$XXXXXXXX_B$
007903_H	Reload Register H1	PRLH1	R/W		$XXXXXXXX_B$
007904_H	Reload Register L2	PRLL2	R/W	16-bit PPG2/PPG3	$XXXXXXXX_B$
007905_H	Reload Register H2	PRLH2	R/W		$XXXXXXXX_B$
007906_H	Reload Register L3	PRLL3	R/W		$XXXXXXXX_B$
007907_H	Reload Register H3	PRLH3	R/W		$XXXXXXXX_B$

Address	Register	Abbreviation	Access	Resource Name	Initial Value
007908_H	Reload Register L4	PRLL4	R/W	16-bit PPG4/PPG5	$XXXXXXXX_B$
007909_H	Reload Register H4	PRLH4	R/W		$XXXXXXXX_B$
$00790A_H$	Reload Register L5	PRLL5	R/W		$XXXXXXXX_B$
$00790B_H$	Reload Register H5	PRLH5	R/W		$XXXXXXXX_B$
$00790C_H$	Reload Register L6	PRLL6	R/W	16-bit PPG6/PPG7	$XXXXXXXX_B$
$00790D_H$	Reload Register H6	PRLH6	R/W		$XXXXXXXX_B$
$00790E_H$	Reload Register L7	PRLL7	R/W		$XXXXXXXX_B$
$00790F_H$	Reload Register H7	PRLH7	R/W		$XXXXXXXX_B$
007910_H	Reload Register L8	PRLL8	R/W	16-bit PPG8/PPG9	$XXXXXXXX_B$
007911_H	Reload Register H8	PRLH8	R/W		$XXXXXXXX_B$
007912_H	Reload Register L9	PRLL9	R/W		$XXXXXXXX_B$
007913_H	Reload Register H9	PRLH9	R/W		$XXXXXXXX_B$
007914_H	Reload Register LA	PRLLA	R/W	16-bit PPGA/PPGB	$XXXXXXXX_B$
007915_H	Reload Register HA	PRLHA	R/W		$XXXXXXXX_B$
007916_H	Reload Register LB	PRLLB	R/W		$XXXXXXXX_B$
007917_H	Reload Register HB	PRLHB	R/W		$XXXXXXXX_B$
007918_H	Reload Register LC	PRLLC	R/W	16-bit PPGC/PPGD	$XXXXXXXX_B$
007919_H	Reload Register HC	PRLHC	R/W		$XXXXXXXX_B$
$00791A_H$	Reload Register LD	PRLLD	R/W		$XXXXXXXX_B$
$00791B_H$	Reload Register HD	PRLHD	R/W		$XXXXXXXX_B$
$00791C_H$	Reload Register LE	PRLLE	R/W	16-bit PPGE/PPGF	$XXXXXXXX_B$
$00791D_H$	Reload Register HE	PRLHE	R/W		$XXXXXXXX_B$
$00791E_H$	Reload Register LF	PRLLF	R/W		$XXXXXXXX_B$
$00791F_H$	Reload Register HF	PRLHF	R/W		$XXXXXXXX_B$
007920_H	Input Capture 0	IPCP0	R	Input Capture 0/1*	00000000_B
007921_H	Input Capture 0	IPCP0	R		00000000_B
007922_H	Input Capture 1	IPCP1	R		00000000_B
007923_H	Input Capture 1	IPCP1	R		00000000_B
007924_H	Input Capture 2	IPCP2	R	Input Capture 2/3*	00000000_B
007925_H	Input Capture 2	IPCP2	R		00000000_B
007926_H	Input Capture 3	IPCP3	R		00000000_B
007927_H	Input Capture 3	IPCP3	R		00000000_B
007928_H	Input Capture 4	IPCP4	R	Input Capture 4/5*	00000000_B
007929_H	Input Capture 4	IPCP4	R		00000000_B
$00792A_H$	Input Capture 5	IPCP5	R		00000000_B
$00792B_H$	Input Capture 5	IPCP5	R		00000000_B
$00792C_H$	Input Capture 6	IPCP6	R	Input Capture 6/7*	00000000_B
$00792D_H$	Input Capture 6	IPCP6	R		00000000_B
$00792E_H$	Input Capture 7	IPCP7	R		00000000_B
$00792F_H$	Input Capture 7	IPCP7	R		00000000_B

* : The Initial values of CY90V950AJAS and CY90V950AMAS are $XXXXXXXX_B$.

Address	Register	Abbreviation	Access	Resource Name	Initial Value
007930_H	Output Compare 0	OCCP0	R/W	Output Compare 0/1	$XXXXXXXX_B$
007931_H	Output Compare 0	OCCP0	R/W		$XXXXXXXX_B$
007932_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007933_H	Output Compare 1	OCCP1	R/W		$XXXXXXXX_B$
007934_H	Output Compare 2	OCCP2	R/W	Output Compare 2/3	$XXXXXXXX_B$
007935_H	Output Compare 2	OCCP2	R/W		$XXXXXXXX_B$
007936_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007937_H	Output Compare 3	OCCP3	R/W		$XXXXXXXX_B$
007938_H	Output Compare 4	OCCP4	R/W	Output Compare 4/5	$XXXXXXXX_B$
007939_H	Output Compare 4	OCCP4	R/W		$XXXXXXXX_B$
$00793A_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793B_H$	Output Compare 5	OCCP5	R/W		$XXXXXXXX_B$
$00793C_H$	Output Compare 6	OCCP6	R/W	Output Compare 6/7	$XXXXXXXX_B$
$00793D_H$	Output Compare 6	OCCP6	R/W		$XXXXXXXX_B$
$00793E_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
$00793F_H$	Output Compare 7	OCCP7	R/W		$XXXXXXXX_B$
007940_H	Timer Data 0	TCDT0	R/W	I/O Timer 0	00000000_B
007941_H	Timer Data 0	TCDT0	R/W		00000000_B
007942_H	Timer Control Status 0	TCCSL0	R/W		00000000_B
007943_H	Timer Control Status 0	TCCSH0	R/W		01100000_B
007944_H	Timer Data 1	TCDT1	R/W	I/O Timer 1	00000000_B
007945_H	Timer Data 1	TCDT1	R/W		00000000_B
007946_H	Timer Control Status 1	TCCSL1	R/W		00000000_B
007947_H	Timer Control Status 1	TCCSH1	R/W		01100000_B
007948_H	Timer 0/Reload 0	TMR0/TMRLR0	R/W	16-bit Reload Timer 0	$XXXXXXXX_B$
007949_H			R/W		$XXXXXXXX_B$
$00794A_H$	Timer 1/Reload 1	TMR1/TMRLR1	R/W	16-bit Reload Timer 1	$XXXXXXXX_B$
$00794B_H$			R/W		$XXXXXXXX_B$
$00794C_H$	Timer 2/Reload 2	TMR2/TMRLR2	R/W	16-bit Reload Timer 2	$XXXXXXXX_B$
$00794D_H$			R/W		$XXXXXXXX_B$
$00794E_H$	Timer 3/Reload 3	TMR3/TMRLR3	R/W	16-bit Reload Timer 3	$XXXXXXXX_B$
$00794F_H$			R/W		$XXXXXXXX_B$
007950_H	Serial Mode Register 3	SMR3	W, R/W	UART3	00000000_B
007951_H	Serial Control Register 3	SCR3	W, R/W		00000000_B
007952_H	Reception/Transmission Data Register 3	RDR3/TDR3	R/W		00000000_B/ 11111111_B
007953_H	Serial Status Register 3	SSR3	R, R/W		00001000_B
007954_H	Extended Communication Control Register 3	ECCR3	R, W, R/W		$000000XX_B$
007955_H	Extended Status Control Register 3	ESCR3	R/W		$00000X00_B$
007956_H	Baud Rate Generator Register 30	BGR30	R, R/W		00000000_B
007957_H	Baud Rate Generator Register 31	BGR31	R, R/W		00000000_B

Address	Register	Abbreviation	Access	Resource Name	Initial Value
007958_H	Serial Mode Register 4	SMR4	W, R/W	UART4	00000000_B
007959_H	Serial Control Register 4	SCR4	W, R/W		00000000_B
$00795A_H$	Reception/Transmission Data Register 4	RDR4/TDR4	R/W		00000000_B/ 11111111_B
$00795B_H$	Serial Status Register 4	SSR4	R, R/W		00001000_B
$00795C_H$	Extended Communication Control Register 4	ECCR4	R, W, R/W		$000000XX_B$
$00795D_H$	Extended Status Control Register 4	ESCR4	R/W		$00000X00_B$
$00795E_H$	Baud Rate Generator Register 40	BGR40	R, R/W		00000000_B
$00795F_H$	Baud Rate Generator Register 41	BGR41	R, R/W		00000000_B
007960_H	Clock Supervisor Control Register	CSVCR	R/W	Clock Supervisor	00011100_B
007961_H to $00796B_H$	Reserved				
$00796C_H$	Clock Output Enable Register	CLKR	R/W	Clock Monitor	11110000_B
$00796D_H$	Reserved				
$00796E_H$	CAN Direct Mode Register	CDMR	R/W	CAN Clock Sync	11111110_B
$00796F_H$	CAN Switch Register	CANSWR	R/W	CAN 0/1	11111100_B
007970_H	I^2C Bus Status Register 0	IBSR0	R	I^2C Interface 0	00000000_B
007971_H	I^2C Bus Control Register 0	IBCR0	W, R/W		00000000_B
007972_H	I^2C 10-bit Slave Address Register 0	ITBAL0	R/W		00000000_B
007973_H		ITBAH0	R/W		00000000_B
007974_H	I^2C 10-bit Slave Address Mask Register 0	ITMKL0	R/W		11111111_B
007975_H		ITMKH0	R/W		00111111_B
007976_H	I^2C 7-bit Slave Address Register 0	ISBA0	R/W		00000000_B
007977_H	I^2C 7-bit Slave Address Mask Register 0	ISMK0	R/W		01111111_B
007978_H	I^2C Data Register 0	IDAR0	R/W		00000000_B
007979_H, $00797A_H$	Reserved				
$00797B_H$	I^2C Clock Control Register 0	ICCR0	R/W	I^2C Interface 0	00011111_B
$00797C_H$ to $00797F_H$	Reserved				
007980_H	I^2C Bus Status Register 1	IBSR1	R	I^2C Interface 1	00000000_B
007981_H	I^2C Bus Control Register 1	IBCR1	W, R/W		00000000_B
007982_H	I^2C 10-bit Slave Address Register 1	ITBAL1	R/W		00000000_B
007983_H		ITBAH1	R/W		00000000_B
007984_H	I^2C 10-bit Slave Address Mask Register 1	ITMKL1	R/W		11111111_B
007985_H		ITMKH1	R/W		00111111_B
007986_H	I^2C 7-bit Slave Address Register 1	ISBA1	R/W		00000000_B
007987_H	I^2C 7-bit Slave Address Mask Register 1	ISMK1	R/W		01111111_B
007988_H	I^2C Data Register 1	IDAR1	R/W		00000000_B
007989_H, $00798A_H$	Reserved				

Address	Register	Abbreviation	Access	Resource Name	Initial Value
$00798B_H$	I^2C Clock Control Register 1	ICCR1	R/W	I^2C Interface1	00011111_B
$00798C_H$ to $00798F_H$	Reserved				
007990_H	Serial Mode Register 5	SMR5	W, R/W	UART5	00000000_B
007991_H	Serial Control Register 5	SCR5	W, R/W		00000000_B
007992_H	Reception/Transmission Data Register 5	RDR5/TDR5	R/W		00000000_B/ 11111111_B
007993_H	Serial Status Register 5	SSR5	R, R/W		00001000_B
007994_H	Extended Communication Control Register 5	ECCR5	R, W, R/W		$000000XX_B$
007995_H	Extended Status Control Register 5	ESCR5	R/W		$00000X00_B$
007996_H	Baud Rate Generator Register 50	BGR50	R, R/W		00000000_B
007997_H	Baud Rate Generator Register 51	BGR51	R, R/W		00000000_B
007998_H	Serial Mode Register 6	SMR6	W, R/W	UART6	00000000_B
007999_H	Serial Control Register 6	SCR6	W, R/W		00000000_B
$00799A_H$	Reception/Transmission Data Register 6	RDR6/TDR6	R/W		00000000_B/ 11111111_B
$00799B_H$	Serial Status Register 6	SSR6	R, R/W		00001000_B
$00799C_H$	Extended Communication Control Register 6	ECCR6	R, W, R/W		$000000XX_B$
$00799D_H$	Extended Status Control Register 6	ESCR6	R/W		$00000X00_B$
$00799E_H$	Baud Rate Generator Register 60	BGR60	R, R/W		00000000_B
$00799F_H$	Baud Rate Generator Register 61	BGR61	R, R/W		00000000_B
$0079A0_H$	UART Input Level Setting Register	ILSR2	R/W	UART	11111100_B
$0079A1_H$	Reserved				
$0079A2_H$	Flash Write Control Register 0	FWR0	R/W	Flash Memory	00000000_B
$0079A3_H$	Flash Write Control Register 1	FWR1	R/W	Flash Memory	00000000_B
$0079A4_H$ to $0079B1_H$	Reserved				
$0079B2_H$	Low Voltage/CPU Operation Detection Setting Register	LVRS	R/W	Low Voltage/ CPU Operation Detection Reset	10000111_B
$0079B3_H$ to $0079B7_H$	Reserved				
$0079B8_H$	Clock Calibration Unit Control	CUCR	R/W	Clock Calibration Unit	00000000_B
$0079B9_H$	CR Oscillation Trimming Setting	CRTR	R/W		11110111_B
$0079BA_H$	CR Oscillation Timer Data Register	CUTDL	R/W		01010000_B
$0079BB_H$		CUTDH	R/W		11000011_B
$0079BC_H$	Main Timer Data Register 1	CUTR1L	R		00000000_B
$0079BD_H$		CUTR1H	R		00000000_B
$0079BE_H$	Main Timer Data Register 2	CUTR2L	R		00000000_B
$0079BF_H$		CUTR2H	R		00000000_B
$0079C0_H$ to $0079DF_H$	Reserved				

Address	Register	Abbreviation	Access	Resource Name	Initial Value
$0079E0_H$	Detect Address Setting 0	PADR0	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E1_H$	Detect Address Setting 0	PADR0	R/W		$XXXXXXXX_B$
$0079E2_H$	Detect Address Setting 0	PADR0	R/W		$XXXXXXXX_B$
$0079E3_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E4_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E5_H$	Detect Address Setting 1	PADR1	R/W		$XXXXXXXX_B$
$0079E6_H$	Detect Address Setting 2	PADR2	R/W	Address Match Detection 0	$XXXXXXXX_B$
$0079E7_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E8_H$	Detect Address Setting 2	PADR2	R/W		$XXXXXXXX_B$
$0079E9_H$ to $0079EF_H$	Reserved				
$0079F0_H$	Detect Address Setting 3	PADR3	R/W	Address Match Detection 1	$XXXXXXXX_B$
$0079F1_H$	Detect Address Setting 3	PADR3	R/W		$XXXXXXXX_B$
$0079F2_H$	Detect Address Setting 3	PADR3	R/W		$XXXXXXXX_B$
$0079F3_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F4_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F5_H$	Detect Address Setting 4	PADR4	R/W		$XXXXXXXX_B$
$0079F6_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F7_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F8_H$	Detect Address Setting 5	PADR5	R/W		$XXXXXXXX_B$
$0079F9_H$ to $0079FF_H$	Reserved				
$007A00_H$ to $007AFF_H$	Reserved for CAN Controller 0. Refer to "CAN Controllers"				
$007B00_H$ to $007BFF_H$	Reserved for CAN Controller 0. Refer to "CAN Controllers""				
$007C00_H$ to $007CFF_H$	Reserved for CAN Controller 1. Refer to "CAN Controllers""				
$007D00_H$ to $007DFF_H$	Reserved for CAN Controller 1. Refer to "CAN Controllers""				
$007E00_H$ to $007EFF_H$	Reserved for CAN Controller 2. Refer to "CAN Controllers""				
$007F00_H$ to $007FFF_H$	Reserved for CAN Controller 2. Refer to "CAN Controllers""				

Notes :
- Initial value of "X" represents unknown value.
- Any write access to reserved addresses in I/O map should not be performed. A read access to reserved addresses results in reading "X".

9. CAN Controllers

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
  29-bit ID and 8-byte data
  Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)
- **List of Control Registers** (**1**)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
000070_H	000080_H	$0000E0_H$	Message Buffer Valid Register	BVALR	R/W	00000000_B 00000000_B
000071_H	000081_H	$0000E1_H$				
000072_H	000082_H	$0000E2_H$	Transmit Request Register	TREQR	R/W	00000000_B 00000000_B
000073_H	000083_H	$0000E3_H$				
000074_H	000084_H	$0000E4_H$	Transmit Cancel Register	TCANR	W	00000000_B 00000000_B
000075_H	000085_H	$0000E5_H$				
000076_H	000086_H	$0000E6_H$	Transmission Complete Register	TCR	R/W	00000000_B 00000000_B
000077_H	000087_H	$0000E7_H$				
000078_H	000088_H	$0000E8_H$	Receive Complete Register	RCR	R/W	00000000_B 00000000_B
000079_H	000089_H	$0000E9_H$				
$00007A_H$	$00008A_H$	$0000EA_H$	Remote Request Receiving Register	RRTRR	R/W	00000000_B 00000000_B
$00007B_H$	$00008B_H$	$0000EB_H$				
$00007C_H$	$00008C_H$	$0000EC_H$	Receive Overrun Register	ROVRR	R/W	00000000_B 00000000_B
$00007D_H$	$00008D_H$	$0000ED_H$				
$00007E_H$	$00008E_H$	$0000EE_H$	Reception Interrupt Enable Register	RIER	R/W	00000000_B 00000000_B
$00007F_H$	$00008F_H$	$0000EF_H$				

■ **List of Control Registers (2)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
$007B00_H$	$007D00_H$	$007F00_H$	Control Status Register	CSR	R/W, W R/W, R	$0XXXX0X1_B$ $00XXX000_B$
$007B01_H$	$007D01_H$	$007F01_H$				
$007B02_H$	$007D02_H$	$007F02_H$	Last Event Indicator Register	LEIR	R/W	$000X0000_B$ $XXXXXXXX_B$
$007B03_H$	$007D03_H$	$007F03_H$				
$007B04_H$	$007D04_H$	$007F04_H$	Receive And Transmit Error Counter	RTEC	R	00000000_B 00000000_B
$007B05_H$	$007D05_H$	$007F05_H$				
$007B06_H$	$007D06_H$	$007F06_H$	Bit Timing Register	BTR	R/W	11111111_B $X1111111_B$
$007B07_H$	$007D07_H$	$007F07_H$				
$007B08_H$	$007D08_H$	$007F08_H$	IDE Register	IDER	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B09_H$	$007D09_H$	$007F09_H$				
$007B0A_H$	$007D0A_H$	$007F0A_H$	Transmit RTR Register	TRTRR	R/W	00000000_B 00000000_B
$007B0B_H$	$007D0B_H$	$007F0B_H$				
$007B0C_H$	$007D0C_H$	$007F0C_H$	Remote Frame Receive Waiting Register	RFWTR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B0D_H$	$007D0D_H$	$007F0D_H$				
$007B0E_H$	$007D0E_H$	$007F0E_H$	Transmit Interrupt Enable Register	TIER	R/W	00000000_B 00000000_B
$007B0F_H$	$007D0F_H$	$007F0F_H$				
$007B10_H$	$007D10_H$	$007F10_H$	Acceptance Mask Select Register	AMSR	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B11_H$	$007D11_H$	$007F11_H$				
$007B12_H$	$007D12_H$	$007F12_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B13_H$	$007D13_H$	$007F13_H$				
$007B14_H$	$007D14_H$	$007F14_H$	Acceptance Mask Register 0	AMR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B15_H$	$007D15_H$	$007F15_H$				
$007B16_H$	$007D16_H$	$007F16_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B17_H$	$007D17_H$	$007F17_H$				
$007B18_H$	$007D18_H$	$007F18_H$	Acceptance Mask Register 1	AMR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007B19_H$	$007D19_H$	$007F19_H$				
$007B1A_H$	$007D1A_H$	$007F1A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007B1B_H$	$007D1B_H$	$007F1B_H$				

■ List of Message Buffers (ID Registers) (1)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
$007A00_H$ to $007A1F_H$	$007C00_H$ to $007C1F_H$	$007E00_H$ to $007E1F_H$	General-Purpose Ram	—	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A20_H$	$007C20_H$	$007E20_H$	ID Register 0	IDR0	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A21_H$	$007C21_H$	$007E21_H$				
$007A22_H$	$007C22_H$	$007E22_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A23_H$	$007C23_H$	$007E23_H$				
$007A24_H$	$007C24_H$	$007E24_H$	ID Register 1	IDR1	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A25_H$	$007C25_H$	$007E25_H$				
$007A26_H$	$007C26_H$	$007E26_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A27_H$	$007C27_H$	$007E27_H$				
$007A28_H$	$007C28_H$	$007E28_H$	ID Register 2	IDR2	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A29_H$	$007C29_H$	$007E29_H$				
$007A2A_H$	$007C2A_H$	$007E2A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2B_H$	$007C2B_H$	$007E2B_H$				
$007A2C_H$	$007C2C_H$	$007E2C_H$	ID Register 3	IDR3	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2D_H$	$007C2D_H$	$007E2D_H$				
$007A2E_H$	$007C2E_H$	$007E2E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A2F_H$	$007C2F_H$	$007E2F_H$				
$007A30_H$	$007C30_H$	$007E30_H$	ID Register 4	IDR4	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A31_H$	$007C31_H$	$007E31_H$				
$007A32_H$	$007C32_H$	$007E32_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A33_H$	$007C33_H$	$007E33_H$				
$007A34_H$	$007C34_H$	$007E34_H$	ID Register 5	IDR5	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A35_H$	$007C35_H$	$007E35_H$				
$007A36_H$	$007C36_H$	$007E36_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A37_H$	$007C37_H$	$007E37_H$				
$007A38_H$	$007C38_H$	$007E38_H$	ID Register 6	IDR6	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A39_H$	$007C39_H$	$007E39_H$				
$007A3A_H$	$007C3A_H$	$007E3A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3B_H$	$007C3B_H$	$007E3B_H$				
$007A3C_H$	$007C3C_H$	$007E3C_H$	ID Register 7	IDR7	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3D_H$	$007C3D_H$	$007E3D_H$				
$007A3E_H$	$007C3E_H$	$007E3E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A3F_H$	$007C3F_H$	$007E3F_H$				

■ List of Message Buffers (ID Registers) (2)

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
$007A40_H$	$007C40_H$	$007E40_H$	ID Register 8	IDR8	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A41_H$	$007C41_H$	$007E41_H$				
$007A42_H$	$007C42_H$	$007E42_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A43_H$	$007C43_H$	$007E43_H$				
$007A44_H$	$007C44_H$	$007E44_H$	ID Register 9	IDR9	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A45_H$	$007C45_H$	$007E45_H$				
$007A46_H$	$007C46_H$	$007E46_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A47_H$	$007C47_H$	$007E47_H$				
$007A48_H$	$007C48_H$	$007E48_H$	ID Register 10	IDR10	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A49_H$	$007C49_H$	$007E49_H$				
$007A4A_H$	$007C4A_H$	$007E4A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4B_H$	$007C4B_H$	$007E4B_H$				
$007A4C_H$	$007C4C_H$	$007E4C_H$	ID Register 11	IDR11	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4D_H$	$007C4D_H$	$007E4D_H$				
$007A4E_H$	$007C4E_H$	$007E4E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A4F_H$	$007C4F_H$	$007E4F_H$				
$007A50_H$	$007C50_H$	$007E50_H$	ID Register 12	IDR12	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A51_H$	$007C51_H$	$007E51_H$				
$007A52_H$	$007C52_H$	$007E52_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A53_H$	$007C53_H$	$007E53_H$				
$007A54_H$	$007C54_H$	$007E54_H$	ID Register 13	IDR13	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A55_H$	$007C55_H$	$007E55_H$				
$007A56_H$	$007C56_H$	$007E56_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A57_H$	$007C57_H$	$007E57_H$				
$007A58_H$	$007C58_H$	$007E58_H$	ID Register 14	IDR14	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A59_H$	$007C59_H$	$007E59_H$				
$007A5A_H$	$007C5A_H$	$007E5A_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5B_H$	$007C5B_H$	$007E5B_H$				
$007A5C_H$	$007C5C_H$	$007E5C_H$	ID Register 15	IDR15	R/W	$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5D_H$	$007C5D_H$	$007E5D_H$				
$007A5E_H$	$007C5E_H$	$007E5E_H$				$XXXXXXXX_B$ $XXXXXXXX_B$
$007A5F_H$	$007C5F_H$	$007E5F_H$				

■ **List of Message Buffers (DLC Registers and Data Registers) (1)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
$007A60_H$	$007C60_H$	$007E60_H$	DLC Register 0	DLCR0	R/W	$XXXXXXXX_B$
$007A61_H$	$007C61_H$	$007E61_H$				
$007A62_H$	$007C62_H$	$007E62_H$	DLC Register 1	DLCR1	R/W	$XXXXXXXX_B$
$007A63_H$	$007C63_H$	$007E63_H$				
$007A64_H$	$007C64_H$	$007E64_H$	DLC Register 2	DLCR2	R/W	$XXXXXXXX_B$
$007A65_H$	$007C65_H$	$007E65_H$				
$007A66_H$	$007C66_H$	$007E66_H$	DLC Register 3	DLCR3	R/W	$XXXXXXXX_B$
$007A67_H$	$007C67_H$	$007E67_H$				
$007A68_H$	$007C68_H$	$007E68_H$	DLC Register 4	DLCR4	R/W	$XXXXXXXX_B$
$007A69_H$	$007C69_H$	$007E69_H$				
$007A6A_H$	$007C6A_H$	$007E6A_H$	DLC Register 5	DLCR5	R/W	$XXXXXXXX_B$
$007A6B_H$	$007C6B_H$	$007E6B_H$				
$007A6C_H$	$007C6C_H$	$007E6C_H$	DLC Register 6	DLCR6	R/W	$XXXXXXXX_B$
$007A6D_H$	$007C6D_H$	$007E6D_H$				
$007A6E_H$	$007C6E_H$	$007E6E_H$	DLC Register 7	DLCR7	R/W	$XXXXXXXX_B$
$007A6F_H$	$007C6F_H$	$007E6F_H$				
$007A70_H$	$007C70_H$	$007E70_H$	DLC Register 8	DLCR8	R/W	$XXXXXXXX_B$
$007A71_H$	$007C71_H$	$007E71_H$				
$007A72_H$	$007C72_H$	$007E72_H$	DLC Register 9	DLCR9	R/W	$XXXXXXXX_B$
$007A73_H$	$007C73_H$	$007E73_H$				
$007A74_H$	$007C74_H$	$007E74_H$	DLC Register 10	DLCR10	R/W	$XXXXXXXX_B$
$007A75_H$	$007C75_H$	$007E75_H$				
$007A76_H$	$007C76_H$	$007E76_H$	DLC Register 11	DLCR11	R/W	$XXXXXXXX_B$
$007A77_H$	$007C77_H$	$007E77_H$				
$007A78_H$	$007C78_H$	$007E78_H$	DLC Register 12	DLCR12	R/W	$XXXXXXXX_B$
$007A79_H$	$007C79_H$	$007E79_H$				
$007A7A_H$	$007C7A_H$	$007E7A_H$	DLC Register 13	DLCR13	R/W	$XXXXXXXX_B$
$007A7B_H$	$007C7B_H$	$007E7B_H$				
$007A7C_H$	$007C7C_H$	$007E7C_H$	DLC Register 14	DLCR14	R/W	$XXXXXXXX_B$
$007A7D_H$	$007C7D_H$	$007E7D_H$				
$007A7E_H$	$007C7E_H$	$007E7E_H$	DLC Register 15	DLCR15	R/W	$XXXXXXXX_B$
$007A7F_H$	$007C7F_H$	$007E7F_H$				

■ **List of Message Buffers (DLC Registers and Data Registers) (2)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
$007A80_H$ to $007A87_H$	$007C80_H$ to $007C87_H$	$007E80_H$ to $007E87_H$	Data Register 0 (8 bytes)	DTR0	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A88_H$ to $007A8F_H$	$007C88_H$ to $007C8F_H$	$007E88_H$ to $007E8F_H$	Data Register 1 (8 bytes)	DTR1	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A90_H$ to $007A97_H$	$007C90_H$ to $007C97_H$	$007E90_H$ to $007E97_H$	Data Register 2 (8 bytes)	DTR2	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007A98_H$ to $007A9F_H$	$007C98_H$ to $007C9F_H$	$007E98_H$ to $007E9F_H$	Data Register 3 (8 bytes)	DTR3	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AA0_H$ to $007AA7_H$	$007CA0_H$ to $007CA7_H$	$007EA0_H$ to $007EA7_H$	Data Register 4 (8 bytes)	DTR4	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AA8_H$ to $007AAF_H$	$007CA8_H$ to $007CAF_H$	$007EA8_H$ to $007EAF_H$	Data Register 5 (8 bytes)	DTR5	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AB0_H$ to $007AB7_H$	$007CB0_H$ to $007CB7_H$	$007EB0_H$ to $007EB7_H$	Data Register 6 (8 bytes)	DTR6	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AB8_H$ to $007ABF_H$	$007CB8_H$ to $007CBF_H$	$007EB8_H$ to $007EBF_H$	Data Register 7 (8 bytes)	DTR7	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AC0_H$ to $007AC7_H$	$007CC0_H$ to $007CC7_H$	$007EC0_H$ to $007EC7_H$	Data Register 8 (8 bytes)	DTR8	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AC8_H$ to $007ACF_H$	$007CC8_H$ to $007CCF_H$	$007EC8_H$ to $007ECF_H$	Data Register 9 (8 bytes)	DTR9	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AD0_H$ to $007AD7_H$	$007CD0_H$ to $007CD7_H$	$007ED0_H$ to $007ED7_H$	Data Register 10 (8 bytes)	DTR10	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AD8_H$ to $007ADF_H$	$007CD8_H$ to $007CDF_H$	$007ED8_H$ to $007EDF_H$	Data Register 11 (8 bytes)	DTR11	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AE0_H$ to $007AE7_H$	$007CE0_H$ to $007CE7_H$	$007EE0_H$ to $007EE7_H$	Data Register 12 (8 bytes)	DTR12	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AE8_H$ to $007AEF_H$	$007CE8_H$ to $007CEF_H$	$007EE8_H$ to $007EEF_H$	Data Register 13 (8 bytes)	DTR13	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

■ **List of Message Buffers (DLC Registers and Data Registers) (3)**

Address			Register	Abbreviation	Access	Initial Value
CAN0	CAN1	CAN2				
$007AF0_H$ to $007AF7_H$	$007CF0_H$ to $007CF7_H$	$007EF0_H$ to $007EF7_H$	Data Register 14 (8 bytes)	DTR14	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$
$007AF8_H$ to $007AFF_H$	$007CF8_H$ to $007CFF_H$	$007EF8_H$ to $007EFF_H$	Data Register 15 (8 bytes)	DTR15	R/W	$XXXXXXXX_B$ to $XXXXXXXX_B$

10. Interrupt Factors, Interrupt Vectors, Interrupt Control Register

Interrupt Cause	EI^{2}OS Support	DMA Channel Number	Interrupt Vector		Interrupt Control Register	
			Number	Address	Number	Address
Reset	N	—	#08	FFFFDC$_H$	—	—
INT9 instruction	N	—	#09	FFFFD8$_H$	—	—
Exception	N	—	#10	FFFFD4$_H$	—	—
CAN0 RX	N	—	#11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN0 TX/NS	N	—	#12	FFFFCC$_H$		
CAN1 RX/Input Capture 6	Y1	—	#13	FFFFC8$_H$	ICR01	0000B1$_H$
CAN1 TX/NS/Input Capture 7	Y1	—	#14	FFFFC4$_H$		
CAN2 RX / I^{2}C0	N	—	#15	FFFFC0$_H$	ICR02	0000B2$_H$
CAN2 TX / NS / Clock Calibration Unit	N	—	#16	FFFFBC$_H$		
16-bit Reload Timer 0	Y1	0	#17	FFFFB8$_H$	ICR03	0000B3$_H$
16-bit Reload Timer 1	Y1	1	#18	FFFFB4$_H$		
16-bit Reload Timer 2	Y1	2	#19	FFFFB0$_H$	ICR04	0000B4$_H$
16-bit Reload Timer 3	Y1	—	#20	FFFFAC$_H$		
PPG0 / PPG1 / PPG4 / PPG5	N	—	#21	FFFFA8$_H$	ICR05	0000B5$_H$
PPG2 / PPG3 / PPG6 / PPG7	N	—	#22	FFFFA4$_H$		
PPG8 / PPG9 / PPGC / PPGD	N	—	#23	FFFFA0$_H$	ICR06	0000B6$_H$
PPGA / PPGB / PPGE / PPGF	N	—	#24	FFFF9C$_H$		
Time Base Timer	N	—	#25	FFFF98$_H$	ICR07	0000B7$_H$
External Interrupt 0 to 3, 8 to 11	Y1	3	#26	FFFF94$_H$		
Watch Timer	N	—	#27	FFFF90$_H$	ICR08	0000B8$_H$
External Interrupt 4 to 7, 12 to 15	Y1	4	#28	FFFF8C$_H$		
A/D Converter	Y1	5	#29	FFFF88$_H$	ICR09	0000B9$_H$
I/O Timer 0/1	N	—	#30	FFFF84$_H$		
Input Capture 4/5 / I^{2}C1	Y1	6	#31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 0/1/4/5	Y1	7	#32	FFFF7C$_H$		
Input Capture 0 to 3	Y1	8	#33	FFFF78$_H$	ICR11	0000BB$_H$
Output Compare 2/3/6/7	Y1	9	#34	FFFF74$_H$		
UART0 RX	Y2	10	#35	FFFF70$_H$	ICR12	0000BC$_H$
UART0 TX	Y1	11	#36	FFFF6C$_H$		
UART1 RX / UART3 RX / UART5 RX	Y2	12	#37	FFFF68$_H$	ICR13	0000BD$_H$
UART1 TX / UART3 TX / UART5 TX	Y1	13	#38	FFFF64$_H$		
UART2 RX / UART4 RX / UART6 RX	Y2	14	#39	FFFF60$_H$	ICR14	0000BE$_H$
UART2 TX / UART4 TX / UART6 TX	Y1	15	#40	FFFF5C$_H$		
Flash Memory	N	—	#41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed Interrupt	N	—	#42	FFFF54$_H$		

Y1 : Usable
Y2 : Usable, with EI^{2}OS stop function
N : Unusable

Notes :
- The peripheral resources sharing the ICR register have the same interrupt level.
- When two peripheral resources share the ICR register, only one can use Extended Intelligent I/O Service at a time.
- When either of the two peripheral resources sharing the ICR register specifies Extended Intelligent I/O Service, the other one cannot use interrupts.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH ≥ AVRL
Input voltage*1	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*3
Maximum Clamp Current	I_{CLAMP}	−4.0	+4.0	mA	*5
Total Maximum Clamp Current	$\Sigma\lvert I_{CLAMP}\rvert$	—	40	mA	*5
“L” level maximum output current	I_{OL}	—	15	mA	*4
“L” level average output current	I_{OLAV}	—	4	mA	*4
“L” level maximum overall output current	ΣI_{OL}	—	100	mA	*4
“L” level average overall output current	ΣI_{OLAV}	—	50	mA	*4
“H” level maximum output current	I_{OH}	—	−15	mA	*4
“H” level average output current	I_{OHAV}	—	−4	mA	*4
“H” level maximum overall output current	ΣI_{OH}	—	−100	mA	*4
“H” level average overall output current	ΣI_{OHAV}	—	−50	mA	*4
Power consumption	P_D	—	430	mW	
Operating temperature	T_A	−40	+105	°C	
		−40	+125	°C	*6
Storage temperature	T_{STG}	−55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS} = 0$ V

*2: Set AV_{CC} and V_{CC} to the same voltage. Make sure that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3 V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*4: Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0, PA1

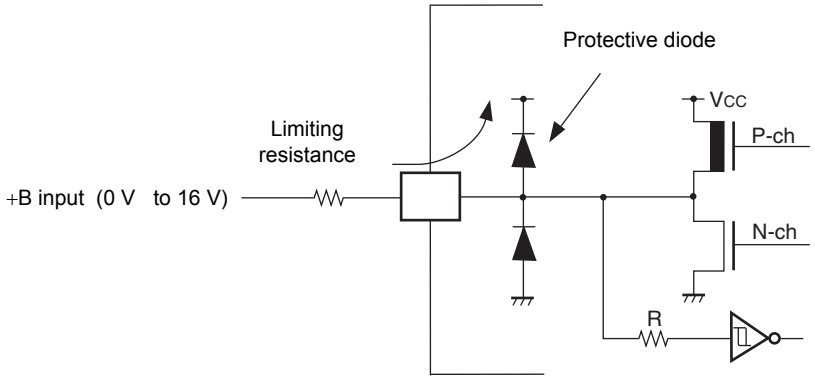
(Continued)

(Continued)

*5: ● Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47,
P50 to P55, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA1

- Use within recommended operating conditions.
- Use with DC voltage (current)
- The +B signal should always be applied by using a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed the rated value, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Sample recommended circuits:

• Input/output equivalent circuits



*6 : If used exceeding T_A = + 105°C, please consult with us due to the restricted reliability.
It is ensured to write/erase data to the Flash memory between T_A = − 40°C and + 105°C.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

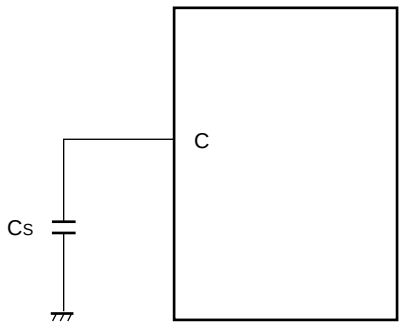
11.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Condi-tions	Value			Unit	Remarks
			Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	—	3.0	5.0	5.5	V	Under normal operation
			4.5	5.0	5.5	V	When External bus is used.
			3.0	—	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor	C_S	—	0.1	—	1.0	µF	Use a ceramic capacitor or capacitor of better AC characteristics. Capacitor at the V_{CC} should be greater than this capacitor.
Operating temperature	T_A	—	–40	—	+105	°C	CY90F952JDS, CY90F952MDS
			–40	—	+125		*

* : If used exceeding T_A = + 105°C, please consult with us due to the restricted reliability.
It is ensured to write/erase data to the Flash memory between T_A = – 40°C and + 105°C.

C Pin Connection Diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

11.3 DC Characteristics

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage (At V_{CC} = 5 V ± 10%)	V_{IHS}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected
	V_{IHA}	—	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if Automotive input levels are selected
	V_{IHT}	—	—	2.0	—	V_{CC} + 0.3	V	Port inputs if TTL input levels are selected
	V_{IHS}	P12,P15, P44 to P47, P50,P82, P85,P90, P94	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Port inputs if CMOS hysteresis input levels are selected
	V_{IHR}	$\overline{RST}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{IHM}	MD0 to MD2	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	MD input pins
Input L voltage (At V_{CC} = 5 V ± 10%)	V_{ILS}	—	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected
	V_{ILA}	—	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	Port inputs if Automotive input levels are selected
	V_{ILT}	—	—	V_{SS} – 0.3	—	0.8	V	Port inputs if TTL input levels are selected
	V_{ILS}	P12,P15, P44 to P47, P50,P82, P85,P90, P94	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Port inputs if CMOS hysteresis input levels are selected
	V_{ILR}	$\overline{RST}$	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	$\overline{RST}$ input pin (CMOS hysteresis)
	V_{ILM}	MD0 to MD2	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	MD input pins
Output H voltage	V_{OH}	Normal outputs	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
Output H voltage	V_{OHI}	I^2C outputs	V_{CC} = 4.5 V, I_{OH} = –3.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL}	Normal outputs	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
Output L voltage	V_{OLI}	I^2C outputs	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	—	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–1	—	+1	µA	
Pull-up resistance	R_{UP}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, $\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	Except Flash memory devices

Parameter	Sym-bol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internal frequency : 32 MHz, At normal operation.	—	40	50	mA	
			V_{CC} = 5.0 V, Internal frequency : 32 MHz, At writing Flash memory/erasing.	—	50	65	mA	CY90F952JDS, CY90F952MDS
	I_{CCS}		V_{CC} = 5.0 V, Internal frequency : 32 MHz, In Sleep mode.	—	13	23	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internal frequency : 2 MHz, In Main Timer mode	—	0.4	1.0	mA	CY90F952JDS
				—	0.3	0.9		CY90F952MDS
	$I_{CTSPLL6}$		V_{CC} = 5.0 V, Internal frequency : 32 MHz, In PLL Timer mode, external frequency = 4 MHz	—	4	7	mA	
	I_{CCL}		V_{CC} = 5.0 V Internal frequency : 12.5 kHz, In CR sub operation T_A = +25°C	—	170	400	µA	CY90F952JDS
	I_{CCLS}		V_{CC} = 5.0 V Internal frequency : 12.5 kHz, In CR sub sleep T_A = +25°C	—	130	250	µA	CY90F952JDS
	I_{CCT}		V_{CC} = 5.0 V Internal frequency : 12.5 kHz, In CR watch mode T_A = +25°C	—	130	250	µA	CY90F952JDS
	I_{CCH}		V_{CC} = 5.0 V, In Stop mode, T_A = +25°C	—	70	170	µA	CY90F952JDS
				—	25	100		CY90F952MDS
Input capacitance	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}	—	—	5	15	pF	

* : The power supply current is measured with an external clock.

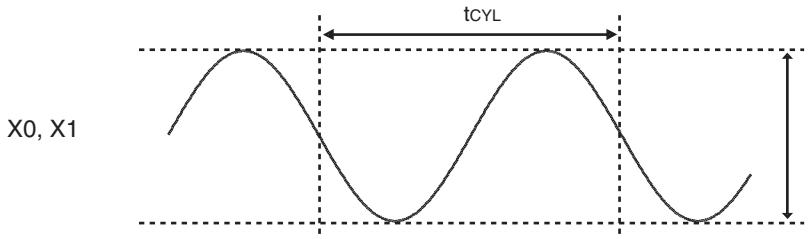
11.4 AC Characteristics

11.4.1 Clock Timing

(T_A = –40°C to +105°C, V_{CC} = 5.0 V ± 10%, f_{CP} ≤ 32 MHz, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Pin Name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	f_C	X0, X1	—	3	—	16	MHz	1/2 multiplied (PLL stopped) When using an oscillation circuit
				4		16		PLL multiplied by 1 When using an oscillation circuit
				4		16		PLL multiplied by 2 When using an oscillation circuit
				4		10		PLL multiplied by 3 When using an oscillation circuit
				4		8		PLL multiplied by 4 When using an oscillation circuit
				4		5		PLL multiplied by 6 When using an oscillation circuit
				4		4		PLL multiplied by 8 When using an oscillation circuit
Clock cycle time	t_{CYL}	X0, X1	—	62.5	—	333	ns	When using an oscillation circuit
Internal operating clock frequency (machine clock)	f_{CP}	—	—	1.5	—	32	MHz	When using main clock
	f_{CPL}	—	—	10.625	12.5	14.375	kHz	When using CR clock
Internal operating clock cycle time (machine clock)	t_{CP}	—	—	31.25	—	666	ns	When using main clock
	t_{CPL}	—	—	69.565	80	94.118	µs	When using CR clock
Internal CR oscillation frequency	f_{CCR}	—	—	85	100	115	kHz	When trimming with the clock calibration unit

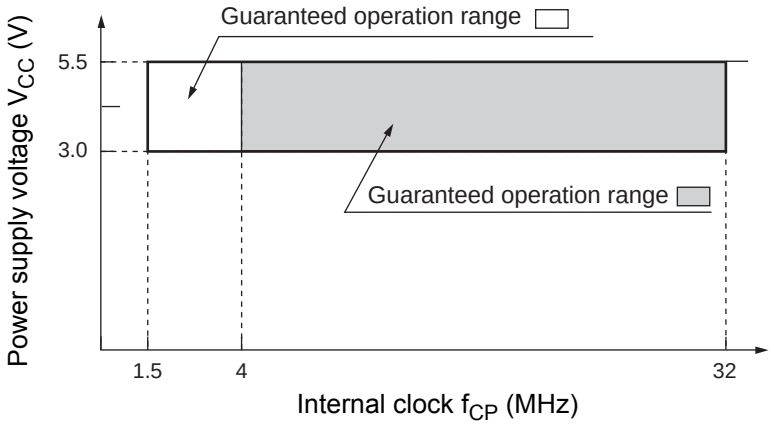
- When oscillation circuit is used



Amplitude:
It varies depending on the external resistance, power rating and the different kind of device.
Reference values: 1 V to 2.5 V

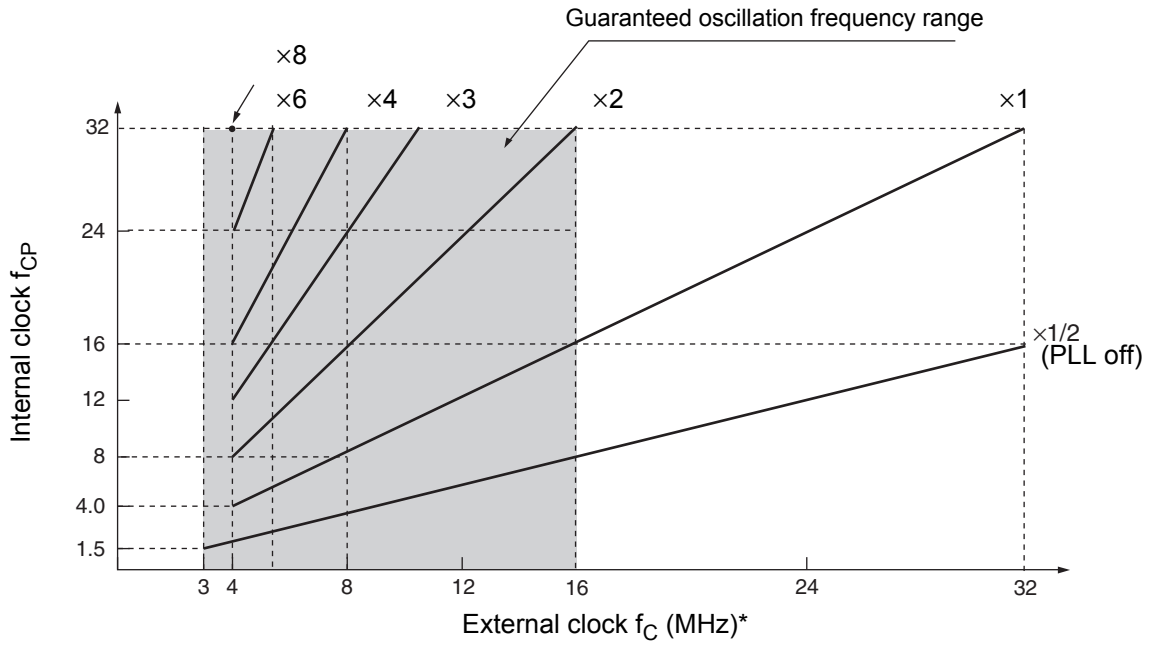
Note: The amplitude of CY90V950AJAS and CY90V950AMAS are the same as V_{CC}.

- Guaranteed PLL operation range



Note: When the power supply voltage is lower than the setting voltage of low voltage detection, CY90F952JDS are reset.

Internal clock f_{CP} – External clock f_C



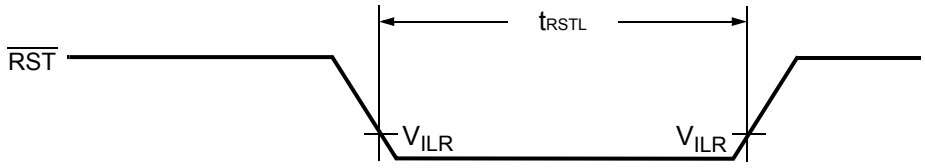
* : When using a crystal oscillator or ceramic oscillator, the maximum oscillation clock frequency is 16 MHz

11.4.2 Reset Standby Input

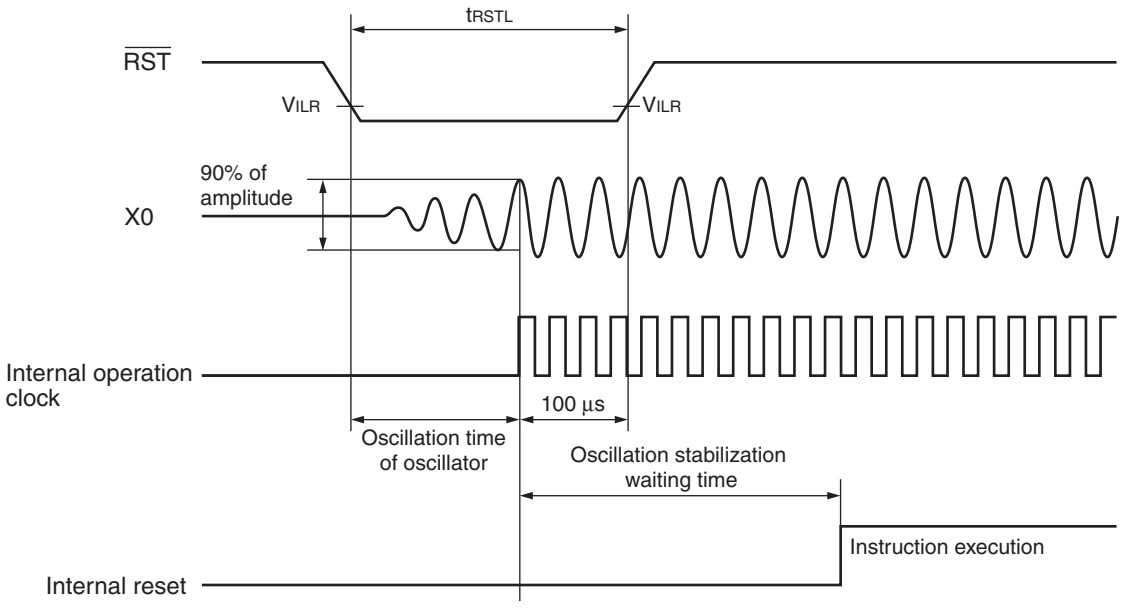
Parameter	Symbol	Pin Name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	500	—	ns	Under normal operation
				Oscillation time of oscillator* + 100 µs	—	µs	In Stop mode, Sub Clock mode, Sub Sleep mode and Watch mode
				100	—	µs	In Time Base Timer mode

* : The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

- **Under normal operation:**

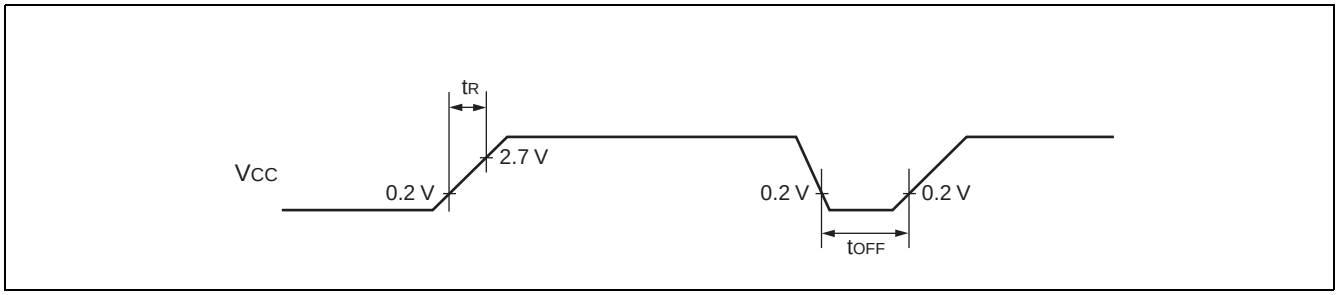


- **In Stop mode, Sub Clock mode, Sub Sleep mode, Watch mode:**

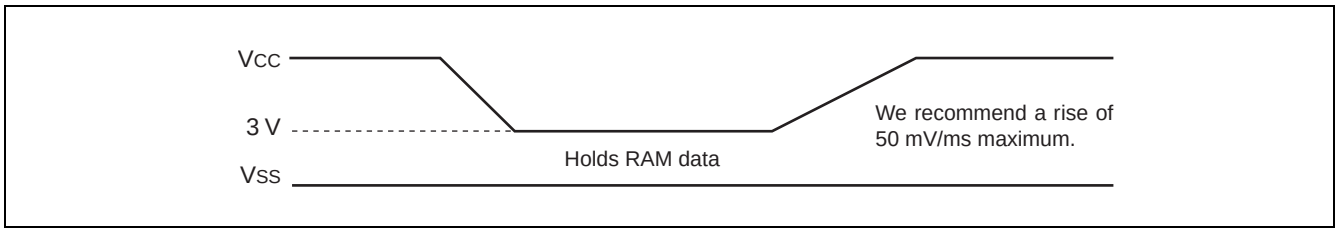


11.4.3 Power On Reset

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	
Power off time	t_{OFF}	V_{CC}		1	—	ms	Due to repetitive operation



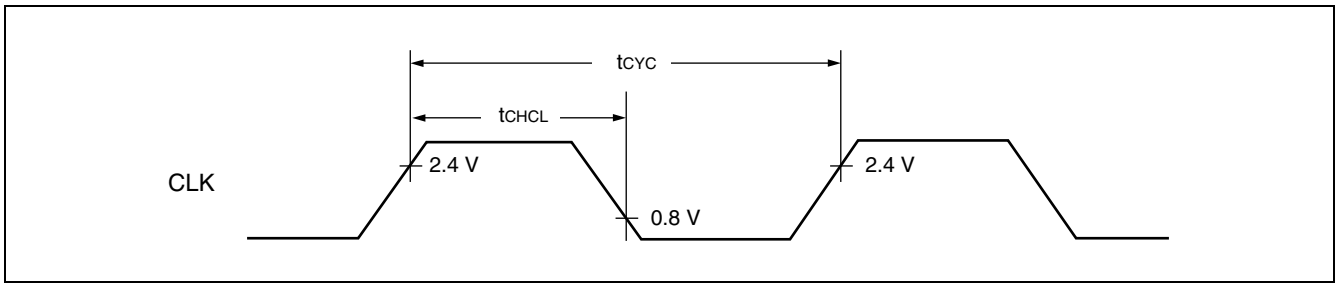
Note: If you change the power supply voltage too rapidly, a power on reset may occur. We recommend that you startup smoothly by restraining voltages when changing the power supply voltage during operation, as shown in the figure below. Perform while not using the PLL clock. However, if voltage drops are within 1 V/s, you can operate while using the PLL clock.



11.4.4 Clock Output Timing

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	CLK	—	tcp*	—	ns	
CLK ↑ → CLK ↓	t_{CHCL}	CLK	—	tcp* / 2 – 15	tcp* / 2 + 15	ns	f_{CP} = 25 MHz
				tcp* / 2 – 20	tcp* / 2 + 20	ns	f_{CP} = 16 MHz

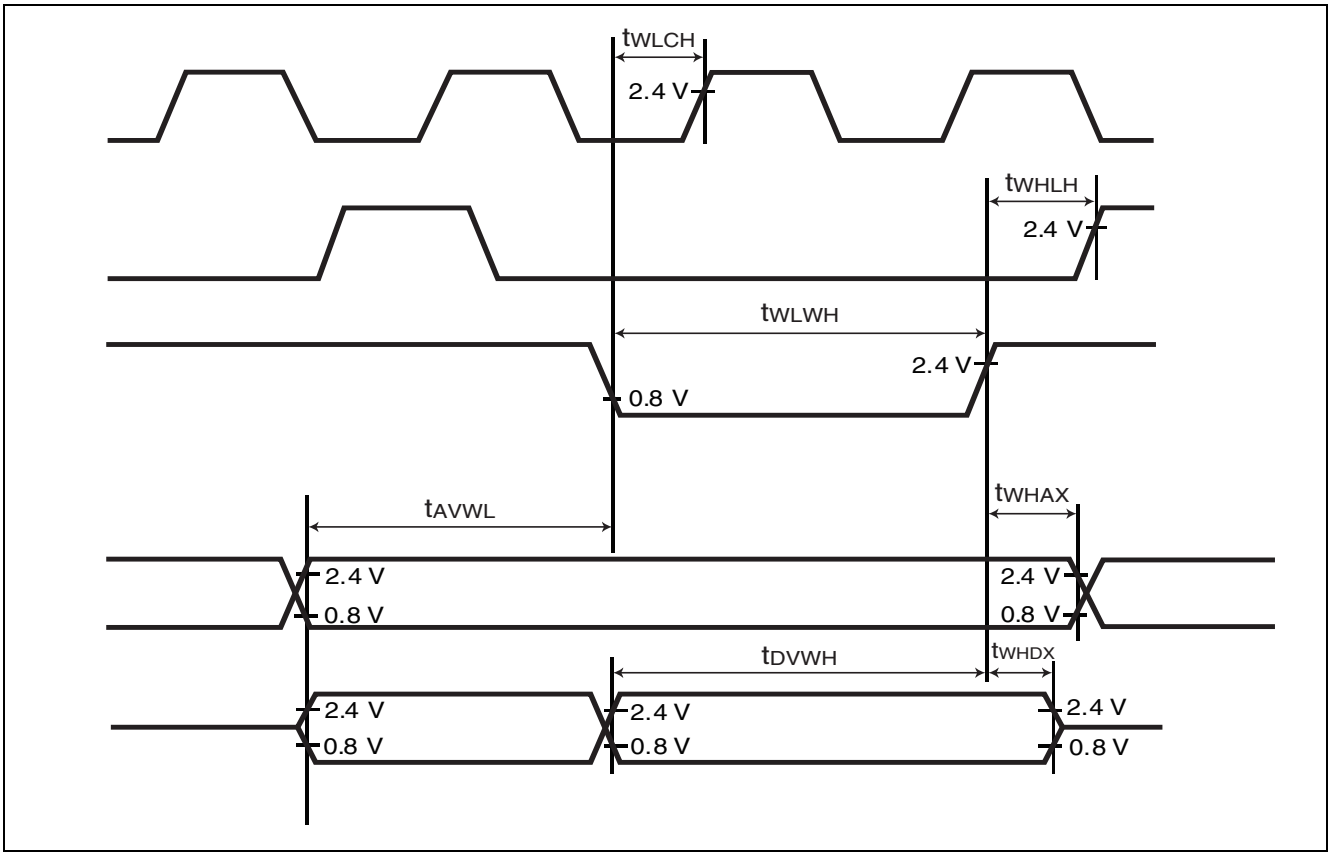
* : tcp is the Internal clock cycle time. Refer to “ (1) Clock Timing”.



11.4.5 Bus Timing (Read)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
ALE pulse width	t_{LHLL}	ALE	–	tcp*/ 2 – 15	–	ns	16MHz < fcp ≤ 25 MHz
				tcp*/ 2 – 20	–	ns	8 MHz < fcp ≤ 16 MHz
				tcp*/ 2 – 35	–	ns	fcp ≤ 8 MHz
Valid address → ALE ↓ time	t_{AVLL}	Address, ALE	–	tcp*/ 2 – 17	–	ns	
				tcp*/ 2 – 40	–	ns	fcp ≤ 8 MHz
ALE ↓ → Address valid time	t_{LLAX}	ALE , Address	–	tcp*/ 2 – 15	–	ns	
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, Address	–	tcp* – 25	–	ns	
Valid address → Valid data input	t_{AVDV}	Address/ Data	–	–	tcp* / 2 – 55	ns	
				–	tcp* / 2 – 80	ns	fcp ≤ 8 MHz
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$	–	3 tcp* / 2 – 25	–	ns	16 MHz < fcp ≤ 25 MHz
				3 tcp* / 2 – 20	–	ns	8 MHz < fcp ≤ 16 MHz
$\overline{RD}$ ↓ → Valid data input	t_{RLDV}	$\overline{RD}$, Data	–		3 tcp* / 2 – 55	ns	
					3 tcp* / 2 – 80	ns	fcp ≤ 8 MHz
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	$\overline{RD}$, Data	–	0	–	ns	
$\overline{RD}$ ↓ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE	–	tcp* / 2 – 15	–	ns	
$\overline{RD}$ ↑ → Address valid time	t_{RHAX}	Address, $\overline{RD}$	–	tcp* / 2 – 10	–	ns	
Valid address → CLK ↑ time	t_{AVCH}	Address, CLK	–	tcp* / 2 – 17	–	ns	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$,CLK	–	tcp* / 2 – 17	–	ns	
ALE ↓ → $\overline{RD}$ ↓ time	t_{LLRL}	$\overline{RD}$,ALE	–	tcp* / 2 – 15	–	ns	

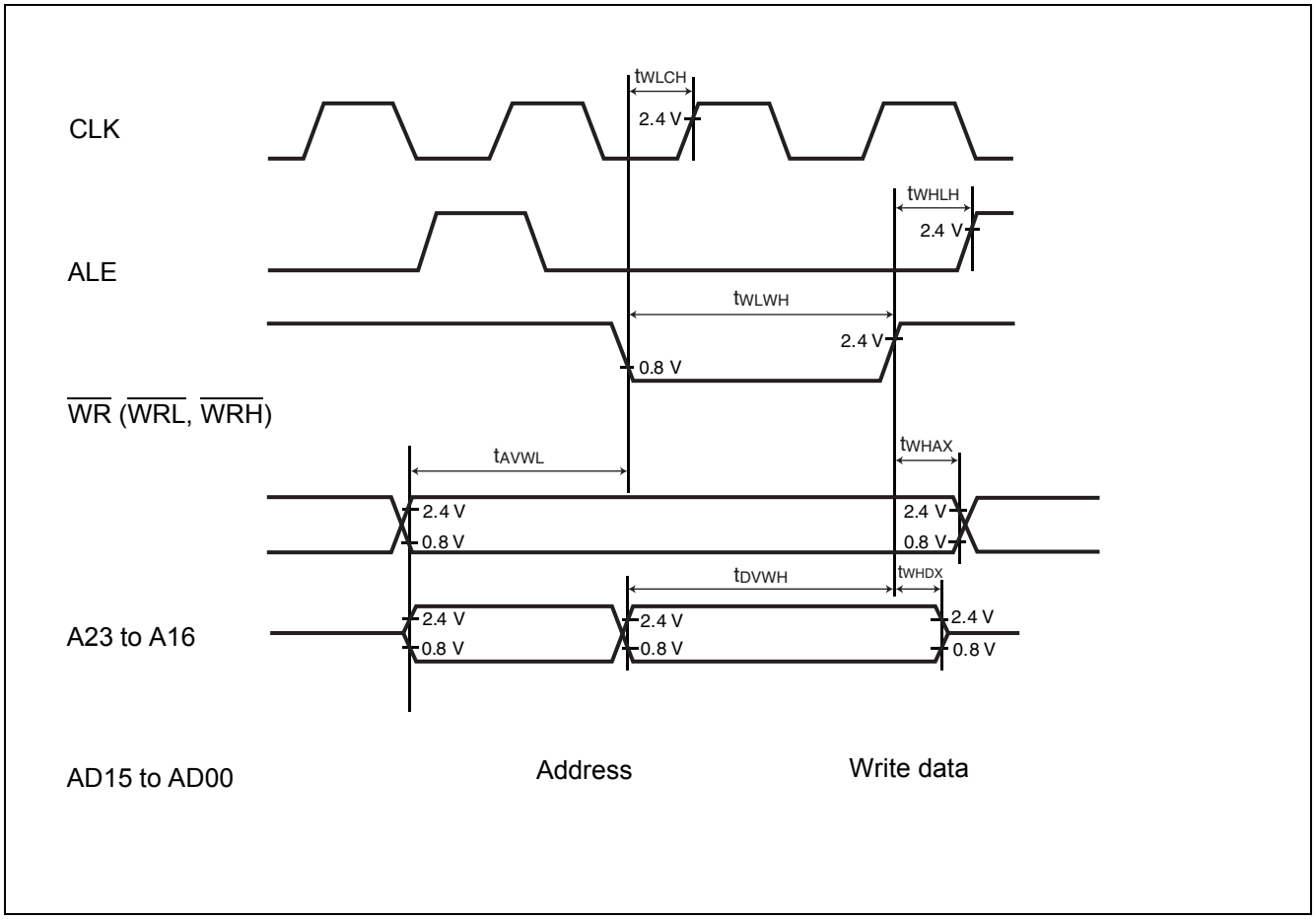
* : tcp is the Internal cycle time. Refer to “Clock Timing”.


tWLCH
2.4 V
tWHLH
2.4 V
tWLWH
2.4 V
0.8 V
tAVWL
tWHAX
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
2.4 V
0.8 V
2.4 V
0.8 V
2.4 V
0.8 V

11.4.6 Bus Timing (Write)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	Address, $\overline{WR}$	—	tcp* – 15	—	ns	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WRL}$, $\overline{WRH}$	—	3 tcp* / 2 – 25	—	ns	16 MHz < fcp ≤ 25 MHz
				3 tcp* / 2 – 20	—	ns	8 MHz < fcp ≤ 16 MHz
Valid data output → $\overline{WR}$ ↑ time	t_{DVWH}	Data, $\overline{WR}$	—	3 tcp* / 2 – 15	—	ns	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	$\overline{WR}$, Data	—	10	—	ns	16 MHz < fcp ≤ 25 MHz
				20	—	ns	8 MHz < fcp ≤ 16 MHz
				30	—	ns	fcp ≤ 8 MHz
$\overline{WR}$ ↑ → A ddress valid time	t_{WHAX}	$\overline{WR}$, Address	—	tcp* / 2 – 10	—	ns	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE	—	tcp* / 2 – 15	—	ns	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK	—	tcp* / 2 – 17	—	ns	

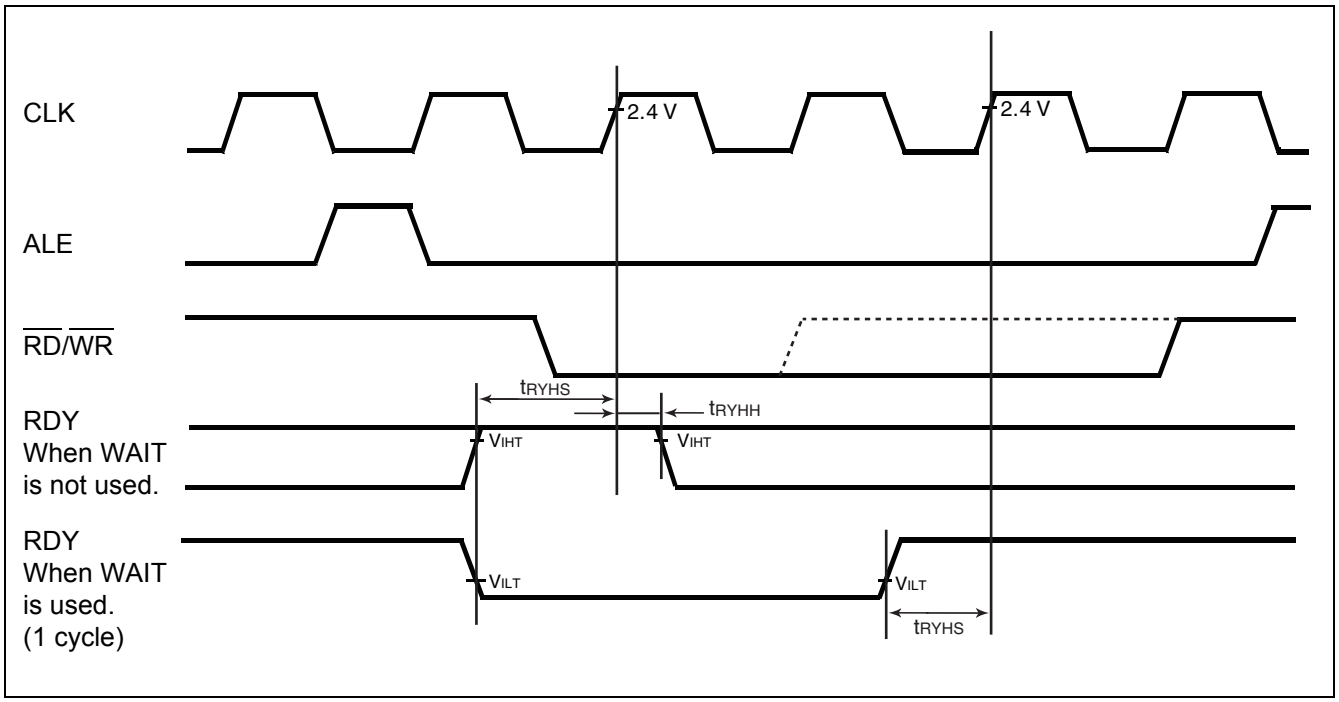
*: tcp is the Internal operating clock cycle time. Refer to “Clock Timing”.


CLK
ALE
WR (WRL, WRH)
A23 to A16
AD15 to AD00
tWLCH
2.4 V
tWHLH
2.4 V
tWLWH
2.4 V
0.8 V
tAVWL
tWHAX
2.4 V
0.8 V
2.4 V
0.8 V
tDVWH
tWHDX
2.4 V
0.8 V
2.4 V
0.8 V
2.4 V
0.8 V
Address
Write data

11.4.7 Ready Input Timing

Parameter	Symbol	Pin Name	Test Condition	Rated Value		Unit	Remarks
				Min	Max		
RDY setup time	t_{RYHS}	RDY	—	35	—	ns	
				70	—	ns	f_{CP} = 8 MHz
RDY hold time	t_{RYHH}	RDY		0	—	ns	

Note : If the RDY setup time is insufficient, use the auto-ready function.

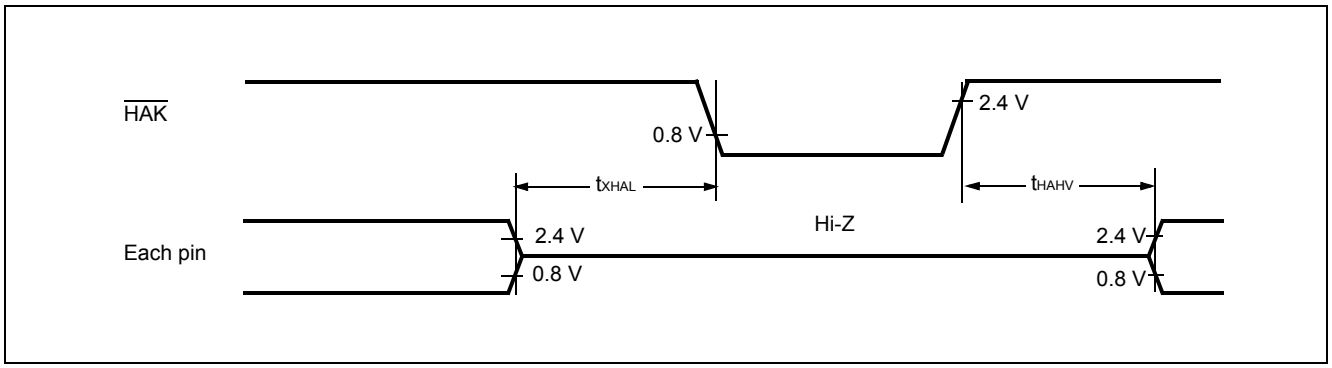


11.4.8 Hold Timing

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Pin floating → $\overline{HAK}$ ↓ time	t_{XHAL}	$\overline{HAK}$	—	30	t_{CP}*	ns
$\overline{HAK}$ ↓ → time → Pin valid time	t_{HAHV}	$\overline{HAK}$		t_{CP}*	2 t_{CP}*	ns

* : tcp is the Internal operating clock cycle time. Refer to “Clock Timing”.

Note : There is more than 1 cycle from when HRQ reads in until the $\overline{HAK}$ is changed.

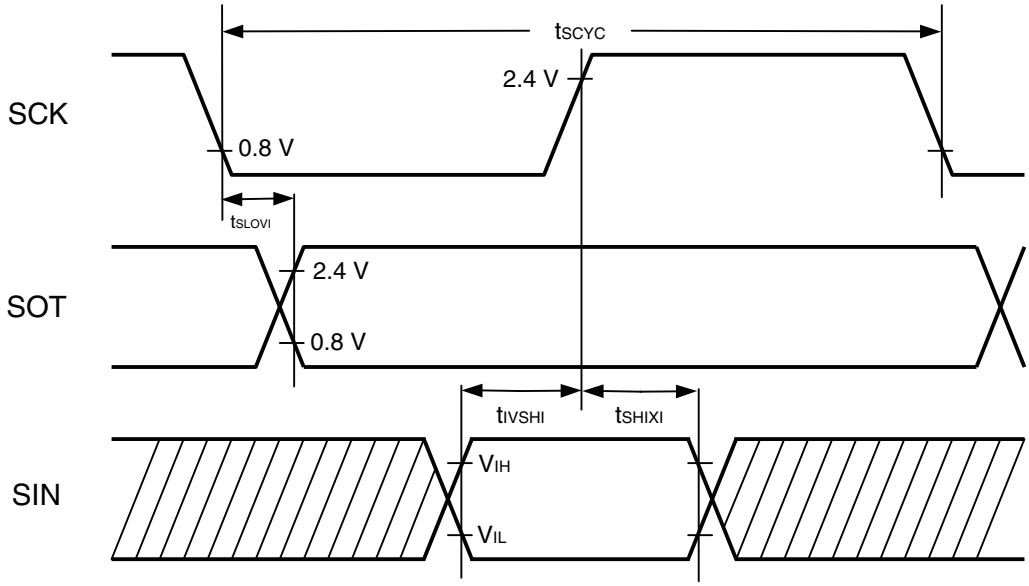


11.4.9 UART

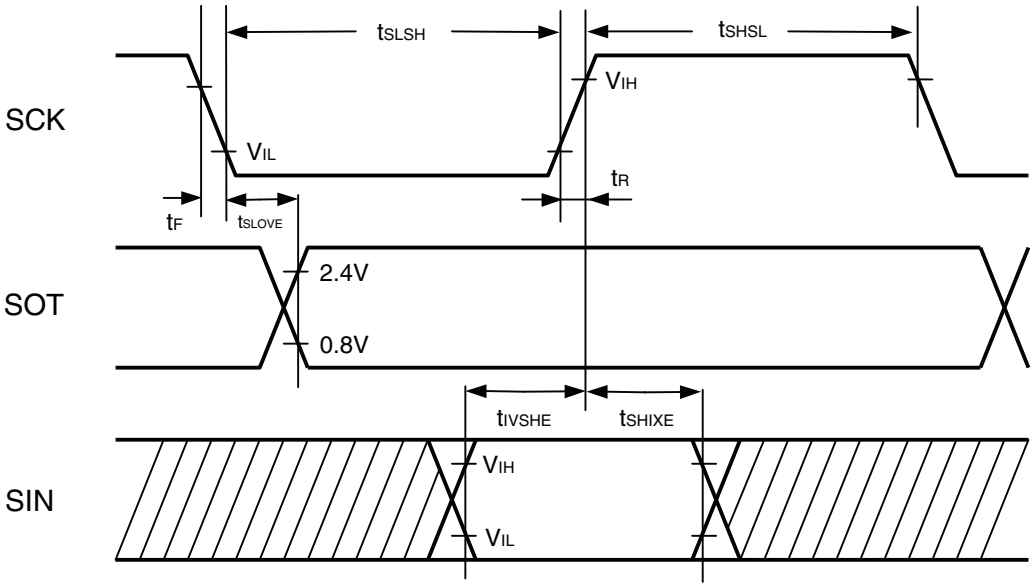
■ ESCR : SCES = 0, ECCR : SCDE = 0

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80 pF + 1 TTL.	5 tcp*	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}		– 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp* + 80	–	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	–	ns
Serial clock “H” pulse width	t_{SLSH}	External shift clock operation C_L = 80 pF + 1 TTL.	3 tcp* – t_R	–	ns
Serial clock “L” pulse width	t_{SHSL}		tcp* + 10	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}		–	2 tcp* + 60	ns
SIN → SCK ↑ setup time	t_{IVSHE}		30	–	ns
SCK ↑ → SIN hold time	t_{SHIXE}		tcp* + 30	–	ns
SCK fall time	t_F		–	10	ns
SCK rise time	t_R		–	10	ns

*: tcp indicates the machine clock time



Internal Clock Shift Operation

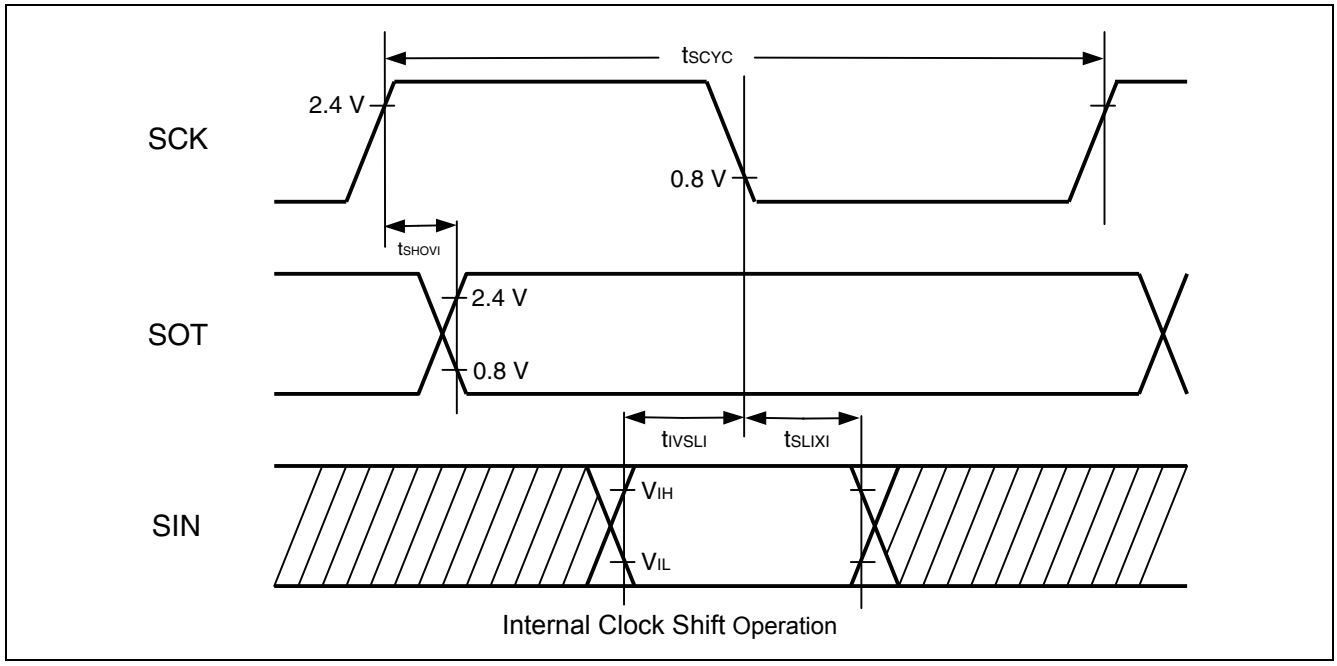


External Clock Shift Operation

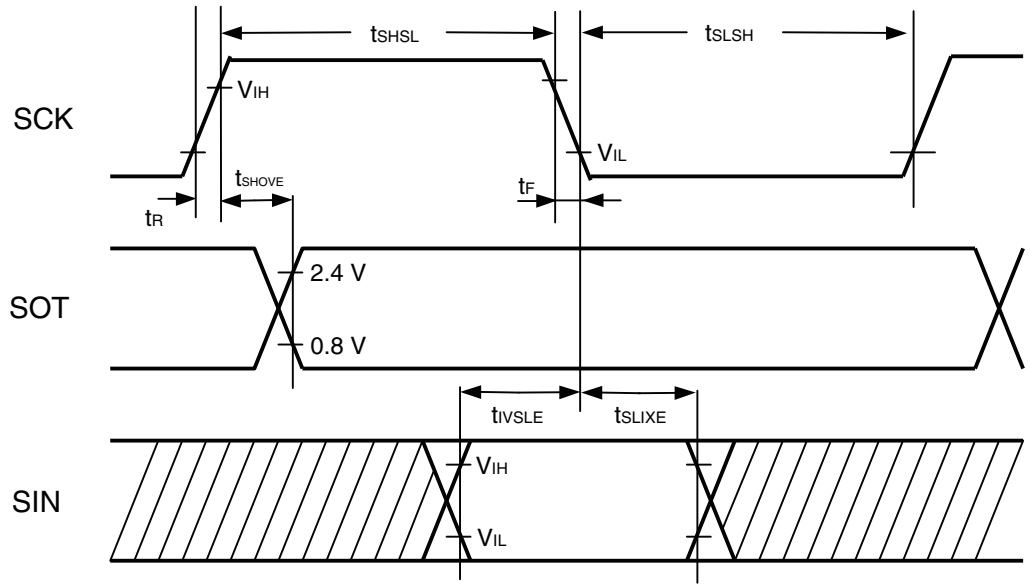
■ ESCR : SCES = 1, ECCR : SCDE = 0

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80 pF + 1 TTL.	5 tcp*	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}		– 50	+ 50	ns
SIN → SCK ↓ setup time	t_{IVSLI}		tcp* + 80	–	ns
SCK ↓ → SIN hold time	t_{SLIXI}		0	–	ns
Serial clock “H” pulse width	t_{SHSL}	External shift clock operation C_L = 80 pF + 1 TTL.	3 tcp* – t_R	–	ns
Serial clock “L” pulse width	t_{SLSH}		tcp* + 10	–	ns
SCK ↑ → SOT delay time	t_{SHOVE}		–	2 tcp* + 60	ns
SIN → SCK ↓ setup time	t_{IVSLE}		30	–	ns
SCK ↓ → SIN hold time	t_{SLIXE}		tcp* + 30	–	ns
SCK fall time	t_F		–	10	ns
SCK rise time	t_R		–	10	ns

*: tcp indicates the machine clock time



Internal Clock Shift Operation

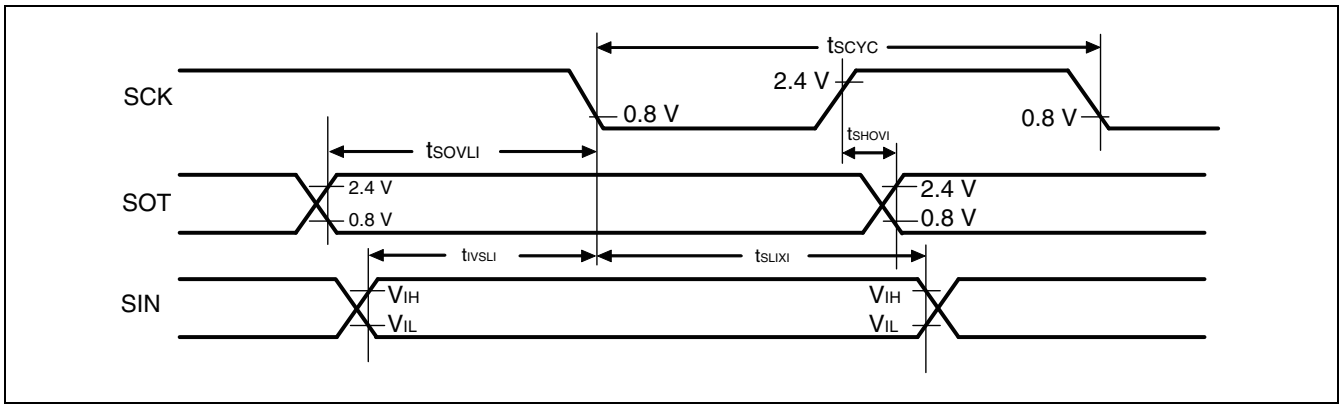


External Clock Shift Operation

■ ESCR : SCES = 0, ECCR : SCDE = 1

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal shift clock operation C_L = 80 pF + 1 TTL.	5 tcp*	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}		– 50	+ 50	ns
SIN → SCK ↓ setup time	t_{IVSLI}		tcp* + 80	–	ns
SCK ↓ → SIN hold time	t_{SLIXI}		0	–	ns
SOT → SCK ↓ delay time	t_{SOVLI}		3 tcp* – 70	–	ns

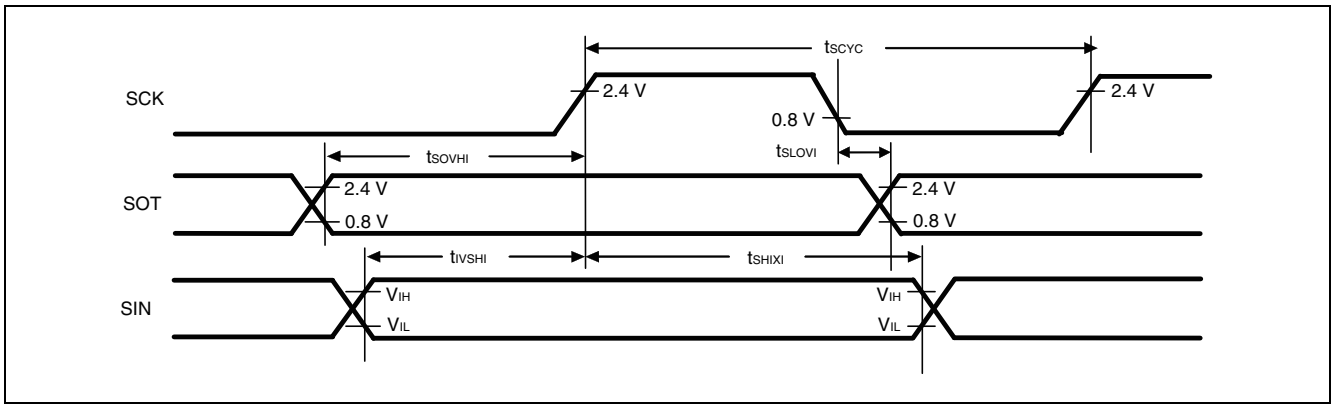
*: tcp indicates the machine clock time



■ ESCR : SCES = 1, ECCR : SCDE = 1

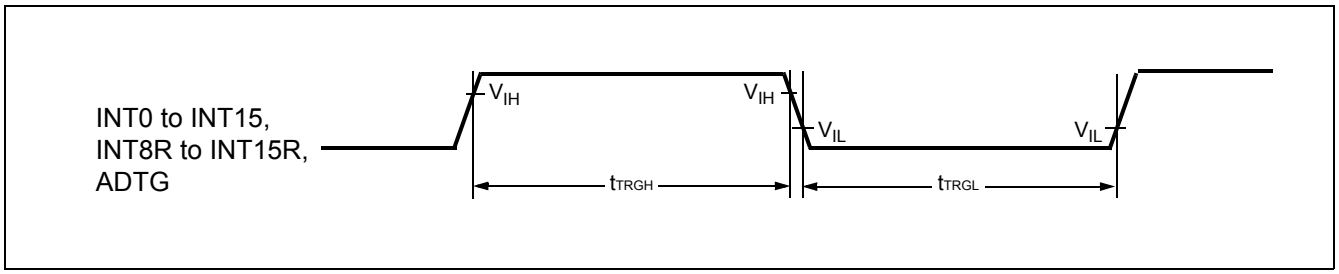
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Serial clock cycle time	t_{SCYC}	Internal clock operation C_L = 80 pF + 1 TTL.	5 tcp*	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}		– 50	+ 50	ns
SIN → SCK ↑ setup time	t_{IVSHI}		tcp* + 80	–	ns
SCK ↑ → SIN hold time	t_{SHIXI}		0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}		3 tcp* – 70	–	ns

*: tcp indicates the machine clock time



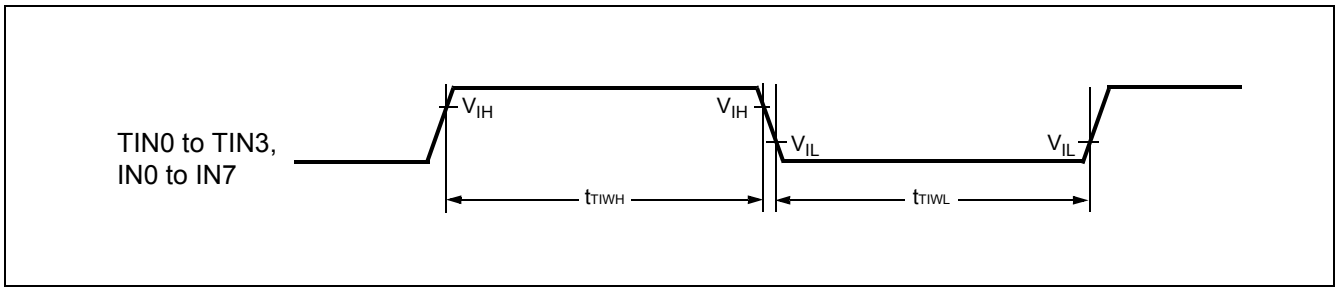
11.4.10 rigger Input Timing

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT15, INT8R to INT15R, ADTG	–	5 t_{CP}	–	ns



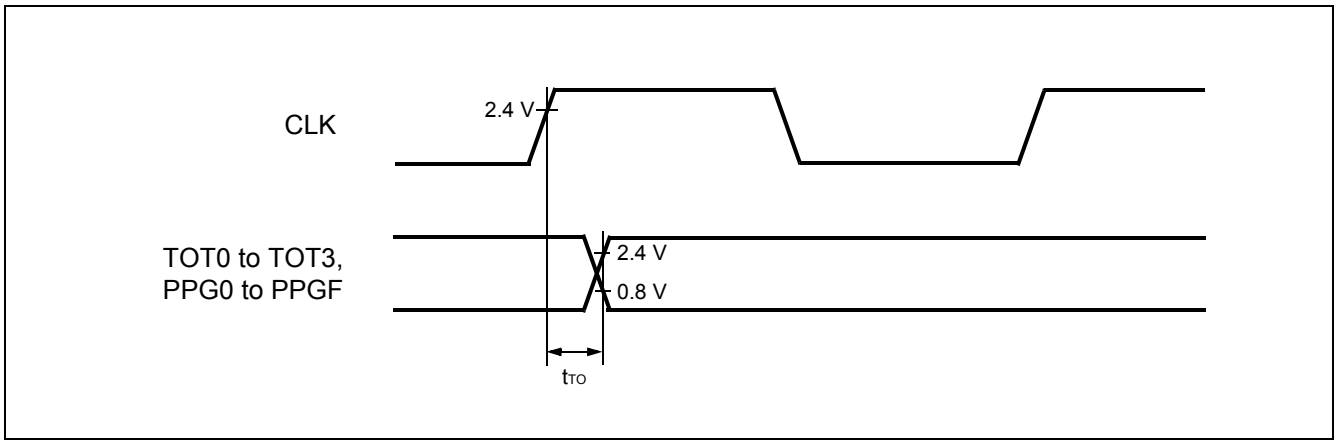
11.4.11 Timer Related Resource Input Timing

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	TIN0 to TIN3, IN0 to IN7	–	4 t_{CP}	–	ns



11.4.12 Timer Related Resource Output Timing

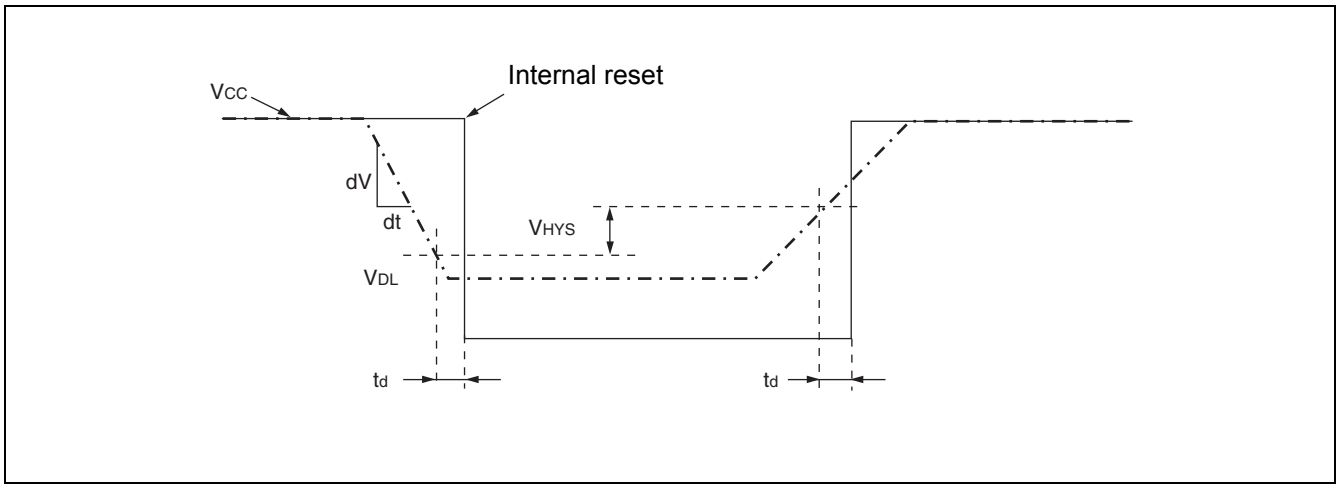
Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
CLK ↑ → T_{OUT} change time	t_{TO}	TOT0 to TOT3, PPG0 to PPGF	–	30	–	ns



11.4.13 Low voltage detection

Parameter	Symbol	Pin Name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Detection voltage initial value	V_{DL}	V_{CC}	—	3.8	4.0	4.2	V	During voltage drop
Hysteresis width	V_{HYS}	V_{CC}	—	169	173	177	mV	During voltage rise
Power supply voltage change rate	dV/dt	V_{CC}	—	− 0.1	—	+ 0.1	V/μs	dV/dt at low voltage reset
				− 0.004	—	+ 0.004	V/μs	dV/dt at standard value of low voltage detection/release voltage
Detection delay time	td	—	—	—	—	3.2	μs	When | dV/dt | ≤ 0.004 V/μs

Note: The power supply voltage change rate is at 0.004 V/μs<|dv/dt|<0.1 V/μs, a reset may be generated or released after the power supply voltage is passed the detection voltage range.



11.4.14 I^2C Timing

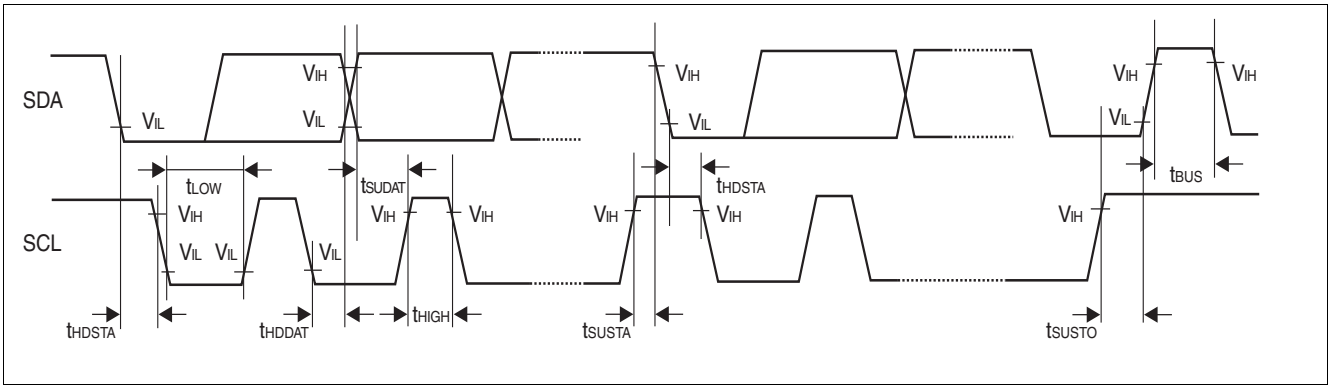
Parameter	Symbol	Conditions	Standard-mode		Fast-mode*1		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	R = 1.7 kΩ, C = 50 pF*2	0	100	0	400	kHz
Hold time (repeated) START condition SDA↓ → SCL ↓	t_{HDSTA}		4.0	–	0.6	–	µs
"L" width of the SCL clock	t_{LOW}		4.7	–	1.3	–	µs
"H" width of the SCL clock	t_{HIGH}		4.0	–	0.6	–	µs
Set-up time (repeated) START condition SCL ↑ → SDA ↓	t_{SUSTA}		4.7	–	0.6	–	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*3	0	0.9*4	µs
Data set-up time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	–	100	–	ns
Set-up time for STOP condition SCL ↑ → SDA ↑	t_{SUSTO}		4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUS}		4.7	–	1.3	–	µs

*1: For use at over 100 kHz, set the machine clock to at least 6 MHz.

*2: R,C: Pull-up resistor and load capacitor of the SCL and SDA lines.

*3: The maximum t_{HDDAT} meets the requirement that it does not extend the "L" width (t_{LOW}) of the SCL signal.

*4: A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SUDAT} \geq 250$ ns must then be met.

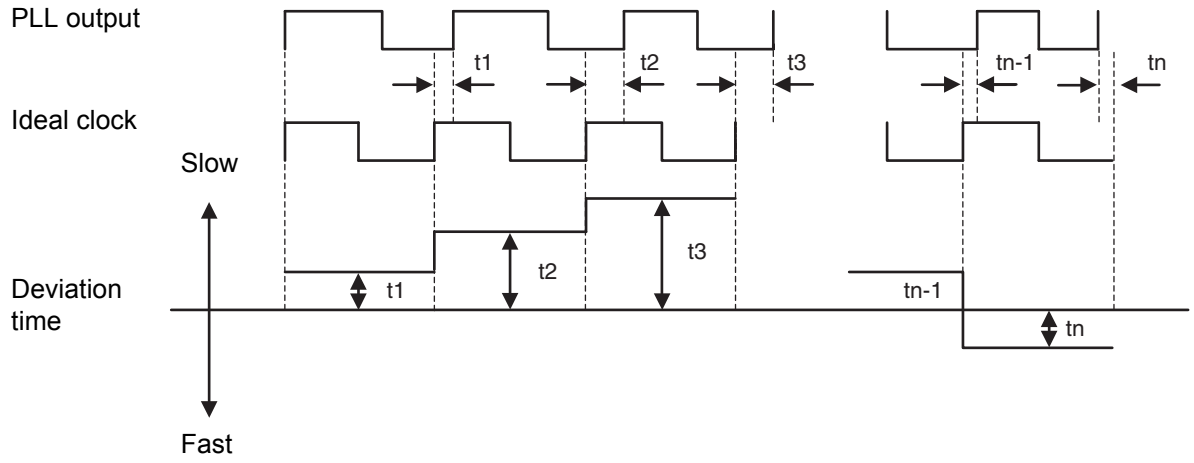


11.4.15 CAN PLL cycle jitter

Parameter	Sym-bol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
CAN PLL cycle jitter (When locked)	t_{PJ}	–	–	– 10	–	+ 10	ns	F_{CP} = 16 MHz (4 MHz×multiplied by 4) 24 MHz (4 MHz×multiplied by 6) 32 MHz (4 MHz×multiplied by 8)

- CAN PLL cycle jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



11.5 A/D Converter

(3.0 V ≤ AVRH − AVRL)

Parameter	Symbol	Pin Name	Condi-tions	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	—	10	bit	
Total error	—	—	—	—	—	±3.0	LSB	
Nonlinearity error	—	—	—	—	—	±2.5	LSB	
Differential nonlinearity error	—	—	—	—	—	±1.9	LSB	
Zero reading voltage	V_{OT}	AN0 to AN23	—	AVRL − 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	AN0 to AN23	—	AVRH − 3.5 LSB	AVRH − 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	—	—	—	0.66	—	16500	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
				2.2				3.0 V ≤ AV_{CC} < 4.5 V
Sampling time	—	—	—	0.4	—	×	µs	4.5 V ≤ AV_{CC} ≤ 5.5 V
				1.0				3.0 V ≤ AV_{CC} < 4.5 V
Analog port input current	I_{AIN}	AN0 to AN23	—	−0.3	—	+0.3	µA	
Analog input voltage range	V_{AIN}	AN0 to AN23	—	AVRL	—	AVRH	V	
Reference voltage range	—	AVRH	—	AVRL + 2.7	—	AV_{CC}	V	
	—	AVRL	—	0	—	AVRH − 2.7	V	
Power supply current	I_A	AV_{CC}	—	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	—	600	900	µA	
	I_{RH}	AVRH	—	—	—	5	µA	*
Offset between input channels	—	AN0 to AN23	—	—	—	4	LSB	

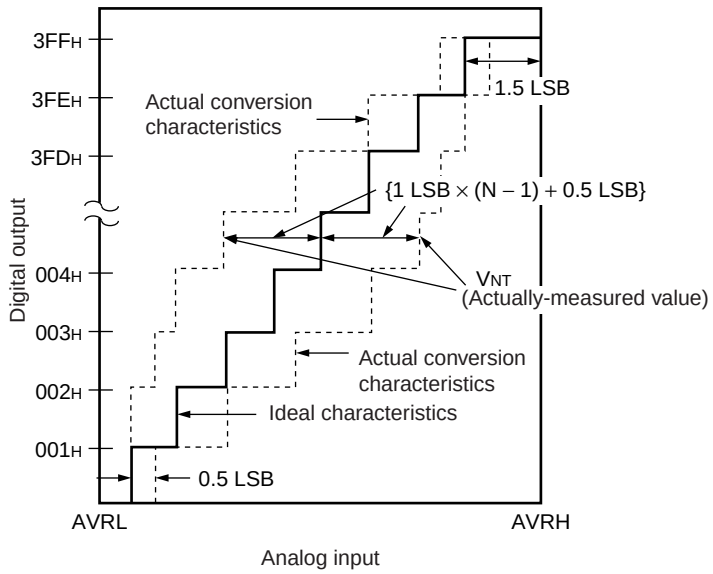
*: If the A/D convertor is not operating, a current when CPU is stopped is applicable (V_{CC} = AV_{CC} = AVRH = 5.0 V) .

Note: The accuracy gets worse as |AVRH − AVRL| becomes smaller.

11.6 Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by the A/D converter.
Non linearity error	:	The deviation between the actual conversion characteristics and a line that joins the zero-transition line (“00 0000 0000” ← → “00 0000 0001”) to the full-scale transition line (“11 1111 1110” ← → “11 1111 1111”) .
Differential linearity error	:	Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	:	Difference between the actual value and the ideal value. The total error includes zero transition error, full-scale transition error, and linear error.

Total error



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB (Ideal value)} = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

N : Value of the digital output from the A/D converter

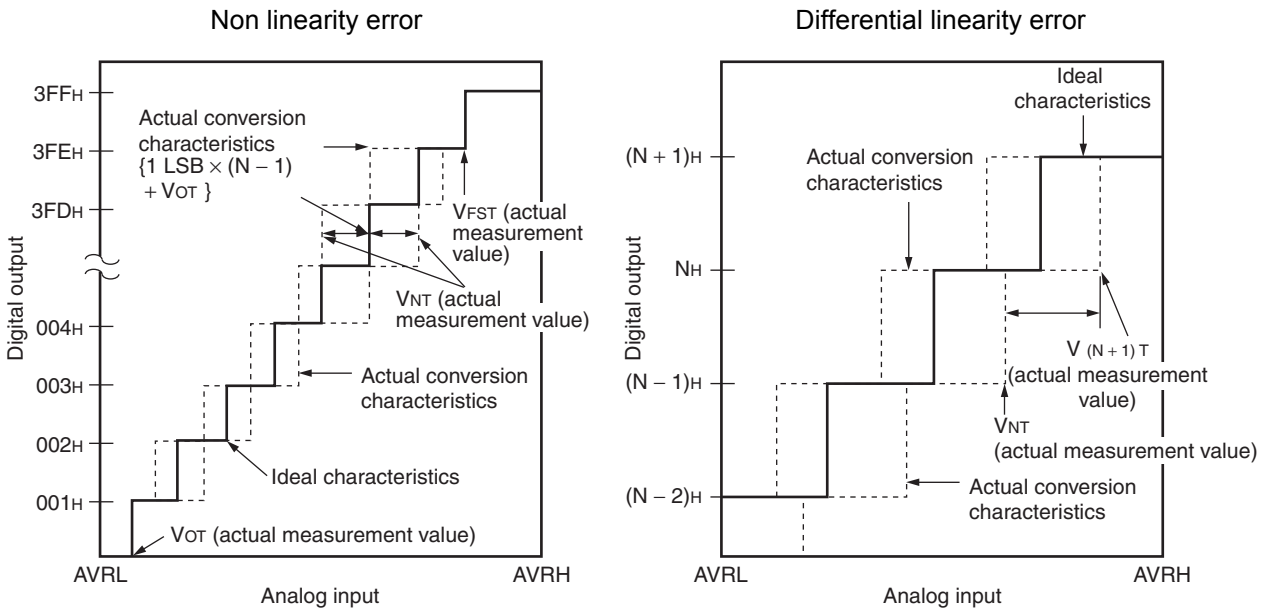
V_{OT} (Ideal value) = AVRL + 0.5 LSB [V]

V_{FST} (Ideal value) = AVRH – 1.5 LSB [V]

V_{NT} : A voltage at which the digital output transitions from $(N - 1)_H$ to N_H.

(Continued)

(Continued)



$$\text{Non linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1)\ + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

N : Value of the digital output from the A/D converter
V_{OT} : Voltage at which digital output transits from "000_H" to "001_H."
V_{FST} : Voltage at which digital output transits from "$3FE_H$" to "$3FF_H$."

11.7 Notes on A/D Converter Section

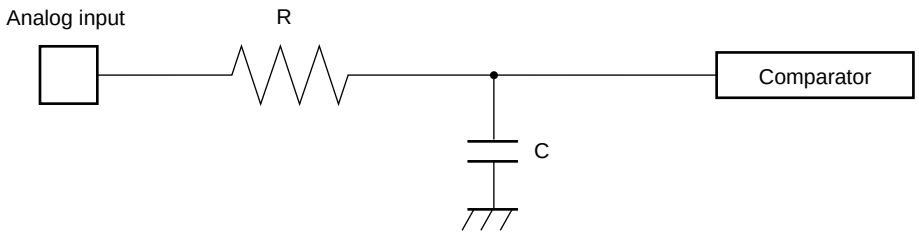
Use the device with external circuits of the following output impedance for analog inputs :

Recommended output impedance of external circuits are : Approx. 4.2 kΩ or lower (4.5 V ≤ AV_{CC} ≤ 5.5 V, sampling period = 0.4 μs)

If an external capacitor is used, in consideration of the capacitive voltage dividing effect between the external capacitor and the internal on-chip capacitor, it is recommended that the capacitance of the external capacitor be several thousand times greater than the capacitance of the internal capacitor.

If the output impedance of the external circuit is too high, a sampling period for an analog voltage may be insufficient.

- Analog input circuit model

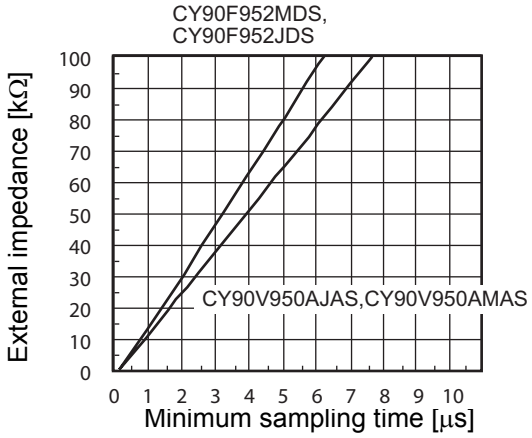


CY90F952JDS/F952MDS	4.5 V ≤ AV_{CC} ≤ 5.5 V : R ≔ 4.1 kΩ, C ≔ 8.5 pF
	3.0 V ≤ AV_{CC} < 4.5 V : R ≔ 10.33 kΩ, C ≔ 8.5 pF
CY90V950AJAS/V950AMAS	4.5 V ≤ AV_{CC} ≤ 5.5 V : R ≔ 2.52 kΩ, C ≔ 10.7 pF

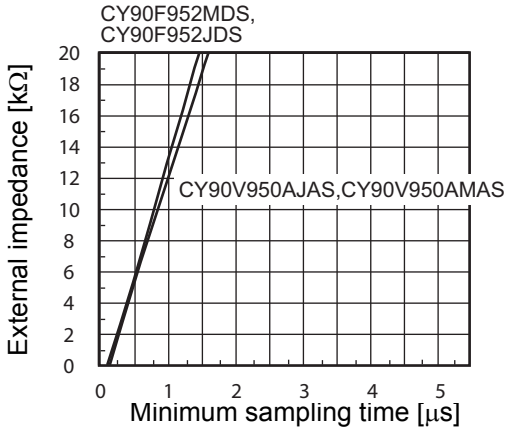
Note : Use the values in the figure only as a guideline.

- The relationship between external impedance and minimum sampling time
  - At 4.5 V ≤ AV_{CC} ≤ 5.5 V

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)

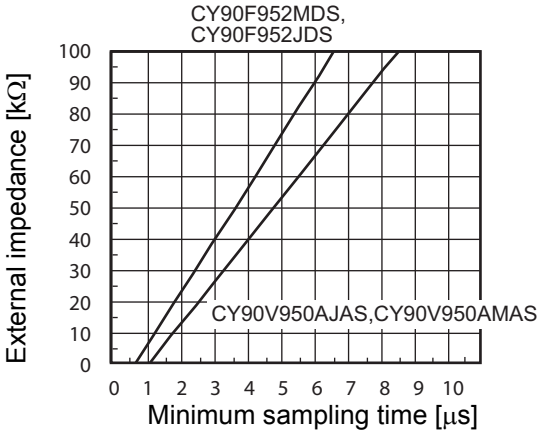


	Minimum sampling time [µs] (4.5 V ≤ AV_{CC} ≤ 5.5 V)		
External impedance [kΩ]	5	10	50
CY90F952MDS,CY90F952JDS	0.54	0.84	3.22
CY90V950AJAS,CY90V950AMAS	0.56	0.94	3.93

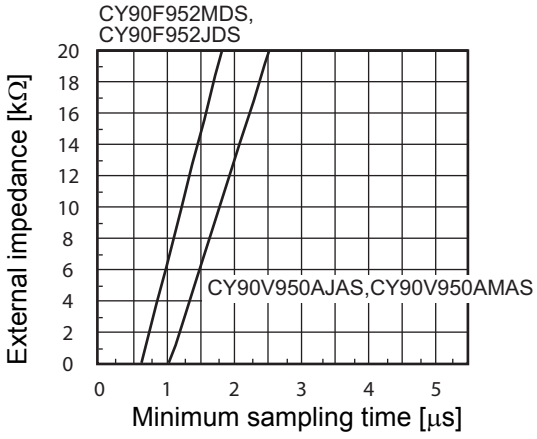
  - At 3.0 V ≤ AV_{CC} < 4.5 V

(CY90V950 is at 4.0 V ≤ AVcc < 4.5 V)

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



	Minimum sampling time [µs] (3.0 V ≤ AV_{CC}<4.5 V)		
External impedance [kΩ]	5	10	50
CY90F952MDS,CY90F952JDS	0.91	1.21	3.59
CY90V950AJAS,CY90V950AMAS	1.39	1.77	4.76

•About errors

As | AVR − AV_{SS} | becomes smaller, values of relative errors grow larger.

11.8 Flash Memory Program/Erase Characteristics

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	—	—	0.9	3.6	s	Excludes programming prior to erasure
Chip erase time		—	7.2	28.8	s	Main Flash
		—	3.6	14.4	s	Satellite Flash
Word (16-bit width) programming time		—	15	240	µs	Except for the overhead time of the system
Word (16-bit width) programming time		—	23	370	µs	Except for the overhead time of the system
Program/Erase cycle	T_A > +85 °C	10000	—	—	cycle	
	T_A ≤ +85 °C	100000	—	—	cycle	
Flash Data Retention Time	Average T_A = +85 °C	20	—	—	year	*

* : The value was converted into the normalized temperature at +85ÅãC from the results of evaluating the reliability of the technology.

11.9 D/A Converter

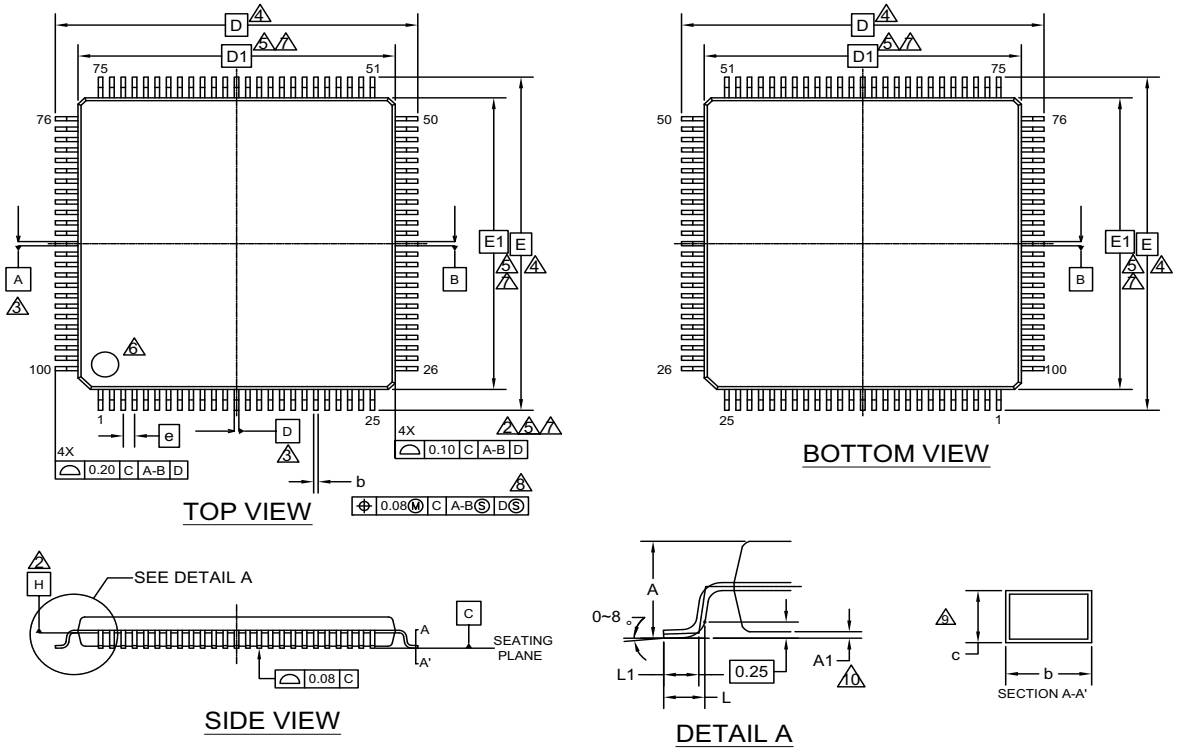
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	—	—	8	—	bit	
Non linearity error	—	—	—	-0.5	—	+0.5	LSB	
Conversion time	—	—	—	0.773	0.787	1.078	µs	C_L = 20 pF
			—	2.490	2.535	3.474		C_L = 100 pF
Output impedance	R_O	DA0, DA1	—	3.19	3.50	4.80	kΩ	
Power supply current	I_A	AV_{CC}	—	—	476	920	µA	
	I_{AH}	AV_{CC}	—	—	—	5	µA	

12. Ordering Information

Part number	Package	Remarks
CY90F952JDSPMC-GS-UJE1	100-pin plastic LQFP (LQI100)	

13. Package Dimensions

Package Type	Package Code
LQFP 100	LQI100



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.15	—	0.27
c	0.09	—	0.20
D	16.00 BSC		
D1	14.00 BSC		
e	0.50 BSC		
E	16.00 BSC		
E1	14.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

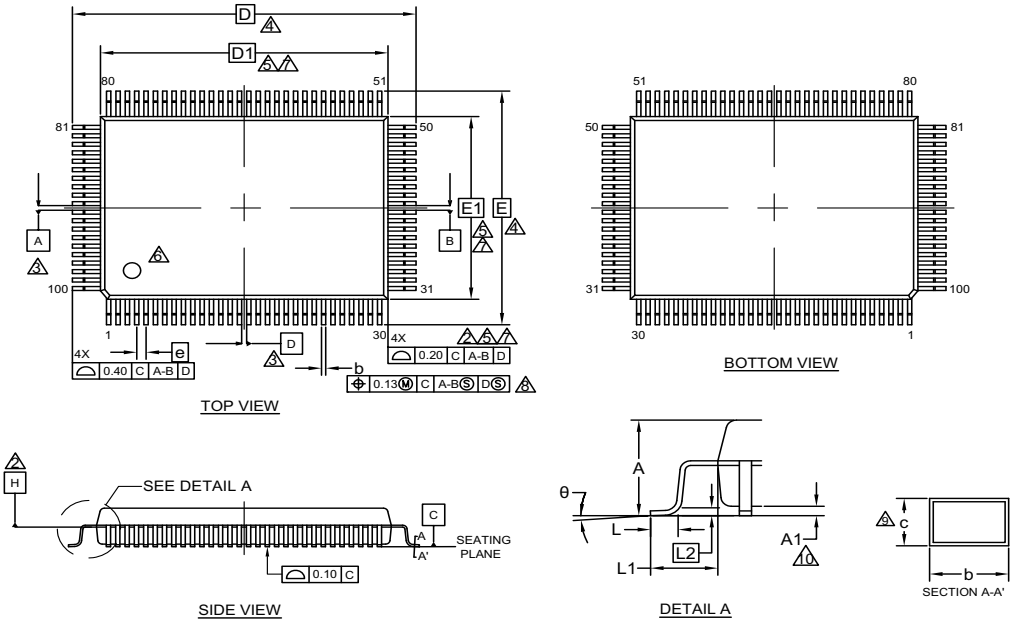
NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11500 *A

PACKAGE OUTLINE, 100 LEAD LQFP
14.0X14.0X1.7 MM LQI100 REV*A

Package Type	Package Code
QFP 100	PQH100 *



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.35
A1	0.05	—	0.45
b	0.27	0.32	0.37
c	0.11	—	0.23
D	23.90 BSC		
D1	20.00 BSC		
e	0.65 BSC		
E	17.90 BSC		
E1	14.00 BSC		
θ	0°	—	8°
L	0.73	0.88	1.03
L1	1.95 REF		
L2	0.25 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15156 **

*: Only for support

PACKAGE OUTLINE, 100 LEAD QFP
20.00X14.00X3.35 MM PQH100 REV**

14. Major Changes

Spansion Publication Number: DS07-13752-4E

Page	Section	Change Results
–	–	Changed the part number; MB90V950MAS→MB90V950AMAS MB90V950JAS→MB90V950AJAS
74	Electrical Characteristics AC Characteristics	Added the item “(15) CAN PLL cycle jitter”.
Rev.*B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix.	
6, 7, 15, 81, 82, 83	2.Pin Assignments 3.Pin Description 12.Ordering Information 13.Package Dimensions	Package description modified to JEDEC description. FPT-100P-M06 → PQH100 FPT-100P-M20 → LQI100
81	12.Ordering Information	Revised Marketing Part Numbers as follows: Before) MB90F952JDSPF MB90F952MDSPF MB90F952JDSPFV MB90F952MDSPFV MB90V950AMASCR-ES MB90V950AJASCR-ES After) CY90F952JDSPMC-GS-UJE1
Rev.*C		
1	—	Company name changed Fujitsu to Cypress.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY90F952JDS/F952MDS, CY90V950AJAS/V950AMAS F^{2}MC-16LX CY90950 Series 16-bit Microcontrollers Document Number: 002-04500				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	06/29/2009	Migrated to Cypress and assigned document number 002-04500. No change to document contents or format.
*A	5209387	AKIH	04/13/2016	Updated to Cypress template
*B	6013526	KUME	01/05/2018	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 2.Pin Assignments 3.Pin Description 12.Ordering Information 13.Package Dimension For details, please see 14.Major Changes.
*C	6129329	GSHI	04/10/2018	Company name changed Fujitsu to Cypress.

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