SiS176LDN

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Vishay Siliconix



PRODUCT SUMMARY						
V _{DS} (V)	70					
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0109					
$R_{DS(on)}$ max. (Ω) at V_{GS} = 3.3 V	0.0125					
Q _g typ. (nC)	9.2					
I _D (A)	42.3					
Configuration	Single					

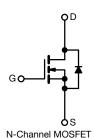
FEATURES

N-Channel 70 V (D-S) MOSFET

- TrenchFET[®] Gen IV power MOSFET
- Very low R_{DS} x Q_g figure-of-merit (FOM)
- Tuned for the lowest R_{DS} x Q_{oss} FOM
- 100 % R_q and UIS tested
- · Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Synchronous rectification
- Primary side switch
- DC/DC converter
- Motor drive control
- Load switch



ORDERING INFORMATION

Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiS176LDN-T1-GE3

ABSOLUTE MAXIMUM RATING	S (T _A = 25 °C, u	inless otherw	ise noted)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	70	v	
Gate-source voltage		V _{GS}	± 12	v	
	T _C = 25 °C		42.3		
Continuous drain current ($T_J = 150 \ ^{\circ}C$)	T _C = 70 °C	Ι. Γ	33.8		
	T _A = 25 °C		12.9 ^{b, c}		
	T _A = 70 °C	1 [10.3 ^{b, c}	•	
Pulsed drain current (t = 100 μs)		I _{DM}	100	— A	
	T _C = 25 °C		35.4		
Continuous source-drain diode current	T _A = 25 °C	I _S	3.2 ^{b, c}		
Single pulse avalanche current L = 0.1 mH		I _{AS}	15		
Single pulse avalanche energy L = 0.1 mH		E _{AS}	11.25	mJ	
	T _C = 25 °C		39		
Maximum neuror discinction	T _C = 70 °C		25	10/	
Maximum power dissipation	T _A = 25 °C	P _D	3.6 ^{b, c}	W	
	T _A = 70 °C	1 [2.4 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^c		Ŭ Ŭ	260	-0	

THEDMAL REGISTANCE BATINGS

	nas				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b	t ≤ 10 s	R _{thJA}	26	34	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	2.4	3.2	0/10

Notes

a. Package limited

b. Surface mounted on 1" x 1" FR4 board

t = 10 s c. d.

See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

Rework conditions: manual soldering with a soldering iron is not recommended for leadless components Maximum under steady state conditions is 81 °C/W

f.

g. T_C = 25 °C

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RoHS COMPLIANT

HALOGEN

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SiS176LDN

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			•			
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	70	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA		45	-	
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-3.2	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$	0.6	-	1.6	V
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 12 V$	-	-	100	nA
		$V_{DS} = 70 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	
Zero gate voltage drain current	IDSS	$V_{DS} = 70 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 70 ^{\circ}\text{C}$	-	-	15	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	40	-	-	Α
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	0.0086	0.0109	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 3.3 \text{ V}, I_D = 10 \text{ A}$	-	0.0097	0.0125	Ω
Forward transconductance ^a	g _{fs}	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$	-	60	_	S
Dynamic ^b	513					
Input capacitance	C _{iss}		-	1660	-	
Output capacitance	C _{oss}	V _{DS} = 35 V, V _{GS} = 0 V, f = 1 MHz	-	175	-	pF
Reverse transfer capacitance	C _{rss}		-	9	-	
		$V_{DS} = 35 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	-	12.6	19	
Total gate charge	Qg		-	9.2	14	
Gate-source charge	Q _{gs}	$V_{DS} = 35 \text{ V}, V_{GS} = 3.3 \text{ V}, I_{D} = 10 \text{ A}$	-	3.9	-	nC
Gate-drain charge	Q _{gd}		-	2.3	-	
Output charge	Q _{oss}	$V_{DS} = 35 \text{ V}, V_{GS} = 0 \text{ V}$	-	15.8	-	
Gate resistance	Rg	f = 1 MHz	0.3	0.9	1.5	Ω
Turn-on delay time	t _{d(on)}		-	10	20	
Rise time	t _r	V_{DD} = 35 V, R_L = 3.5 Ω , $I_D \cong$ 10 A,	-	6	12	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$	-	25	50	
Fall time	t _f		-	6	12	
Turn-on delay time	t _{d(on)}		-	18	36	ns
Rise time	t _r	V_{DD} = 35 V, R_L = 3.5 Ω , $I_D \cong$ 10 A,	-	22	44	
Turn-off delay time	t _{d(off)}	V_{GEN} = 4.5 V, R_g = 1 Ω	-	28	56]
Fall time	t _f		-	9	18	
Drain-Source Body Diode Characteristi	cs		-			
Continuous source-drain diode current	I _S	$T_{C} = 25 \ ^{\circ}C$	-	-	42.3	^
Pulse diode forward current	I _{SM}			-	100	A
Body diode voltage	V _{SD}	$I_{S} = 5 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.77	1.1	V
Body diode reverse recovery time	t _{rr}		-	30	60	ns
Body diode reverse recovery charge	Q _{rr}	I _F = 10 A, di/dt = 100 A/μs,	-	29	58	nC
Reverse recovery fall time	t _a	$T_J = 25 \ ^\circ C$	-	19	-	
Reverse recovery rise time	t _b	1		11	-	ns

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

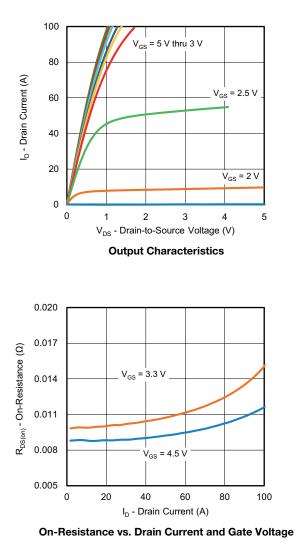
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

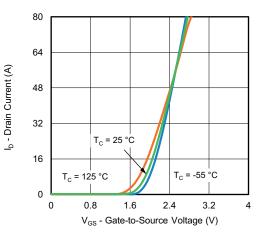
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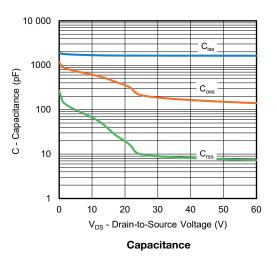
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

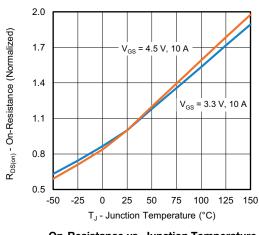


4.5 V_{GS} - Gate-to-Source Voltage (V) I_D = 10 A 3.6 2.7 1.8 = 20 V, 35 V, 50 V Vne 0.9 0 0 3 6 9 12 15 Q_q - Total Gate Charge (nC) Gate Charge



Transfer Characteristics





On-Resistance vs. Junction Temperature

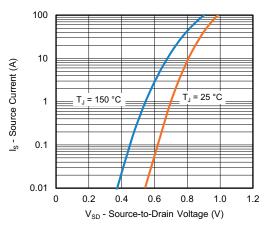
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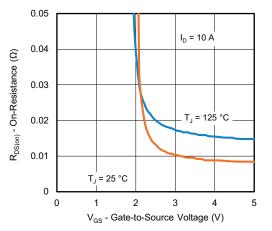
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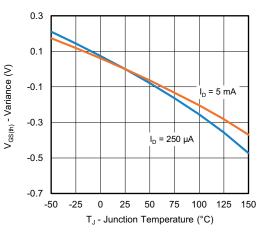
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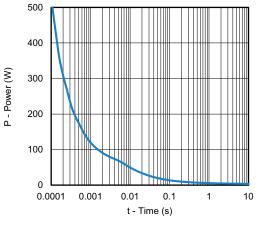
Source-Drain Diode Forward Voltage



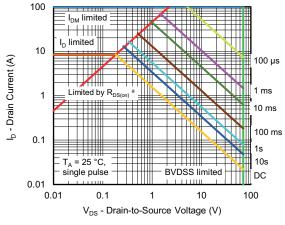
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

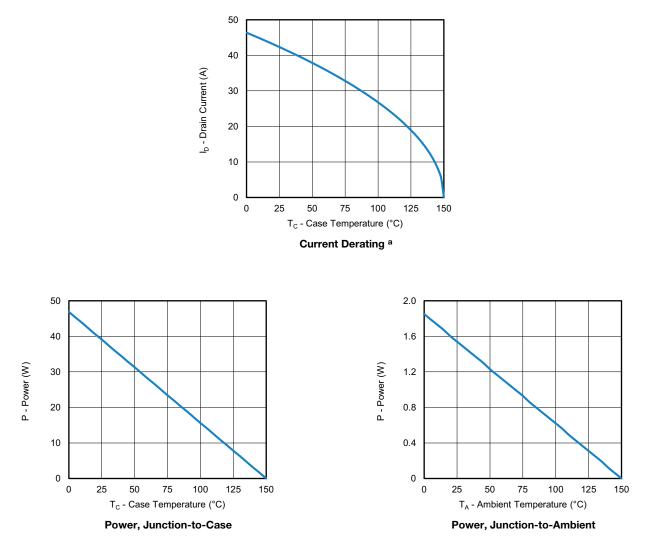
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

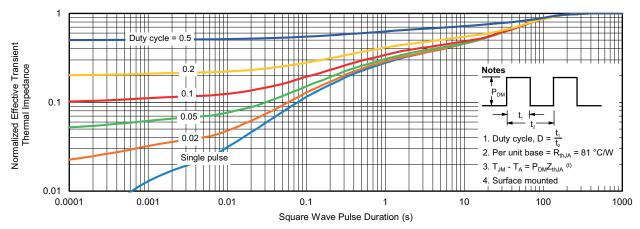


Note

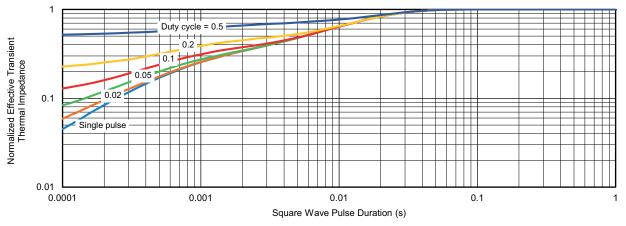
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

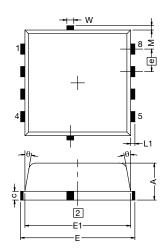


Normalized Thermal Transient Impedance, Junction-to-Case

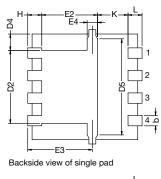
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PowerPAK® 1212-8, (Single / Dual)









Notes

1. Inch will govern

Dimensions exclusive of mold gate burrs
Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES			
DINI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	0.97	1.04	1.12	0.038	0.041	0.044	
A1	0.00	-	0.05	0.000	-	0.002	
b	0.23	0.30	0.41	0.009	0.012	0.016	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
D3	0.48	-	0.89	0.019	-	0.035	
D4		0.47 typ.		0.0185 typ			
D5		2.3 typ.			0.090 typ		
E	3.20	3.30	3.40	0.126	0.130	0.134	
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	1.75	1.85	1.98	0.069	0.073	0.078	
E4		0.034 typ.			0.013 typ.		
е		0.65 BSC		0.026 BSC			
К		0.86 typ.			0.034 typ.		
K1	0.35	-	-	0.014	-	-	
Н	0.30	0.41	0.51	0.012	0.016	0.020	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.			0.005 typ.			
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Revison: 09-Jan-17

Document Number: 71656

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RECOMMENDED MINIMUM PADS FOR PowerPAK[®] 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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